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Low complexity pipeline FFT processor for MIMO-OFDM systems

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Abstract: In this paper, we propose a low complexity pipeline FFT processor for MIMO-OFDM systems with four transmitting and four receiving (4×4) antennas. The proposed FFT processor is based on multi-channel structure which enables to support multiple data streams efficiently. With mixed-radix algorithm, the number of non-trivial multiplications of the proposed FFT processor are decreased. Implementation results show that the proposed FFT processor reduces the required number of logic gates by 25% over the conventional 4-channel R4MDC FFT processor which has been considered to be the most area-efficient FFT processor for 4×4 MIMO-OFDM systems.

Keywords: FFT, MIMO-OFDM, pipeline, mixed-radix

Classification: Science and engineering for electronics

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1 Introduction

Wireless communication systems with multiple antennas at the transmitter and receiver, known as multiple-input multiple-output (MIMO) systems, have recently received considerable attention due to their ability to increase system capacity without bandwidth expansion [1]. In particular, the combination of MIMO signal processing with orthogonal frequency division multiplexing (OFDM) is considered as a promising method of enhancing the data rates of future wireless communication systems such as IEEE 802.11n WLAN, IEEE 802.16e mobile WiMAX and 4 G. However, since the MIMO-OFDM system transmits multiple data streams, it requires several independent baseband processors and its hardware complexity dramatically increases compared with single-input single-output OFDM (SISO-OFDM) systems [1]. Since the FFT processor is one of the highest complex modules in the OFDM baseband processor [2], it is very important to design the FFT processor as efficiently as possible.

The radix-2^3 single-path delay feedback (R2^3SDF) pipeline FFT processor [3] includes the smallest number of non-trivial multiplications, which are the most complex operations in the FFT processor; therefore it is generally used for the SISO-OFDM system. However, the MIMO-OFDM system with k transmitting and receiving antennas consists of k OFDM baseband processors working in parallel, and therefore k FFT processors are required. For this reason, the hardware complexity increases k times.

Recently, it has been proposed that a multi-channel radix-k multi-path delay commutator (MC-RkMDC) FFT processor [4] is the most area-efficient approach to compute k MIMO channels [5]. Since a MC-RkMDC FFT processor can process several independent data channels simultaneously with an extra commutator block, its hardware complexity is less than that of k R2^3SDF FFT processors. However, especially for $k = 4$, the RkMDC FFT processor is not optimal from the viewpoint of hardware complexity as shown in [6].

In this paper, a more area-efficient FFT processor is proposed for 4×4 MIMO-OFDM systems. With a mixed-radix algorithm, the complexity of the proposed FFT processor is reduced by 25% that of the MC-RkMDC FFT processor. The rest of this paper is organized as follows: previous studies are shown in section 2. Section 3 proposes low complexity FFT processor architecture for the MIMO-OFDM systems and section 4 deals with the design and implementation results of the proposed FFT processor. Finally, conclusions are placed in section 5.

2 Pipeline FFT processor for MIMO-OFDM systems

2.1 4-channel R2^3SDF pipeline FFT processor

The architecture of pipelined FFT processor can be classified into 3 architectures: SDF, MDC and single-path delay commutator (SDC) architectures [7]. Among these architectures, it is known that SDF architecture is best suitable for the general OFDM systems in aspects of hardware complexity. Also,

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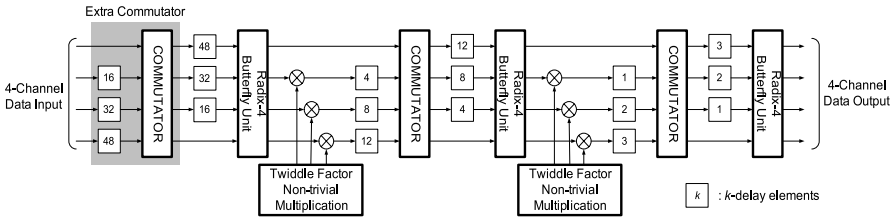

Fig. 1. Block diagram of the MC-RkMDC FFT processor ($k = 4$, $N = 64$)

radix-2^3 algorithm includes the number of minimal non-trivial multiplications. In this reason, R2^3SDF pipelined FFT processor is best approach to compute FFT processing of single-channel OFDM systems because it requires less hardware resources and single I/O path which is suitable for SISO-OFDM systems. However, in case of MIMO-OFDM systems, it is not best approach to compute FFT processing. Due to single I/O path and low throughput of SDF architecture, several SDF FFT processors must be used to implement a MIMO-OFDM system. For example, four R2^3SDF FFT processors are required to compute FFT processing in 4-channel MIMO-OFDM systems. Therefore, the hardware complexity of FFT processor in the MIMO-OFDM systems increases linearly as the number of MIMO channels.

2.2 4-channel R4MDC pipeline FFT processor

In contrast to SDF architecture, MDC architecture has multiple I/O paths. Therefore, a 4-channel R4MDC FFT processor can process four independent data channels simultaneously. Fig. 1 shows the block diagram of the 4-channel R4MDC FFT processor. Unlike a conventional R4MDC FFT processor, a 4-channel R4MDC FFT processor requires an extra commutator, which reorganizes four input data streams to make them transformed simultaneously. The overhead according to this extra commtator is very small because it can be implemented by simple delay elements and a multiplexer. However, R4MDC architecture is not optimal architecture in a viewpoint of hardware complexity. As stated, the complexity of the RkMDC FFT processor can be further reduced by using a mixed-radix algorithm [6].

3 Proposed multi-channel mixed-radix MDC FFT processor for MIMO-OFDM systems

In [6], the authors proposed the single channel mixed-radix MDC (SC-MRMDC) pipeline FFT processor, which is more area-efficient than the RkMDC FFT processor with a reduced number of non-trivial multiplications. Similar to MC-MRMDC architecture, SC-MRMDC architecture can be modified to support k MIMO channels simultaneously with an extra commutator because it is also based on MDC pipeline architecture. Since the SC-MRMDC FFT processor has fewer non-trivial multiplications than the SC-RkMDC FFT processor, the proposed MC-MRMDC FFT processor also includes fewer non-trivial multiplications than the MC-RkMDC FFT proces-

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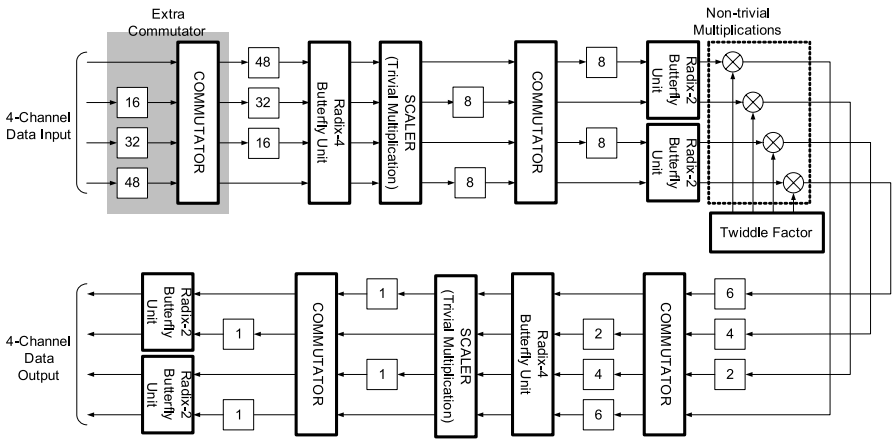

Fig. 2. Block diagram of the MC-MRMDC FFT processor ($k = 4$, $N = 64$)

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Fig. 2 depicts the block diagram of the proposed MC-MRMDC FFT processor for $k = 4$ and $N = 64$. As shown in Figs. 1 and 2, the MC-R4MDC FFT processor has 6 non-trivial multiplications, while the MC-MRMDC FFT processor has 4 non-trivial multiplications. Table I shows the hardware requirements of various FFT processors to support k MIMO channels. The constant T denotes the number of adders required to implement trivial multiplications and $\lceil a \rceil$ stands for the smallest integer greater than a. As depicted in Table I, for $k = 4$ and $N = 64$, the proposed FFT processor saves 2 non-trivial multiplications compared with the MC-R4MDC FFT processor and 76 complex adders compared with the MC-R2^{3}SDF FFT processor, respectively.

Table I. FFT hardware requirements comparison for k MIMO channels

	Number of processors (P)	Complex-multipliers/P	Complex-Adders/P	Memory size/P
R2SDF	k	$\log_2 N - 1$	$2\log_2 N$	$N - 1$
R4SDF	k	$\log_4 N - 1$	$8\log_4 N$	$N - 1$
R4SDC	k	$\log_4 N - 1$	$3\log_4 N$	$2N - 2$
R2^{2}SDF	k	$\log_2 N - 1$	$4\log_4 N$	$N - 1$
R2^{3}SDF	k	$2(\log_8 N - 1)$	$(62T)\log_8 N$	$N - 1$
R2MDC	$\lceil k/2 \rceil$	$\log_2 N - 2$	$2\log_2 N$	$3N/2 - 2$
R4MDC	$\lceil k/4 \rceil$	$3(\log_4 N - 1)$	$8\log_4 N$	$5N/2 - 4$
MRMDC	$\lceil k/4 \rceil$	$4(\log_8 N - 1)$	$(12 + 3T)\log_8 N$	$5N/2 - 4$

4 Implementation results

The proposed 4-channel MRMDC FFT processor is simulated by using high-level programming language and 10-bit fixed-point word length is chosen to

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trade-off between hardware complexity and quantization noise. Then, the proposed FFT processor is designed using hardware description language (HDL) and synthesized with 0.18 um standard CMOS process cell library. The total logic gate count for this FFT processor is about 52 K. In order to verify the efficiency of the proposed architecture, FFT processors with 4-channel R2^{3}SDF architecture and 4-channel R4MDC architecture are also designed and synthesized with same process cell library. The total gate counts of 4-channel R2^{3}SDF FFT processor and 4-channel R4MDC FFT processor are about 140 K and 69 K, respectively. From the comparison of the implemented results, it is observed that the proposed FFT processor reduces the number of logic gates by 64% and 25% compared with a 4-channel R2^{3}SDF FFT processor and a 4-channel R4MDC FFT processor, respectively.

5 Conclusion

A low complexity pipeline FFT processor supporting 4×4 MIMO-OFDM systems is proposed in this paper. Based on the mixed-radix algorithm and multi-channel MDC architecture, the proposed FFT processor reduces the number of logic gates by 25% compared with a 4-channel R4MDC FFT processor known as the most area-efficient FFT processor for MIMO-OFDM systems. Therefore, the proposed FFT processor would contribute to low complexity implementation of 4×4 MIMO-OFDM systems because the 4-channel FFT processor is one of the largest modules in those systems, in which low complexity design is paramount.

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