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Design and FPGA implementation of digital pulse compression for HF chirp radar based on modified orthogonal transformation

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Abstract: The paper presents a digital pulse compression approach for high frequency (HF) chirp radar. The emphasis is to accomplish echo signal de-chirp operation by modified orthogonal transformation on field programmable gates array (FPGA) chip. This approach has been developed for an all-digital receiver platform which is directly radio frequency (RF) band-pass sampling, compared with the traditional analog receiver or intermediate frequency (IF) receiver, it has an easy hardware structure closing to a "soft" radar mode. The system closed-loop test shows the correctness and rationality of the design, meeting the demand of engineering application.

Keywords: digital pulse compression, orthogonal transformation, all-digital receiver, digital down converter, field programmable gates array

Classification: Electron devices, circuits, and systems

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1 Introduction

For chirp (linear FM, LFM) radar, there are many pulse compression methods, in which the most popular techniques are matched filtering and de-chirp demodulation combined with Fast Fourier transform (FFT) techniques [1, 2, 3, 4, 5, 6]. The matched filter may be implemented by using a digital convolution in time-domain or frequency-domain [1], but the main drawback of matched filtering is the complexity for hardware implementations when the time-bandwidth product of the chirp signal is large [7]. The second method is equivalent to matched filtering, for the traditional superheterodyne receiver architecture, whereas the procedure is multiplying the echo radio frequency (RF) signal with the LO (local oscillator) signal, which has the same sweep slope of the transmitted RF signal and translating the echo signal to intermediate frequency (IF). Then through ADC (Analog-Digital Converter), DDC (digital down converter) and FFT processing, we can get the range compression signal as wanted. So this technique is directly IF band-pass sampling which contains at least one analog mixer structure, but considering the concept of SDR (Software Defined Radio) [8, 9], the trends is to push the analog/digital boundary as close to the antenna as possible, thus reducing the need of large and costly analog components. This means that we prefer practical directly digitizing RF signal than digitizing IF signal.

In this work, we proposed a digital pulse compression method derivation from the second method referred above based on an all-digital receiver platform for HF chirp radar. The approach is directly digitizing the RF echo signal and then transports the discrete values to FPGA chips for digital pulse compression processing. Compared to the IF sampling mode, the mixer signal is not analog LO signal but the discrete values of the transmitted RF signal. This processing procedure is not only finishing the de-chirp demodulation but also implements the digital orthogonal transformation to form in-phase and quadrature (I/Q) signals. And then through the decimation

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filters we can get the baseband I/Q signals to accomplish FFT operation. So the advantages of the proposed method are as follows:

① it obtains more information by directly RF sampling;

② the architecture reduces system complexity with less analog devices;

③ the digital orthogonal transformation processing owns less amplitude error and phase orthogonality error;

④ the decimation stage greatly reduces the sampling data and is suitable for the chirp signal when the time-bandwidth product is large.

In the following, section 2 presents the signal processing procedure for the chirp signal waveform which contains a digital pulse compression stage and a decimation filter stage to obtain the orthogonal baseband signals; section 3 describes the receiver platform and FPGA implementations of the algorithm mentioned in section 2; in section 4, the system experiment results of the radar receiver are given, and in section 5 our conclusions.

2 Signal processing procedure for RF sampling receiver

2.1 Digital orthogonal transformation

Denote the sampling frequency is f_s, carrier frequency is f_c and the receiving echo signal is $x(t) = \cos[2\pi f_c t + \varphi(t)]$, after digitalizing by ADC, it can be expressed as follows:

$$x(n) = \cos[2\pi f_c n/f_s + \varphi(n/f_s)], \tag{1}$$

Where $\varphi(n/f_s)$ is the baseband phase information as we wanted, for the purpose we can multiplying $x(n)$ with sequence of complex numbers$e^{-j2\pi n f_c/f_s}$, and then following by a low-pass filters to obtain the baseband signal $x'(n)$:

$$\begin{aligned} x'(n) &= L\{x(n)e^{-j2\pi n f_c/f_s}\} \\ &\approx 1/2\{\cos[\varphi(n/f_s)]\} + j/2\{\sin[\varphi(n/f_s)]\} \\ &= I(n) + j \cdot Q(n). \end{aligned} \tag{2}$$

In equation (2), $L\{\bullet\}$ represents the low-pass digital filtering processing, $I(n)$ represents the in-phase signal of $x'(n)$ and $Q(n)$ represents the quadrature signal. The above processing is called digital orthogonal transformation or digital orthogonal demodulation.

2.2 2.2 Pulse compression processing based on modified digital orthogonal transformation for chirp signal

As depicted in Section 2.1, the digital orthogonal transformation is widely used in IF sampling receiver for data demodulation. In order to find a suitable method for RF sampling receiver of chirp radar system, we can deduce a procedure from the echo signal form.

Denote the LFM signal in a transmitted period as follows:

$$S(t) = \begin{cases} \cos[2\pi(f_0 + \frac{\alpha t}{2})t], t \in [0, T] \\ 0, t \in (T, T_s] \end{cases}, \tag{3}$$

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where f_0 is carrier frequency, $\alpha = B/T$ is sweep slope and is constant as usual, B is sweep bandwidth and T is sweep time (pulse width of LFM), T_s is one transmitted pulse period.

Let's suppose that the backscatter echo has a delay time of τ and the amplitude attenuation factor is A, then the echo can be denoted as:

$$\begin{aligned} &\mathrm{S_R}(t) = AS(t-\tau) \\ &= A\cos[2\pi f_0(t-\tau) + \pi\alpha(t-\tau)^2]. \end{aligned} \tag{4}$$

Here we will process the RF echo signal in all-digital method. The echo signal $S_R(t)$ is converted to discrete values by ADC with sample frequency of f_s after low-noise amplifying and filtering, and then the echo signal is turned to:

$$\begin{aligned} &\mathrm{S_R}(n) = AS(n/f_s - \tau) \\ &= A\cos[2\pi f_0(n/f_s - \tau) + \pi\alpha(n/f_s - \tau)^2]. \\ &= A\cos\left[2\pi\left(f_0 + \tfrac{\alpha n}{2f_s}\right)n/f_s + (-2\pi f_0\tau + \pi\alpha\tau^2 - \pi\alpha\tau n/f_s)\right] \\ &= A\cos\left[2\pi\left(f_0 + \tfrac{\alpha n}{2f_s}\right)n/f_s + \varphi(n/f_s)\right], \end{aligned} \tag{5}$$

In equation (5) $\varphi(n/f_s) = -2\pi f_0\tau + \pi\alpha\tau^2 - \pi\alpha\tau n/f_s$, compared equation (5) with equation (1), we can see that $\varphi(n/f_s)$ is the baseband signal as we wanted, but the carrier frequency is different, which the first is f_c and the second is $f_0 + \frac{\alpha n}{2f_s}$. To obtain the baseband signal $\varphi(n/f_s)$, we should modified the complex sequence $e^{-j2\pi n f_c/f_s}$ to $e^{-j2\pi n(f_0+n\alpha/2/f_s)/f_s}$, and the following processing is as the same as digital orthogonal transformation. Then the output echo signal is as follows:

$$\begin{aligned} &S'_R(n) = L\{S_R(n)e^{-j2\pi n(f_0+n\alpha/2/f_s)/f_s}\} \\ &= A/2\{\cos[\varphi(n/f_s)] + jA/2\{\sin[\varphi(n/f_s)] \end{aligned} \tag{6}$$

From equation (6), we can get the baseband signal $S'_R(n)$. Compared with the analog processing of orthogonal transformation, the amplitude error and phase orthogonality error of I/Q signals are smaller. The orthogonal transformation is implemented on FPGA chips.

2.3 Data decimation processing

Suppose the maximum detection range of radar is$R_{\max}$, after orthogonal transformation and low-pass filtering processing, the real bandwidth of the I/Q signal is $\Delta B = 2R_{\max} * \alpha/c$, in the HF ground-wave radar application, $\Delta B \ll B$, and according to Nyquist sampling theorem, the sample rate $f_s \geq 2B$ (in our system f_s is 40 MHz, B is 30 kHz or 60 kHz). This will result in redundant data which will be a heavy burden for the following data transferring and data real-time processing. So decreasing data rate becomes necessary and beneficial to data transfer and by attenuating the unwanted frequencies the signal can be re-sampled at a lower rate. Depending on the selected frequency range, sample rate, and desired quality, different filter combinations can be used. The decimation filters stages in our system as shown in Figure 2 (b).

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Through the decimation processing stage, we can obtain the orthogonal baseband I/Q signal $I(n)$ and $Q(n)$, then through FFT transformation using computer we can get the Range spectrum which is equivalent to matched filter processing of pulse compression. The method above also is suitable for PMICW or FMICW waveforms which are widely used in HF ground-wave radars [10].

3 Hardware platform and FPGA implementation

According to the radar design requirements, the system is an 8 channel of coherent architecture. The receiver platform is depicted in Fig. 1.

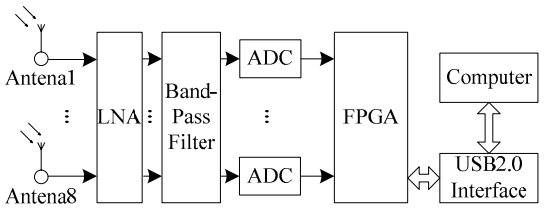

Fig. 1. Receiver platform without mixer architecture, the pulse compression and data decimation processing finished by FPGA EP2C70F896C8, whereas the FFT processing by the computer.

(a) As shown in equation (6), the pulse compression processing needs to generate two orthogonal digital signals. Here we will use direct digital synthesis (DDS) algorithm to implement the NCO (Numerically-Controlled Oscillation) module and the block diagram is shown in Fig. 2 (a).

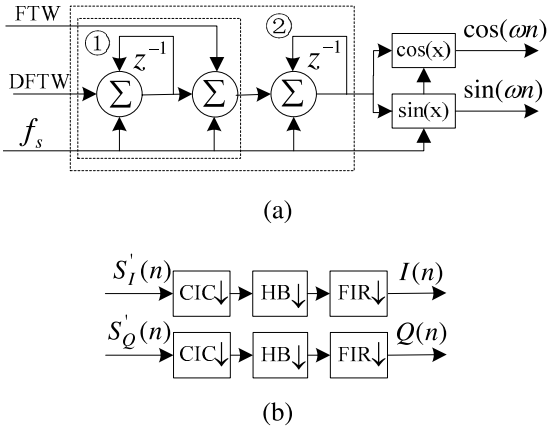

Fig. 2. NCO block diagram and Decimation filters stage, (a) ① frequency accumulator; ② phase accumulator. FTW is frequency control word and DFTW is delta frequency word. And the sin(x) and cos(x) are the sine and cosine waveforms look-up tables in 16-bit fixed-point mode, (b) CIC (Cascaded Integrator Comb), HB (Half Band) and FIR (Finite Impulse Response) decimation filters.

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(b) As shown in Figure 2 (b), CIC decimator is handling the high sample rate by using only additions and no multiplications, but 1-stage CIC filter has bad side-lobe suppression, so we can use 5-stage CIC decimator with decimation factor 100. At the same time the HB filter with decimation factor 2 and FIR filter with decimation factor 4, whereas the total decimation factor is 100*2*4=800, with the sample frequency is 40 MHz, the final data of output per channel is 50 kHz with I/Q signals in 16-bit fixed point.

(c) Besides the pulse compression processing, the FPGA also accomplishes the system synchronization control and data transmission with the radar control computer by USB2.0 interface. So the final compilation reports (by Quartus software ver7.1, FPGA: EP2C70F896C8) as follows:

① total logical elements: 26 843 / 68 416 (19%);
② total memory bits: 65 536 / 1 152 000 (6%);
③ Embedded Multiplier 9-bits elements: 288 / 300 (96%);
④ total pins: 150 / 622 (24%).

4 Experiments and results

4.1 No delay and zero-Doppler test

Experiment platform: as shown in Fig. 3 (a), the RF frequency of DDS signal source is 10.654 MHz; the carrier frequency of NCO is 10.65 MHz; bandwidth of both signals above is 30 kHz; the system clock is from an OXCO of 40 MHz; the output of DDS is 0 dBm, the attenuator is −81 dB; the output sample rate per channel of the decimation stage is 50 kHz.

The results shown in Fig. 3, Figure 3 (b) shows channel 1 I/Q baseband signal $I(n)$ and $Q(n)$ discrete series (sampling points k from 10 to 80), Figure 3 (c) shows the output pulse compression spectrum of channel 1 using

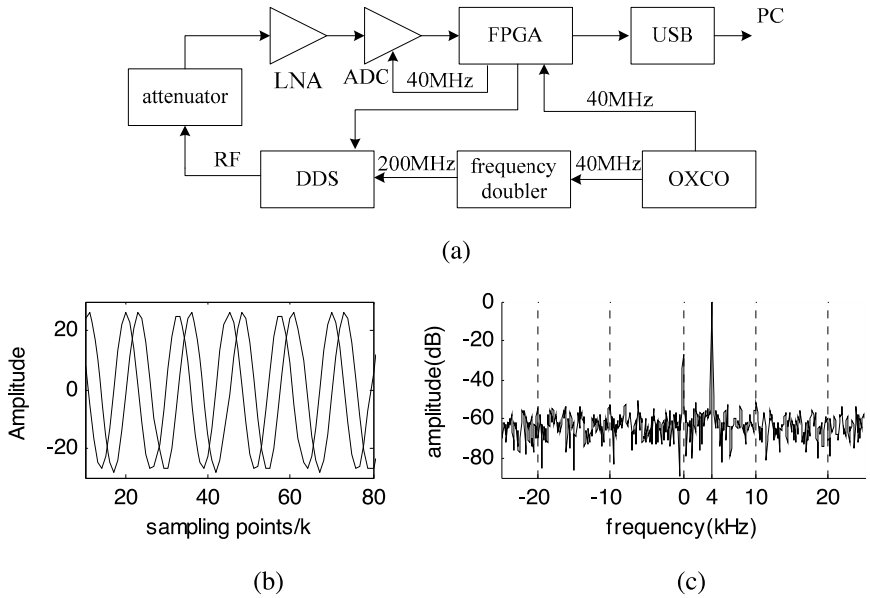

Fig. 3. Results of two experiments, (a) experiment platform, (b) time-domain I/Q baseband signal, (c) the output pulse compression spectrum.

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hamming window to reduce the side-lobes.

5 Conclusion

In this paper we introduce a digital pulse compression approach suitable for an all-digital HF radar receiver architecture. The pulse compression method finishes the echo signal de-chirped demodulation by orthogonal transformation, and through decimation and FFT processing to obtain the range compression signal. Whereas the realization based on the FPGA chips makes it easy to change the radar working parameters to adapt to different situations which following the concept of SDR.

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