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A novel high-precision DAC utilizing tribonacci series

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Abstract: A novel Digital-to-Analog Converter (DAC) utilizing Tribonacci Series is presented in this paper. The ratios of successive weights are smaller than those of binary DAC and larger than those of unary DAC. The proposed DAC has the features that the DNL can be superior to that of a binary DAC and the INL can be superior to that of a unary DAC. In the proposed DAC on a 0.18 μm CMOS process, the number of logic gates can be achieved an around 52% reduction compared to that of the unary DAC.

Keywords: digital-to-analog converter, Tribonacci series, DNL, INL

Classification: Integrated circuits

References

[1] A. R. Bugeja and B.-S. Song, "A Self-Trimming 14-b 100 MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1841–1852, 2000.

[2] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. 21, p. 1057, 2003.

[3] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, 1998.

[4] K. Hokazono, D. Kanemoto, R. Pokharel, A. Tomar, H. Kanaya, and K. Yoshida, "A Low-Glitch and Small-Logic-Area Fibonacci Series DAC," *Proc. International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1–4, Aug. 2011.

[5] M. Feinberg, "Fibonacci-Tribonacci," *The Fibonacci Quarterly*, vol. 1, no. 3, pp. 71–74, 1963.

1 Introduction

In many signal processing and telecommunication applications, the digital-to-analog converter (DAC) is a critical building block limiting the accuracy of the overall systems. A current-steering DAC architecture, in which an analog part is composed of current sources, is almost exclusively used when appli-

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cations require high speed and high resolution such as mobile cellular networks [1]. A current-steering DAC has static problems. It is well known that the static problems are mainly from mismatches among the current sources. Therefore, to realize high static performance, large size of transistors should be used for current sources in analog part [2]. In general, silicon die area allocated to DAC is limited from a LSI cost viewpoint. Therefore, the analog part of the DAC becomes small; it leads to decrease static performance.

In order to shrink logic die area and expand analog part, once, we proposed a Fibonacci Series DAC utilizing Fibonacci Series as weight for DAC cells [4]. However, Fibonacci Series DAC has the fatal disadvantage that the precision may be worse compared to conventional DACs, because each DAC cell weight should utilize offset values in order to achieve large output range such as a 6-bit. The offset, which is also composed of current mirror, does not contribute DAC's INL and DNL performance improving. Therefore a new DAC architecture which does not require offset value for each DAC cell weight is desired.

This paper presents a novel high-precision DAC with Tribonacci Series. The Tribonacci Series DAC has the features that the DNL can be superior to that of a binary DAC and the INL can be superior to that of a unary DAC. In section II, the architecture of DAC with Tribonacci Series DAC is described. In section III, the comparison with DACs is presented.

2 Tribonacci Series DAC

The Tribonacci Series is given as [5],

$$w_{i+3} = w_i + w_{i+1} + w_{i+2} \quad (i \geq 0)$$
$$(w_0,\ w_1,\ w_2\text{: Initial Conditions}) \tag{1}$$

where w_i shows i-th number of Tribonacci Series. Each number of Tribonacci Series is the sum of the three preceding numbers. The each value of Tribonacci Series depends on initial condition values, w_0, w_1 and w_2. The proposed DAC utilizes Tribonacci Series as weight function and some of these weights are selected to express desired output signals. The successive ratios of Tribonacci Series are around Tribonacci constant (i.e. 1.839) whose value is between those of unary DAC (i.e. 1) and those of binary DAC (i.e. 2).

The Tribonacci Series DAC has two features by utilizing such successive ratio. One is that the number of DAC cells can be smaller than unary DAC's. Thus the small number of cells leads to reduce the number of logic gates in decoder circuits, because the decoder circuit area is proportional to control signal numbers. Therefore area of analog part can be expanded and it means large transistor can be allocated for current mirrors, and INL/DNL can be improved. The other feature is that DNL can be improved against binary DAC's. Because, in Tribonacci Series DAC, changing number of active cells is smaller than those of binary DAC at one code transition and all current cells changing at same time are not required; otherwise, in binary DAC, all cell changing appeared at mid-code transition, and the worst DNL is happened.

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In this paper, we explain how to implement a 6-bit Tribonacci Series DAC. Basically, to express 6-bit DAC, the Tribonacci Series DAC has to use over 7 cells. Designing initial condition is important because the series which is utilized for DAC cells weight is changed by initial conditions. In this design, by using computer calculation, we found initial condition "$w_0 = 1$, $w_1 = 3$, $w_2 = 1$," which realize that the maximum weight of DAC is smallest and the sum of weight is $2^n - 1$ (n: number of bit). The proposed weight of the DAC is shown in Table I (a). The output of the DAC can express 6-bit resolution by combination of 7 cells ($w_0 - w_6$).

Table I. (a) Weight of Tribonacci Series DAC. (b) Decoding table of 6-bit DAC.

(a)

i	0	1	2	3	4	5	6
w_i	1	3	1	5	9	15	29

(b)

Digital input	w_k							Analog output
	I_{LSB}	$3I_{LSB}$	I_{LSB}	$5I_{LSB}$	$9I_{LSB}$	$15I_{LSB}$	$29I_{LSB}$	
000000	0	0	0	0	0	0	0	**0**
000001	1	0	0	0	0	0	0	I_{LSB}
000010	1	0	1	0	0	0	0	$2I_{LSB}$
:	:	:	:	:	:	:	:	:
111110	0	1	1	1	1	1	1	$62I_{LSB}$
111111	1	1	1	1	1	1	1	$63I_{LSB}$

Table I (b) shows the operation of the decoder. Input digital data is converted to decoded signals in order to control cells weighted by Tribonacci series DAC. The table indicates that each weighted current sources are summed and the output signal can be express from 0 to 63level. The decoder table is designed in order to reduce the number of changing cells at each step.

3 Comparison with DACs

In this section, we explain the advantages of the proposed DAC against conventional DACs. First, we discuss the DNL and INL of these DACs. The maximum RMS of DNL and INL are proportional to σ, and they are given as [3],

$$DNL_{max} = \sqrt{S_s}\sigma$$
$$INL_{max} = \frac{1}{2}\sqrt{S_{cs}}\sigma \quad (2)$$

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where σ is standard deviation of mismatches between each unit current mirror transistors. In equation (2), the coefficient 1/2 comes from the fact that the INL curve was fit to zero at both ends of the curve. In this paper, S_s expresses the largest number of turned cells (ON→OFF or OFF→ON) for a ramp input code and S_{cs} shows the number of current mirror transistors in DAC. For example, it is well known that DNL_{max} of binary DAC is happened at mid-code transition and S_s is a number of all unit current sources. On the other hand, the INL_{max} is proportional to the number of current sources. In binary DAC, $S_s = 63$ because all unit current mirrors are changed at mid-code, and in unary DAC, $S_s = 1$ because only one unit current mirror is changed. In proposed Tribonacci Series DAC utilizing our designed decoding table, the number of S_s is 59 because the number of changing unit current mirrors is largest in the case that 7th cell (29 current sources) and 1st cell (1 current source) turn ON, and 6th cell (15 current sources), 5th cell (9 current sources) and 4th cell (5 current sources) turn OFF. Therefore DNL of Tribonacci series DAC is superior to that of binary DAC.

On the other hand, in each DAC, the number of total current sources is same; $S_{cs} = 63$. Therefore the coefficient of each DAC's INL is same. Table II shows the detail of DAC's DNL and INL, where the standard deviations of the unit cells in each DAC are given as σ_{b} (Binary), σ_{f} (Fibonacci [4]), σ_{t} (Tribonacci) and σ_{u} (Unary). In Table II, the INL of Fibonacci Series DAC is not described, because in Fibonacci Series DAC the INL does not follow the equation (2) due to the offset. Table II indicates that Tribonacci Series DAC's INL and DNL performance can be improved compared to that of Fibonacci Series DAC.

Table II. Comparison with DACs.

	Binary	Fibonacci[4]	Tribonacci	Unary
Number of current sources(S_{cs})	63	116	63	63
Number of turned cells(S_s)	63	79	59	1
Number of Logic gates(S_{logic})	0	266	222	459
DNL [LSB]	$\sqrt{63}\sigma_b$	$\sqrt{79}\sigma_f$	$\sqrt{59}\sigma_t$	σ_u
INL [LSB]	$\frac{1}{2}\sqrt{63}\sigma_b$	-	$\frac{1}{2}\sqrt{63}\sigma_t$	$\frac{1}{2}\sqrt{63}\sigma_u$

Next, we discuss the standard variance of each DAC in order to compare of INL more detail. In this paper we assume that the total available area for DAC is given from the viewpoint of LSI cost and DAC circuit is consisted of analog current sources part and digital logic circuit part, thus all of the DAC circuit area A can be given by,

$$A = A_{unit} \cdot S_{cs} + A_{st} \cdot S_{log\ ic} \tag{3}$$

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where A_{unit} and A_{st} show the active area of an unit current mirror circuit in analog part and an average size of standard cells in decoder, respectively. S_{logic} indicates the number of logic gates in decoder circuit. Here, the variance coming from the mismatch between each transistors of the unit cell (σ^2) is inverse proportional to its area [3], and it is given as,

$$\sigma^2 \propto \frac{1}{A_{unit}} = \frac{S_{cs}}{A - A_{st} \cdot S_{log\ ic}} \tag{4}$$

In conventional design, σ_{t} must be smaller than σ_{u} because logic number of Tribonacci Series DAC is smaller than unary DAC. Therefore INL of Tribonacci Series DAC is superior to that of unary DAC because S_{logic} of Tribonacci Series DAC is smaller than that of unary DAC.

In this paper A_{st} is assumed to $1.0 \times 10^{-4}\,\mathrm{mm}^2$ and process variation coefficient, which was found by CMOS 0.18 μm process design kit, are used. We can estimate DAC area by relationship (equation (3) and Table II) when desired INL is defined. Fig. 1 (a) shows DAC's INL vs. area reduction ratio (Tribonacci Series DAC/unary DAC). The DAC's area is calculated by equation (2) and (4), and it is given as,

$$A = A_{st} \cdot S_{log\ ic} + \frac{k \cdot {S_{cs}}^2}{4 \cdot {INL_{max}}^2} \tag{5}$$

where k is the process variation coefficient. This figure shows that in higher INL performance, the area reduction ratio becomes small because the logic area is small against the DAC's area, and in lower INL performance, the area reduction ratio settles the reduction ratio of the number of logic gates; 52%. From this figure, we know that area of Tribonacci Series DAC can be reduced compared to unary DAC's area. We can reduce die area about 51% compared to unary DAC utilizing INL = 0.1 [LSB] if we design DAC utilizing Tribonacci Series DAC. This means that Tribonacci Series DAC can realize high INL performance compared to unary DAC under same silicon die area. Fig. 1 (b) shows DAC's area vs. INL reduction ratio (Tribonacci Series DAC/unary DAC). This figure shows that in large size DAC, the INL reduction ratio becomes small, and in the case DAC's area is 0.5 mm^2, the INL of Tribonacci Series DAC can be reduced by only 3% compared to that of unary DAC.

In Table II, the parameters of each DAC are summarized and the comparison of layout areas is shown in Fig. 1 (c). The table shows that in Tribonacci Series DAC the number of logic gates in decoder can be achieved an around 52% reduction and Fig. 1 (c) shows that logic area in Tribonacci Series DAC has around 46% reduction compared to that of unary DAC.

4 Conclusion

We proposed a novel DAC utilizing Tribonacci Series in this paper. The ratios of DAC's successive weights are smaller than those of binary DAC and larger than those of unary DAC. The proposed DAC has the features that the DNL can be superior to that of a binary DAC and the INL can be superior to that of a unary DAC. In the proposed DAC in 0.18 μm CMOS

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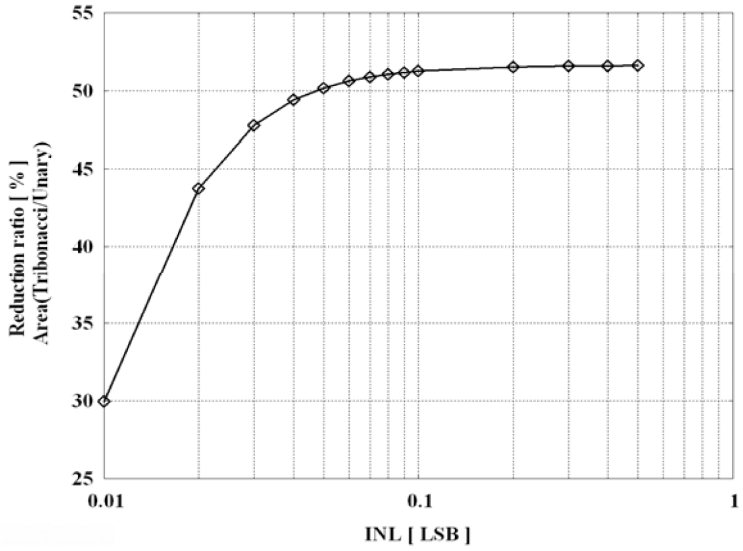
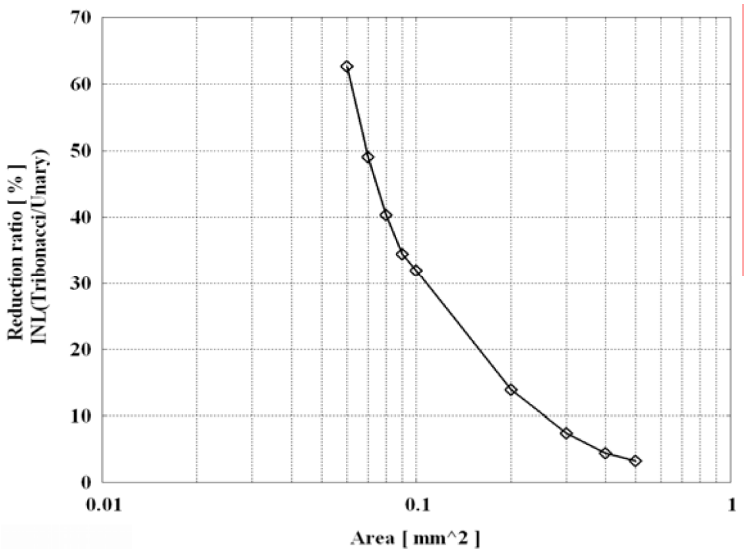
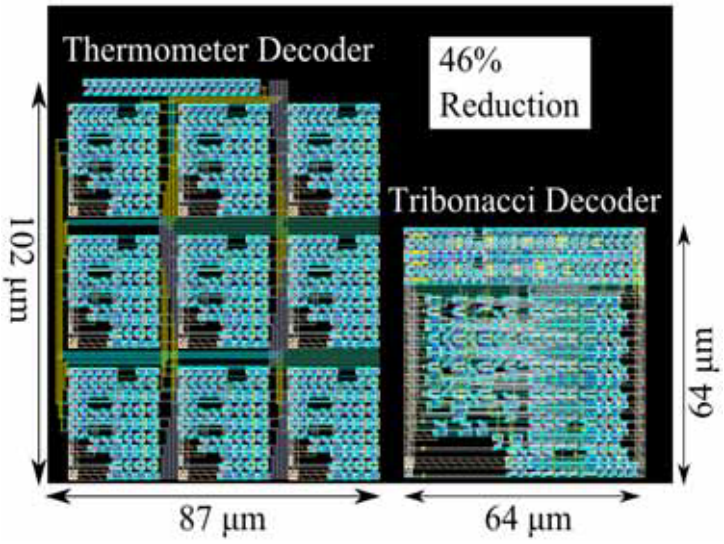


(a) INL vs. area reduction ratio (Tribonacci Series DAC/ Unary DAC).



(b) DAC's area vs. INL reduction ratio (Tribonacci Series DAC/ Unary DAC).



(c) Comparison of layouts with Thermometer decoder and Tribonacci decoder.

Fig. 1. Simulation results of each DAC.

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process, the number of logic gates can be achieved an around 52% reduction compared to that of the unary DAC.

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