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Stacked-FET linear SOI CMOS SPDT antenna switch with input P1dB greater than 40 dBm

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Abstract: The power handling capability is the most stringent specification for antenna switches, and this is dominated by a significant amount of leakage current of off-state FETs. For achieving maximum power handling capability of antenna switches, new DC I-V (FFI-V) characterization method to characterize RF P_{1dB} point of off-state FETs is proposed and experimental study on optimum DC gate and body bias is performed based on proposed FFI-V method. Using R_{on} and C_{off} of minimum channel length MOSFETs at aforementioned optimum DC bias point, antenna switch design methodology for maximum power handling capability and minimum insertion loss is established. The designed SOI CMOS SPDT antenna switch integrated with switch controller shows insertion loss less than 0.5 dB and input P_{1dB} greater than +40 dBm.

Keywords: antenna switch, leakage current, power handling capability, SOI CMOS, SPDT switch

Classification: Integrated circuits

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1 Introduction

High power antenna switches are key building blocks for the RF front-end of the time division duplexing (TDD) wireless systems and multi-band multi-standard radios. The most stringent specification for high power antenna switches is the power handling capability. It should be capable of handling high power signal to +40 dBm under worst case of antenna impedance mismatch. This means that the 1 dB compression point (P_{1dB}) of the antenna switch should be at least greater than +40 dBm. On the other hand, among various process technologies, silicon-on-insulator (SOI) CMOS process has become promising technology for high power antenna switch applications because it provides extremely low substrate loss and near-perfect isolation by thick buried oxide layer ($> 1\,\mu$m) and high resistivity handle wafer (> 1 kohm-cm) while maintaining moderately low cost, high integration capability and good product yield. The insufficient isolation among transistors in stacked-FETs makes unequal voltage distribution and turns few transistors weakly on, which severely limits the power handling capability of the antenna switch. This is why bulk CMOS has not been widely used for high power antenna switches in spite of showing low cost and excellent integration capability.

Many researches related with SOI CMOS antenna switches have been studied. Most of them focus on severe trade-off between on-resistance (R_{on}) and off-capacitance (C_{off}), and thus small signal properties such as insertion loss and isolation have been well analyzed. However, unfortunately, analytical study on power handling capability and gain compression has not been performed. In this paper, firstly, new DC characterization method (Float FET I-V method) to find correlation between DC I-V measurement and RF P_{1dB} measurement is proposed for rapid evaluation of antenna switch power handling capability. Based on FFI-V method, optimum design methodology

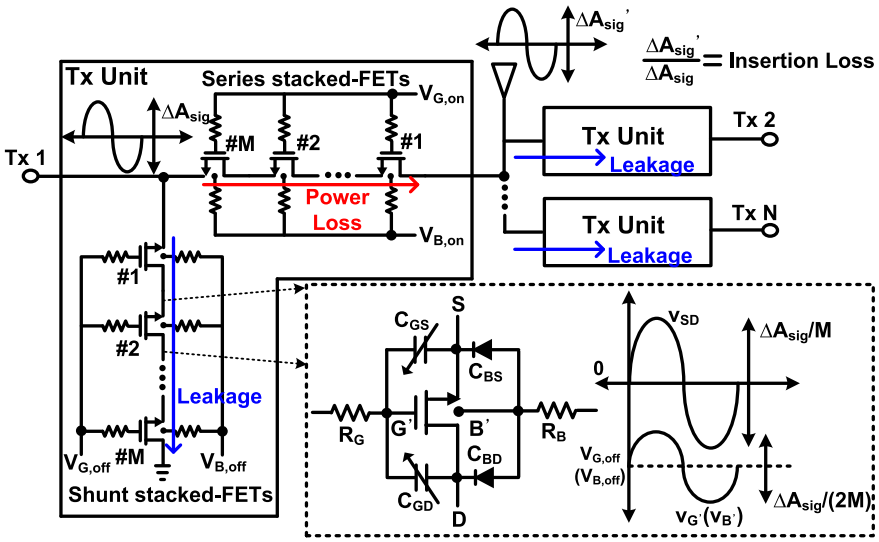

Fig. 1. General high power SPnT antenna switch structure. The voltage waveform is when the Tx 1 is enabled.

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for maximum power handling capability and minimum insertion loss is established, and high power SOI CMOS SPDT antenna switch is designed with its controller part.

2 Overview of SOI CMOS antenna switches

Fig. 1 shows general high power SPnT (single-pole n-throw) antenna switch structure. In Tx unit, the shunt branch is added to improve isolation among Tx ports. For both series and shunt branches, conventional state-of-the-art techniques such as floating gate and body method [1], negative biasing [2], and stacked-FETs technique [3] are adopted to improve power handling capability and minimize insertion loss. These are for keeping on-state FETs turn-on state and off-state FETs turn-off state, respectively, irrespective of applied signal power.

The dominant reason to limit the power handling capability of the antenna switch is undesirable channel formation (leakage current) in off-state FETs in the event of a large signal input. Like other RF circuits, this limitation of the power handling capability appears as gain compression, which is expressed as P_{1dB} point. In unit off-state FET of Fig. 1, if floating gate and body resistors R_G and R_B are much greater than the impedance level of C_{GS}, C_{GD}, C_{BS}, and C_{BD}, the voltage swing level at internal gate (G') and body (B') nodes becomes mean value of voltage swing at drain and source nodes. Therefore, maximum allowed voltage swing between source and drain ($v_{SD}|_{max}$) to keep the transistor and the junction diode turn-off state can be derived as

$$[V_{G,Off} + (v_S + v_D)/2] - v_D < V_{th} :: v_{SD}|_{max} < 2(-V_{G,Off} + V_{th}) \quad (1)$$

and

$$[V_{B,Off} + (v_S + v_D)/2] - v_D < V_{do} :: v_{SD}|_{max} < 2(-V_{B,Off} + V_{do}) \quad (2)$$

where $V_{G,Off}$ and $V_{B,Off}$ denote applied DC bias for off-state FETs, V_{th} is the threshold voltage of MOSFET, and V_{do} is the turn-on voltage of junction diode. We know that negative DC voltage via floating gate and body resistors increases the power handling capability of the antenna switch. In conclusion, maximum allowed voltage swing of stacked-FETs with M stacks becomes M times greater than that of unit FET.

However, as $V_{G,Off}$ and $V_{B,Off}$ are more negative, MOSFET breakdown by various leakage current mechanisms also limits the power handling capability of the antenna switch. Considering the increase of the number of stacks degrades the insertion loss due to the increase of on-resistance, it is important to find optimum negative bias $V_{G,Off}$ and $V_{B,Off}$ to maximize $v_{SD}|_{max}$ in (1) and (2) [4]. If possible, instead of RF measurement, DC characterization method to evaluate antenna switch power handling capability is desirable to save development time and cost.

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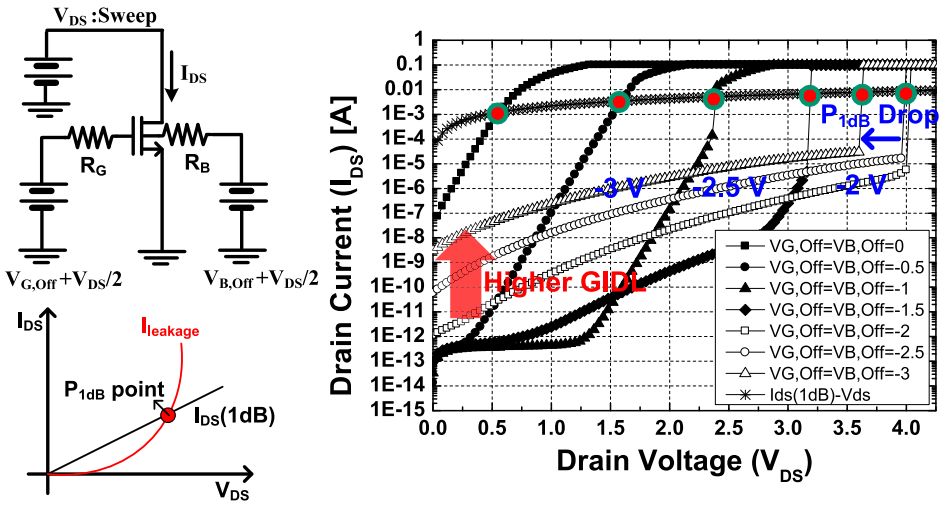

(a) (b)

Fig. 2. (a) Float FET I-V characterization method, (b) measured FFI-V characteristics of SOI MOSFET over $V_{G,off}$ and V_B, off from −3 to 0 V.

3 Float-FET IV characterization method

In unit off-state FET of Fig. 1, one half of the source-to-drain (v_{SD}) voltage swing is added to RF floated gate and body through a capacitive voltage divider. Therefore, in order to reflect antenna switch operation in conventional DC I-V characterization, an I_{DS} vs. V_{DS} sweep is performed, adding $V_{DS}/2$ to off-state DC gate and body bias $V_{G,Off}$ and $V_{B,Off}$ as shown in Fig. 2 (a). This I-V characterization is called as Float FET I-V (FFI-V) characterization method in this paper. In measured FFI-V plot, since the X-axis V_{DS} means the zero-to-peak voltage of applied RF input signal, the zero-to-peak current corresponding to 1 dB loss of the input signal can be derived as I_{DS} (1 dB) ≈ 0.109× V_{DS}/R_S, where R_S is the source impedance. Since 1 dB gain compression occurs when total leakage current flowing into the shunt path is greater than I_{DS} (1 dB), the P_{1dB} for the off-state FET can be found from measured FFI-V plot by drawing I_{DS} (1 dB)-V_{DS} curve and searching the cross point. Namely, this cross point means the P_{1dB} point for the off-state FET which is appropriate for antenna switch applications.

Fig. 2 (b) shows measured FFI-V characteristics of SOI MOSFET with minimum channel length (L_g) of 0.32 μm, channel width (W_g) of 4.8 mm, and gate oxide thickness (t_{ox}) of 52 Å over $V_{G,Off}$ and $V_{B,Off}$ from −3 to 0 V. As predicted, the negative $V_{G,Off}$ (=$V_{B,Off}$) improves the P_{1dB} of the off-state FET. For $V_{G,Off}$ from −0.5 to 0 V, the off-state leakage current mechanism is dominated by sub-threshold leakage, and thus abrupt breakdown characteristic doesn't occur. On the other hand, as the $V_{G,Off}$ is more negative, the off-state leakage current results from the GIDL (gate induced drain leakage). This GIDL current increases the body potential and the back bias effect lowers threshold voltage. This causes an exponential increase of the leakage current, and the parasitic bipolar action finally triggers the drain breakdown.

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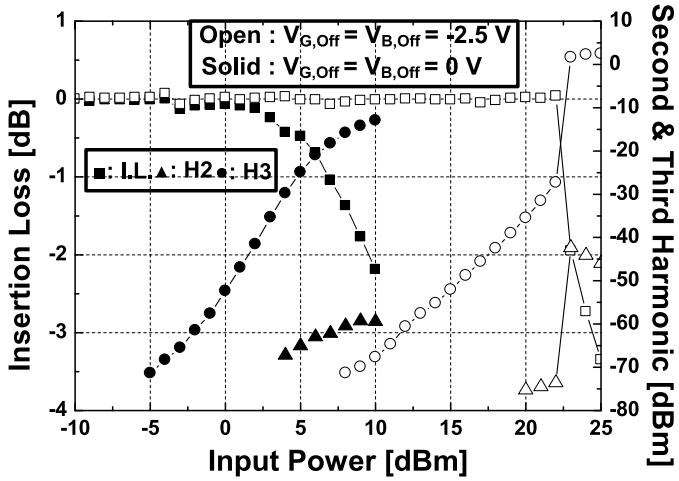

Fig. 3. P_{1dB} measurement of SOI MOSFET with L_g of 0.32 μm, W_g of 4.8 mm, and t_{ox} of 52 Å using RF single tone test.

Table I. Comparison of DC P_{1dB} from FFI-V plot and RF P_{1dB} from RF single tone test.

$V_{G,Off}$ (=$V_{B,Off}$) [V]	0	-0.5	-1	-1.5	-2	-2.5	-3
DC P_{1dB} [V]	0.65	1.65	2.5	3.25	4	4	3.6
RF P_{1dB} [V]	0.7	1.5	2.4	3.1	4	4.2	3.8

As shown in Fig. 2 (b), the negative bias voltage less than −2.5 V reduces the P_{1dB} of the off-state FET because it induces more GIDL current. Therefore, optimum negative voltage to maximize the power handling capability of the off-state FET ranges from −2 to −2.5 V. In addition, considering the P_{1dB} of unit SOI MOSFET with L_g of 0.32 μm is about 4 V, the minimum number of stacks to drive maximum RF signal level to +40 dBm (+32 V_{op}) is calculated as 8.

In order to verify FFI-V characterization method, RF single tone measurement was done for identical SOI MOSFET with L_g of 0.32 μm, W_g of 4.8 mm, and t_{ox} of 52 Å. The 2-port through-line where unit off-state FET is connected in parallel is used for RF measurement. As shown in Fig. 3, like FFI-V characteristics, harmonic distortion performances are abruptly degraded around the P_{1dB} point at $V_{G,Off} = V_{B,Off} = -2.5$ V. Table I summarizes predicted P_{1dB} from FFI-V plot (DC P_{1dB}) and measured P_{1dB} from RF single tone test (RF P_{1dB}). For comparison, the measured P_{1dB} from RF single tone test is converted into the zero-to-peak voltage at 50 ohm reference. The DC P_{1dB} from FFI-V characterization method is well matched to RF P_{1dB} from RF single tone test.

4 Optimum design for maximum power handling capability and minimum insertion loss

As previously discussed, considering maximum P_{1dB} of thick-oxide SOI

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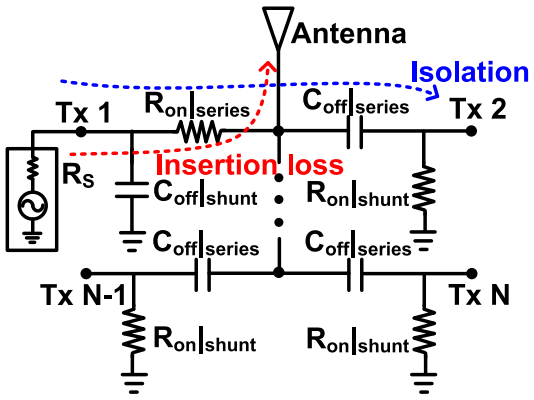

Fig. 4. Small signal equivalent circuit model composed of RC networks for general SPnT antenna switch.

MOSFET with minimum L_g of 0.32 μm is about 4 V at $V_{G,Off} = V_{B,Off} = -2.5$ V, minimum number of stacks to drive maximum RF signal level to +40 dBm is calculated as 8. In order to achieve some margin for power handling capability, the number of stacks for series and shunt stacked-FETs is set equal to 10. For reliability constraints for logic devices, DC gate and body bias $V_{G,On}$ and $V_{B,On}$ for on-state FETs are set equal to +2.5 V and ground, respectively.

For a given process technology, the product of R_{on} and C_{off} is constant. The time constant Γ is also invariant with respect to the number of stacked transistors. Indeed, when the M transistors are stacked in a switch, the overall R_{on} is M times higher while the overall C_{off} is M times lower. The constant Γ can be considered as a figure of merit (F.O.M) for the fabrication process in use, and thus minimum channel length is desirable to minimize the product of R_{on} and C_{off}. Of course, minimum channel length SOI MOSFETs should meet stringent power handling capability requirement for antenna switches. The thick-oxide SOI MOSFET with minimum L_g of 0.32 μm in adopted SOI CMOS technology shows the R_{on_unit} of 0.9 ohm-mm (@ $V_{G,On} = 2.5$ V & $V_{B,On} = 0$ V) and the C_{off_unit} of 300 fF/mm (@ $V_{G,Off} = -2.5$ V & $V_{B,Off} = -2.5$ V), and thus exhibits a value of Γ as low as 270 fsec.

In order to calculate insertion loss and isolation, the small signal equivalent circuit model composed of RC networks for general SPnT antenna switch is established as shown in Fig. 4. It is assumed that only Tx 1 is enabled and everything else is turned off. Assuming the channel width of unit FET inside of series and shunt stacked-FETs is W_{g_unit} and βW_{g_unit}, respectively, and the number of stacks is M, the overall R_{on} and C_{off} of series stacked-FETs and shunt stacked-FETs are calculated as

$$\begin{aligned} &R_{on}|_{series} \simeq M \times R_{on\_unit}/W_{g\_unit}, C_{off}|_{series} \simeq C_{off\_unit} \times W_{g\_unit}/M \\ &R_{on}|_{shunt} \simeq R_{on}|_{series}/\beta, \text{ and } C_{off}|_{shunt} \simeq C_{off}|_{series} \times \beta. \end{aligned} \quad (3)$$

Using these variables, the insertion loss from Tx 1 to antenna port and the

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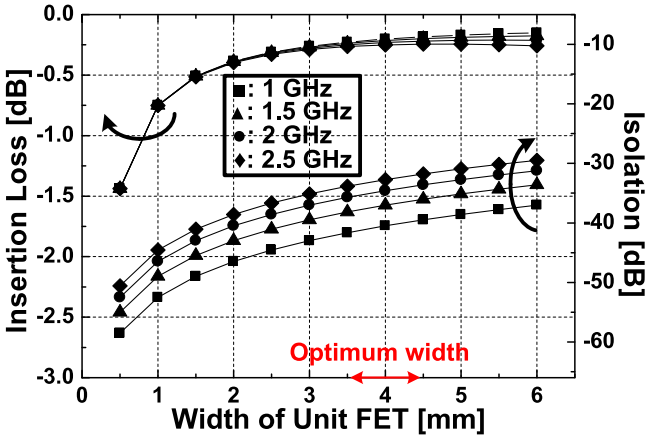
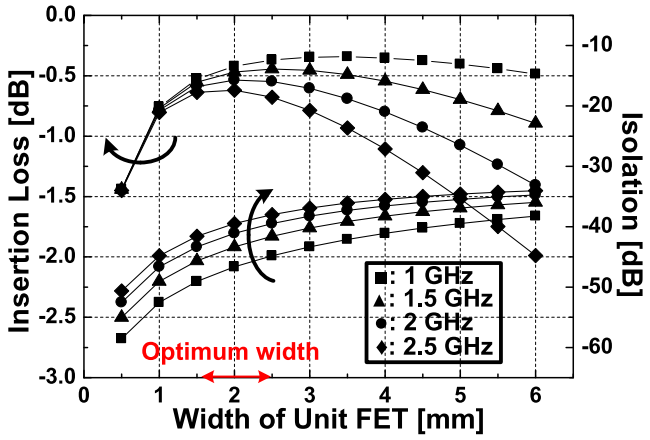


(a)



(b)

Fig. 5. Calculated insertion loss and isolation of 10-stacked antenna switches with the β of 0.5 according to the variation of the W_{g_unit}: (a) SPDT and (b) SP10T.

isolation among Tx ports are given by

$$S_{21}(\text{I.L.}) \simeq 10\log\left[\frac{4{R_S}^2}{(2R_S + R_{on}|_{series})^2 + w^2 {R_S}^4 C_{off}|^2_{series}(N+\beta)^2}\right] \quad (4)$$

and

$$S_{21}(\text{Isol.}) \approx 10\log\left(\frac{[2R_S C_{off}|_{series} R_{on}|_{shunt}]^2 w^2}{(R_S+R_{on}|_{shunt})^2 + w^2 {R_S}^2 C_{off}|_{series}{}^2 (R_S+R_{on}|_{shunt})^2 (N+\beta)^2}\right) \quad (5)$$

where N is the number of throws.

Fig. 5 shows calculated insertion loss and isolation of 10-stacked SPDT and SP10T antenna switches with the β of 0.5 according to the variation of the W_{g_unit}. For 10-stacked SPDT switch with the β of 0.5, the W_{g_unit} of 4 mm is desirable to achieve insertion loss less than 0.3 dB from 1 to 2.5 GHz frequency bands while consuming reasonable chip size. This optimum W_{g_unit} ensures enough isolation greater than +30 dB over target frequency bands.

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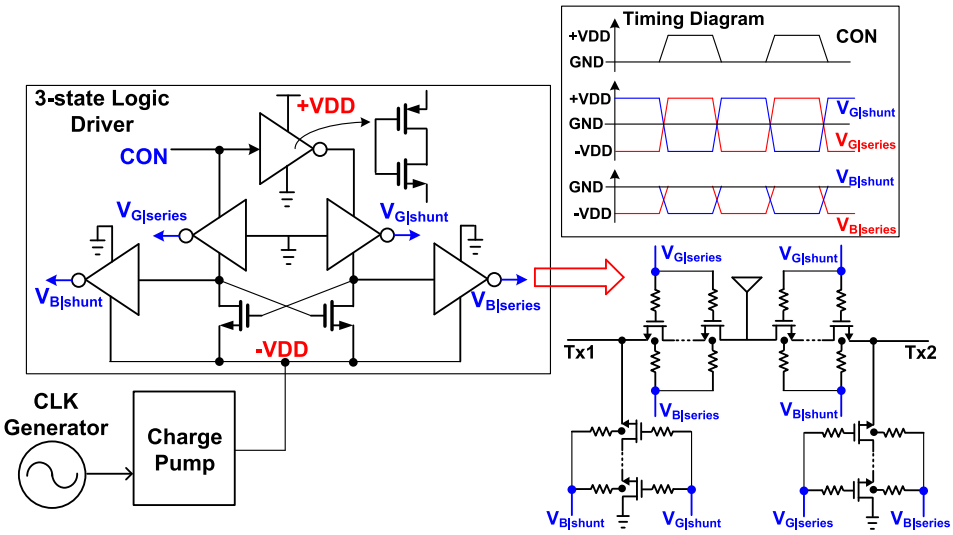

Fig. 6. Proposed antenna switch controller.

On the other hand, for 10-stacked SP10T switch with the β of 0.5, optimum W_{g_unit} is shifted from 4 to 2 mm, because the large W_{g_unit} makes high off-state capacitance resulting from many off-state branches, and thus severely degrades insertion loss at high frequencies. Fortunately, the 10-stacked SP10T switch adopting the W_{g_unit} of 2 mm shows reasonable insertion loss and isolation performances.

5 Antenna switch controller

Fig. 6 shows proposed antenna switch controller that utilizes a charge pump as a tool to generate a negative voltage. It consists of a clock generator, a charge pump, and a 3-state logic driver. An oscillator along with a clock buffer generates differential clock signals with straight edges to be used in the charge pump, and the charge pump yields the negative voltage as a result of transferring charges to a capacitive load. This negative voltage is fed to the 3-state logic driver. Unlike traditional inverter logic, the 3-state logic driver generates one of three states of logic 1 (+VDD), logic 0 (GND), and logic −1 (−VDD) according to control signal CON as shown in timing diagram of Fig. 6. For on-state (off-state) stacked-FETs, the 3-state logic driver actually feeds logic 1 (logic −1) to its gate and logic 0 (logic −1) to its body. One of the most interesting things in proposed 3-state logic driver is that none of the adjacent nodes of the MOSFETs experience a voltage difference greater than +VDD which is the nominal voltage given in process technology. This avoids any reliability issues for used MOSFET devices.

6 Experimental results

The high power SPDT antenna switch has been implemented in partially depleted SOI (PDSOI) CMOS technology. Fig. 7 shows the chip photograph of designed SPDT switch. As mentioned above, the number of stacks for series and shunt stacked-FETs is set equal to 10 to achieve input P_{1dB} greater

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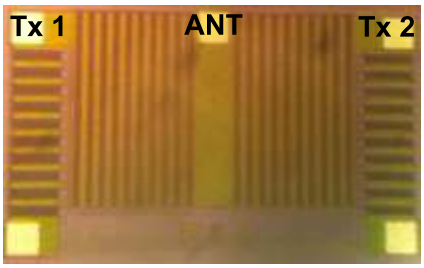

Fig. 7. Chip photograph of the designed SPDT switch.

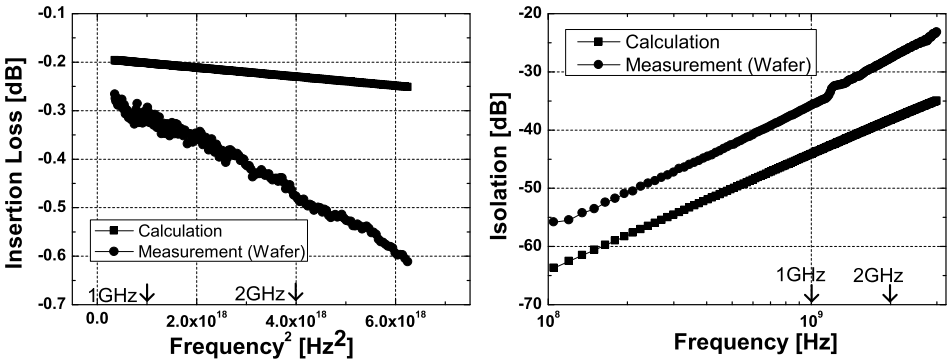

Fig. 8. Calculated and measured (a) insertion loss and (b) isolation performances of the SPDT switch.

than +40 dBm. From the analysis on optimum channel width in chapter 4, the channel width of unit FET inside of series and shunt stacked-FETs is chosen as 4 mm and 2 mm, respectively. To achieve path switching time less than 3 μsec, floating gate and body resistors R_G and R_B in the range of 70 kohm are used.

Fig. 8 shows calculated and measured insertion loss and isolation performances of the SPDT switch. To distinguish two degradation effects by R_{on} and C_{off} on the insertion loss, new characterization method where the insertion loss with dB scale is plotted against the square of frequency is used for the analysis. Since the y-intersection is only related to R_{on} and the slope is only dependent on C_{off} at I.L. (dB) vs. f^2 plot, this is very useful characterization method to distinguish two degradation effects by R_{on} and C_{off} on the insertion loss. For measured insertion loss, the y-intersection is comparable to that for calculated result, but the slope becomes more negative. This is because additional capacitance from PAD and interconnection. The worst insertion loss of the SPDT switch is less than 0.5 dB form 100 MHz to 2.5 GHz. In case of measured isolation, it shows a roll-off rate of 6 dB per octave like calculated result. The difference between calculated and measured results comes from additional contact resistance of a probe. Fig. 9 shows measured power handling capability the SPDT switch. It shows input P_{1dB} greater than +40 dBm at both 1 GHz and 2 GHz.

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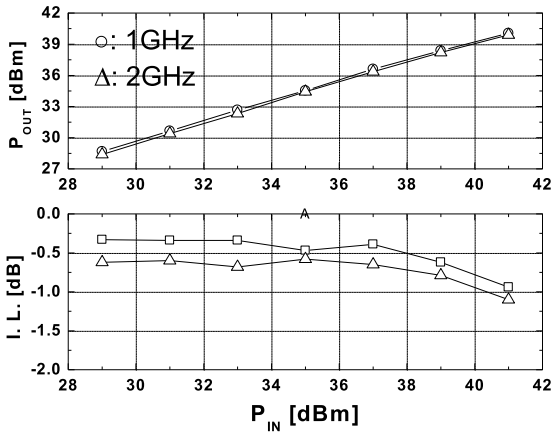

Fig. 9. Measured power handling capability of the SPDT switch.

7 Conclusion

In this paper, new DC I-V (FFI-V) characterization method was proposed in order to characterize P_{1dB} point of off-state FETs for antenna switch applications. Based on proposed FFI-V method, experimental study on optimum DC bias point to maximize the power handling capability of antenna switches was performed. In conclusion, using R_{on} and C_{off} of minimum channel length MOSFETs at aforementioned optimum DC bias point, antenna switch design methodology for maximum power handling capability and minimum insertion loss was established. The designed SOI CMOS SPDT antenna switch integrated with 3-state logic driver to generate DC gate and body bias for on and off-states shows insertion loss less than 0.5 dB and input P_{1dB} greater than +40 dBm over target frequency bands.

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