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Highly linear common-gate mixer employing intrinsic second and third order distortion cancellation

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Abstract: This paper presents a new derivative superposition scheme for simultaneous cancellation of second and third-order distortions in common-gate transconductance stage of mixer, addressing the challenging dynamic range required in multi-mode front-end CMOS circuits. Using Volterra series analysis, the unsatisfactory results of conventional derivative superposition in common-gate structures, and thus the need for simultaneous cancellation is investigated. An inductor interposed between two transconductances tunes out the parasitic capacitors and improves conversion gain. Simulation results of proposed mixer in a 0.13 μm-CMOS technology with 1.2 V supply illustrate 16-dB improvement in IIP3 and 30-dB increase in IIP2 compared to conventional Gilbert mixer.

Keywords: CMOS mixer, common-gate, derivative superposition, highly linear

Classification: Integrated circuits

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1 Introduction

The need for high data rate multi-mode wireless communications has motivated a strong interest towards the development of multi-standard mobile terminals. One key challenge in bringing out a multi-mode front-end resides in fulfilling the high linearity and low power over a wide frequency ranges. Mixer is one of the important blocks in the RF front-ends whose inter-modulation distortion greatly affects the dynamic range of communication systems [1].

Generally a double-balanced Gilbert-cell mixer is used for up/down-conversion, composed of transconductance stage, switching stage, and loads. Transconductance can be either a common-source or a common-gate MOSFET. However, common-gate structure offers wider bandwidth and better matching, compared to its common-source counterpart.

The transconductance nonlinearity is considered the main source of third-order distortion in active mixers [1], while contributing to second-order distortion (IM2) as well. In addition, switching pair nonlinearity and mismatches are other sources of IM2 generation, in which nonlinear parasitic capacitance at common-source node of switching stage dominates the IM2 generation [2].

The random mismatch between switching transistors can be modeled by an offset voltage, which charges/discharges the above parasitic capacitor in each period of the local oscillator frequency (ω_{LO}). The nonlinear current generated in the transconductance modulates the device biasing current, and hence impacts the charging/discharging time constant of the capacitor. This produces two sidebands around $(2k+1)\omega_{LO}$ in the source voltage spectrum which are finally downconverted by switching stage [2]. Therefore, it can be inferred that IM_2 current at the output of the mixer can be suppressed either by tuning out the parasitic capacitor or by cancelling the second and third-order nonlinear currents simultaneously in the transconductance. The latter is the focus of this paper, as will be described below.

It should be noted that, while CMOS technology scaling improves the switching stage nonlinearity, it deteriorates nonlinear performance of the transconductance due to supply voltage and high-field mobility effects [2, 3].

Derivative Superposition (DS) is a third-order distortion cancellation scheme. It is utilized in [4] to achieve high IIP3 in common-source transconductance. However, the amount of IIP3 is limited due to second-order distortion interaction generated in intrinsic/applied series or shunt feedback structures. Modified DS technique in inductively degenerated LNA is also utilized [5] to cancel second-order nonlinearity, giving rise to extra ordinary IIP3. Nevertheless, the above techniques are limited to common-source structures.

Second and third-order distortions have mutual effects, meaning that one can generate the other by different mechanisms like mismatches and feedbacks in the circuit. Therefore, in order to design highly linear multi-mode front-end with low power consumption and reasonable gain, a cancellation scheme is required to simultaneously suppress both distortions.

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In this paper, a new derivative superposition scheme for simultaneous cancellation of second and third-order distortions in common-gate structures is introduced. The necessity of simultaneous cancellation to achieve high IIP3 is investigated by Volterra series analysis. Also, it is shown that conventional DS is not useful for common-gate structures. Although the target application for this design is IEEE802.11a standard, the technique is applicable to many wireless communication systems.

This paper is organized as follows. Section 2 begins with mixer nonlinearity analysis and continues with explaining the new linearization technique used for distortion cancellation. The proposed mixer and simulation results are provided in Sections 3 and 4, respectively. Finally, conclusion is given in Section V.

2 Novel Derivative Superposition Scheme

The nonlinearity of MOSFET drain current stems from the nonlinear transconductance g_m as well as the nonlinear drain conductance $g_{ds} = 1/r_o$. In a conventional Gilbert cell, the nonlinearity of g_{ds} is less noticeable due to small shunt resistance of the switching stage. Thus, the small signal drain current of a common-gate transconductance MOSFET can be expressed by the following Taylor series expansion

$$i_{ds} = g_m v_{gs} + \frac{g'_m}{2!} v_{gs}^2 + \frac{g''_m}{3!} v_{gs}^3 + \cdots \tag{1}$$

where v_{gs} is gate-to-source voltage, g'_m and g''_m denote the first and second order derivative of g_m, respectively. To have insight about distortion mechanisms, Volterra series analysis is employed to calculate third-order intercept point of a common-gate transconductance with Z_L at drain, Z_1 at source, and Z_s at the input.

$$IIP3(2\omega_2 - \omega_1) = \sqrt{\frac{4}{3}\left|\frac{B_1(j\omega_1)}{B_3(-j\omega_1, j\omega_2, j\omega_2)}\right|} \tag{2}$$

where $B_1(j\omega_1)$ and $B_3(-j\omega_1, j\omega_2, j\omega_2)$ are the first and third-order Volterra kernels for the output voltage at the drain, respectively. Calculating Volterra kernels will result in the following equation for IIP3 at the output, while small signal drain voltage caused only by r_o is neglected for simplicity

$$IIP3(2\omega_2 - \omega_1) = \sqrt{\frac{4}{3}\left|\frac{(r_o||Z_L(-j\omega_1))Z_s(j\omega_2)\,|H(j\omega_2)|^2\,|r_o||Z_L(j\omega_2)|^2}{r_o^2(r_o||g_{m^{-1}})^3 Z_s(j\omega_1)H(j\omega_1)\cdot F\cdot\delta}\right|} \tag{3}$$

where

$$H(s) = \frac{r_o||g_{m^{-1}}}{r_o||Z_L(s)} \cdot \frac{r_o}{Z_1(s)||Z_s(s)||r_o||g_{m^{-1}}} \tag{4}$$

$$F = \left[\frac{r_o}{H(-j\omega_1 + j\omega_2 + j\omega_2)} - (r_o||Z_L(-j\omega_1 + j\omega_2 + j\omega_2))\right] \tag{5}$$

and

$$\delta = \frac{g'^2_m}{4}\frac{r_o(r_o||g_{m^{-1}})}{Z_s(-j\omega_1)H(-j\omega_1)\,(r_o||Z_L(j\omega_2 + j\omega_2))\,H(j\omega_2 + j\omega_2)} - \frac{g''_m}{6}\frac{1}{Z_s(-j\omega_1)H(-j\omega_1)} \tag{6}$$

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Eq. (3) and (6) reveal that second-order distortion, g'_m, plays an important role in degradation of third-order intercept point. Since the impedance at the source is not negligible, employing differential circuits for second-order distortion cancelation is useless.

Fig. 1 (a) shows the conventional DS linearization scheme. In this superposition scheme, g''_m sign inversion around the sweet spot, where g''_m crosses zero in moderate inversion region, is employed to cancel g''_m by biasing one of the transistor pair in weak inversion with positive g''_m and the other at strong inversion with negative g''_m. However, when the transistors are biased in the above regions, the second-order nonlinearity of both transistors is at the highest. Consequently, the main drawback of the conventional DS is that second-order nonlinear currents of two transistors are summed up and the total attains a peak (Fig. 1 (b)). Therefore, as shown in Eq. (3) and (6), in conventional DS for common-gate and degenerated common-source structures, the second-order nonlinearity interacts with input signal, generating third-order distortion. Besides, large second-order nonlinear current at the output of transconductance degrades IIP2 performance of the mixer dramatically. Thus, not only conventional DS for cancellation of third-order distortion cannot sufficiently improve IIP3 in these structures, but also it deteriorates IIP2 performance, giving rise to the need for simultaneous cancellation of second and third-order distortions.

Although the second-order nonlinear current does not have such a sweet spot as third-order one, a symmetric property around zero crossing voltage of third-order nonlinear current can be utilized. This symmetry means that two

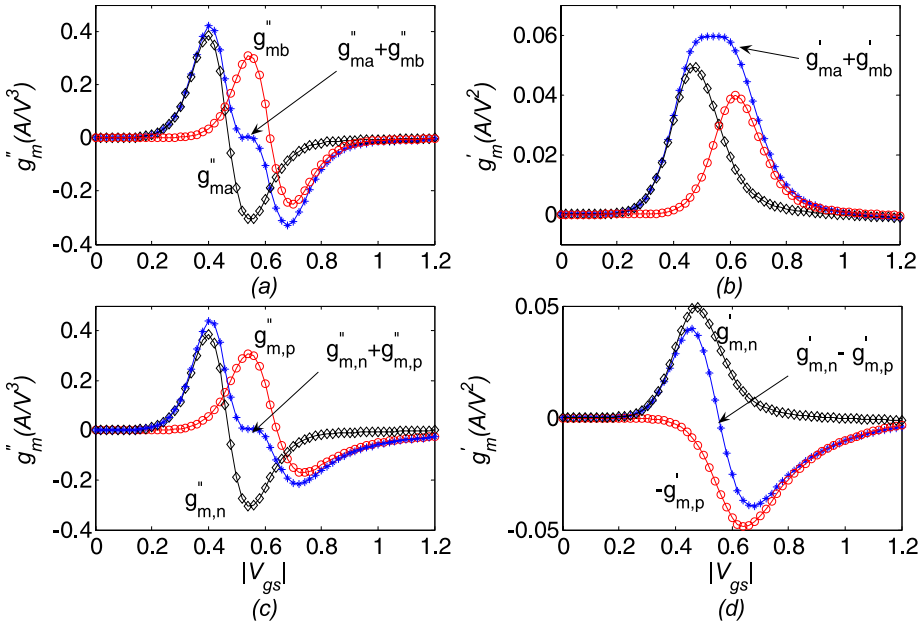

Fig. 1. (a-b) third and second-order nonlinear currents of main transistor M_a, and auxiliary FET M_b, and their summation. (c-d) third and second-order nonlinear currents of main NMOS and auxiliary PMOS and their summation.

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devices employed in DS scheme have equal second-order nonlinear currents. As a result, in order to cancel both second and third-order nonlinear currents, a PMOS transistor with complementary g'_m characteristics is exploited in weak inversion with positive g''_m to simultaneously cancel the second and third-order nonlinearities. The results are shown in Fig. 1 (c-d).

Taylor series analysis for proposed common-gate transconductance is presented in (7). As this equation predicts and Fig. 1 (c-d) shows, both second and third-order nonlinearities can be eliminated from single-ended output current i_o if both NMOS and PMOS devices have well matched g'_m and g''_m.

$$\begin{aligned} i_{out} = i_{ds,n} - i_{sd,p} &= \left(g_{m,n} \cdot (-v_{in}) + \frac{g'_{m,n}}{2} \cdot (-v_{in})^2 + \frac{g''_{m,n}}{6} \cdot (-v_{in})^3 \right) \\ &\quad - \left(g_{m,p} \cdot v_{in} + \frac{g'_{m,p}}{2} \cdot v_{in}^2 + \frac{g''_{m,p}}{6} \cdot v_{in}^3 \right) \\ &= -(g_{m,n} + g_{m,p}) \cdot v_{in} + \frac{(g'_{m,n} - g'_{m,p})}{2} \cdot v_{in}^2 - \frac{(g''_{m,n} + g''_{m,p})}{6} \cdot v_{in}^3 \end{aligned} \quad (7)$$

3 Proposed Mixer

The schematic of the highly linear common-gate mixer is shown in Fig. 2. The value of L_1 and L_2 at the input of the transconductance is chosen to tune out the parasitic capacitance of the mixer input at the frequency of interest (ω_0)

$$\omega_0^2 \approx \frac{1}{(L_1 || L_2)(C_{gs1} + C_{gs3})} \quad (8)$$

Here C_{gs1} and C_{gs3} are the gate-source capacitance of M1 and M3 transistors, respectively. Instead of providing parallel resonance at the input, the value of source inductance can also be chosen sufficiently large at the operating frequency to prevent loading the input. In order to match input impedance to source impedance (R_s), $g_{m1} = 1/R_s$ should be chosen. This allows wide-band input matching. M3 and M4 are biased in weak inversion to generate positive g''_m to cancel third order nonlinearities of NMOS transistors. Consequently, their transconductances are very small compared to NMOS transistors.

M1 and M2 are sized ($5\,\mu$m/$0.13\,\mu$m) $\times$ 8 to satisfy input matching criterion. The size of M3 and M4 are chosen to fully cancel the second and third-order nonlinear currents of M1 and M2. M3 and M4 transistors are sized by ($17\,\mu$m/$0.13\,\mu$m) $\times$ 50. This large size produces large parasitic capacitor at the source of switching pair, degrading gain, noise figure, and linearity of the mixer. In order to tune out this parasitic capacitor, an inductor is interposed between the outputs of two transconductances.

$$\omega_0^2 \approx \frac{1}{L_d(C_{pn} + C_{pp})} \quad (9)$$

where C_{pn} and C_{pp} denote the parasitic capacitance at the drain of NMOS and PMOS, respectively. L_d is chosen 1.45 nH with Q of 15 @ 5 GHz, which can be easily implemented by an on-chip inductor. This technique improves conversion gain of mixer by 5.5 dB (Fig. 3 (a)), while has minor side-effect on sensitivity of the linearization scheme to biasing current variation. However,

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it produces phase shift in high order nonlinear currents and makes redesigning of cancellation circuit inevitable. This phase shift makes distortion cancellation happen at smaller bias current, thus the power consumption will be greatly reduced.

The switching transistors M5-M8 are driven by a local oscillator with 9-dBm power to reach the maximum possible gain and linearity. PMOS transistors M9-M10 are used to provide mixer biasing current, and to create active load at the output. They require lower voltage headroom, while creating common mode feedback (CMFB) in combination with resistor R at the output to set the output dc voltage.

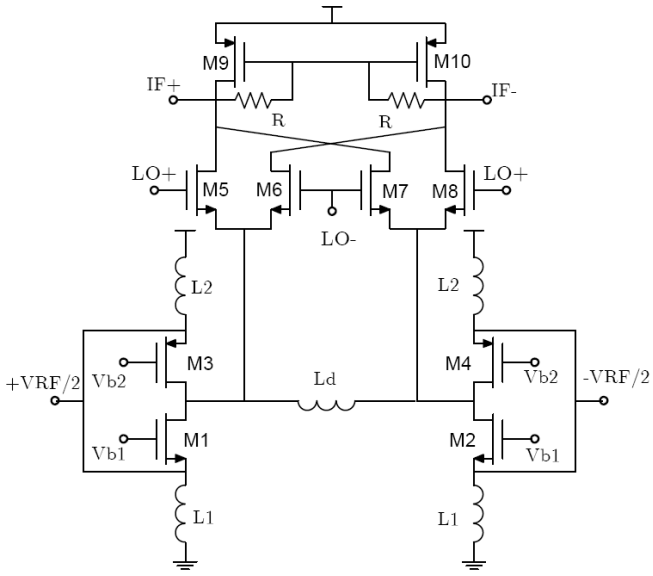

Fig. 2. Schematic of common-gate highly linear mixer.

4 Simulation Results

The design was done in a 0.13 μm 1P8M CMOS technology with 1.2 V supply. The results are extracted using Advanced Design System (ADS) simulator. Simultaneous cancellation of second and third-order distortions results in extraordinary IIP3 of +18-dBm and IIP2 of +77-dBm at 5 GHz. The IIP3 of the mixer was simulated by two input tones with 1 MHz offset, and as expected from simultaneous cancellation, both IIP2 and IIP3 show slight dependency on two-tone frequency spacing. The conversion gain and noise figure of the mixer is 11.6 and 13.8 dB, respectively, while drawing only 2.8 mA from 1.2 V supply. In order to simulate the effects of matching and threshold variation, bias point of M1 and M2 is varied. This will help to investigate the sensitivity of distortion cancellation scheme, as shown in Fig. 3 (b-c). In this figure, a reasonable low-distortion voltage range for both IIP2 and IIP3 can be observed. Nonlinear performance of the proposed mixer is also compared with conventional Gilbert mixer with the same power consumption. The results are given in Fig. 3 (b-c), which illustrate 16-dB and 30-dB improve-

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ment in IIP3 and IIP2, respectively. Further, Fig. 3 (d) shows input and output power characteristics of the mixer with and without auxiliary PMOS transistors for equal power consumptions. Also, this figure shows that IIP3 improvement is about 16-dB. The IM3 cancellation scheme holds effective for input power levels as large as −25 dBm. For higher power levels, the slope is steeper than 3:1, indicating that IMD_3 is dominated by fifth and seventh order nonlinearities.

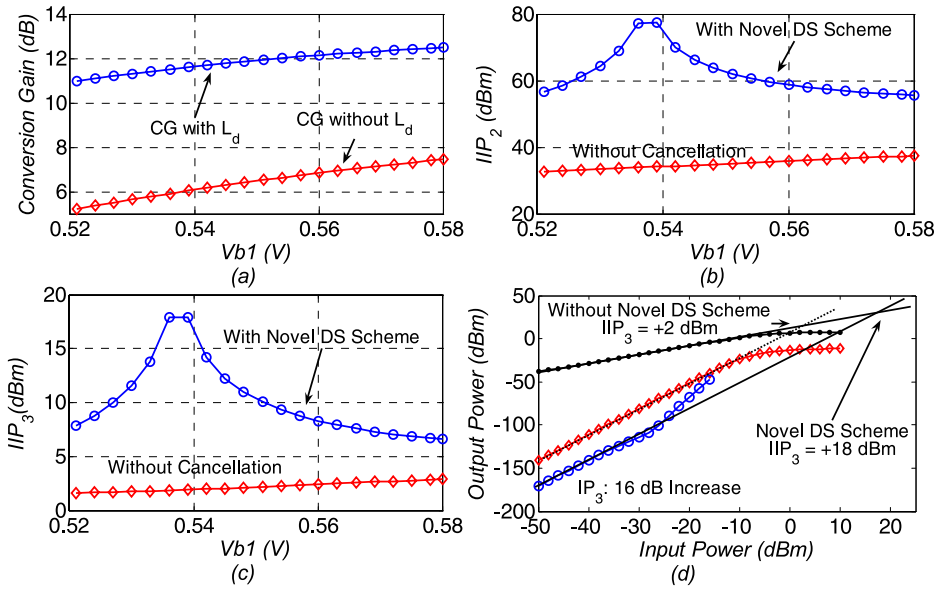

Fig. 3. (a) Conversion gain enhancement by L_d (b-c) The IIP3 and IIP2 performance of the proposed mixer at 5 GHz.

5 Conclusion

A common-gate mixer with very low IM3 and IM2 distortion was presented, using a 0.13 μm-CMOS technology. This is designed by exploiting simultaneous second and third-order distortion cancellation based on an innovative DS scheme, which utilizes PMOS as an auxiliary FET in common-gate transconductance. An inductor interposed between two transconductances tunes out the parasitic capacitors and improves conversion gain. Simulation shows that the mixer achieves 16-dB and 30-dB improvement in IIP3 and IIP2, respectively, in comparison with conventional Gilbert mixers with the same power consumption. The conversion-gain of the mixer is 11.6-dB and draws only 2.8 mA form 1.2 V supply.

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