

Effect of charge sharing on SEU sensitive area of 40-nm 6T SRAM cells

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Abstract: The effect of charge sharing on single event upset (SEU) sensitive area of SRAM cells is studied in a 40-nm bulk CMOS technology. All transistors in a 6T SRAM cell are simulated in 3D TCAD models, and SEU sensitive areas are measured in different simulation conditions. We find the charge sharing can reduce SEU sensitive area of SRAM cells. The effect of charge sharing on radiation sensitivity of both PMOS and NMOS are analyzed in depth. The works in this paper can guide the single event rate prediction and the hardened design of SRAMs in advanced technologies.

Keywords: 6T SRAM cell, charge collection, charge sharing, single event upset (SEU) sensitive area, single event upset reversal (SEUR)

Classification: Integrated circuits

References

- [1] L. L. Sivo, J. C. Peden, M. Brettschneider, W. Price and Pentecost: IEEE Trans. Nucl. Sci. **26** (1979) 5042.
- [2] L. W. Massengill, B. L. Bhuvu and W. T. Holman: Int. Reliab. Phys. Symp. (2012) 3C.1.1.
- [3] O. A. Amusan, A. L. Sternberg, A. F. Witulski, B. L. Bhuvu, J. D. Black, M. P. Baze and L. W. Massengill: Int. Reliab. Phys. Symp. (2007) 306.
- [4] G. Touré, G. Hubert, K. C. Coulié, S. Duzellier and J. M. Portal: IEEE Trans. Nucl. Sci. **58** (2011) 862.
- [5] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuvu, R. D. Schrimpf, J. K. Wang, B. Bartz, E. Pitta and M. Buer: IEEE Trans. Nucl. Sci. **58** (2011) 2761.
- [6] G. Damien, R. Philippe, G. Gilles and H. S. Reno: IEEE Trans. Nucl. Sci. **54** (2007) 904.
- [7] I. Chatterjee: Ph.D thesis University of Vanderbilt, Tennessee (2012).
- [8] J. J. Chen, S. M. Chen, B. Liang and F. Y. Liu: Sci. China Tech. Sci. **55** (2012) 867.
- [9] J. J. Chen, S. M. Chen, B. Liang and B. W. Liu: IEEE Trans. Device Mater. Rel. **12** (2012) 501.
- [10] J. R. Qin, S. M. Chen, B. Liang and B. W. Liu: Chin. Phys. B **21** (2012) 029401.

- [11] H. H. K. Lee, K. Lilja, M. Bounasser, I. Linscott and U. Inan: IEEE Trans. Nucl. Sci. **58** (2011) 3026.

1 Introduction

As one of the most sensitive electronic devices in radiation environments, Static random access memory (SRAM) has been catching the researchers' attentions since the late 1970s [1]. With technology scaling down, the charge sharing between neighboring SRAM cells is strengthened to cause multi single event upsets (SEUs), and increase the radiation immunity of SRAMs in many studies [2, 3].

Moreover, many previous conclusions about the sensitivity of SRAMs are no longer applicable for advanced technologies because of charge sharing. Using electrical simulations, Touré et al. clarified that the sensitive zones of SRAM cells depends on charge sharing in 90 nm and 65 nm bulk CMOS technologies [4]. Chatterjee et al. found that SEU can be quenched in SRAM cells via the 3D device/circuit mixed mode of technology computer-aided-design (TCAD) simulation, and termed it as "Single Event Upset Reversal (SEUR)" [5].

Although, the significance of charge sharing in SRAM cells in advanced technologies has been noticed, some simulations of some research did not reflect the sensitivity of SRAM cells accurately due to their intrinsic drawbacks. The rough simulation methods, such as electrical simulation, can not describe the physics characterization of charge sharing in appropriate way. The 3D device/circuit mixed mode neglects charge sharing between device models and SPICE models. For instance, the unconcerned access transistors, which are always constructed with SPICE models, also affect the sensitivity of SRAMs [6].

In this work, we study the effect of charge sharing on SEU sensitive area of 40-nm standard 6T SRAM cells by using full 3D TCAD simulation, in which all of the transistors in a SRAM cell use 3D models. All potential influence of each transistor on charge sharing can be well presented in our simulations. The simulation results show that the charge sharing reduces SEU sensitive areas of both PMOS and NMOS. The causes of SEU sensitive area reduction are discussed. The work in this paper can improve the accuracy of SER prediction, and guide the hardened design in advanced technologies.

2 Simulation details

The classical 6T SRAM cells are widely adopted in commercial integrated circuits because of its excellence on both performance and reliability. Fig. 1 (a) shows the schematic of the 6T SRAM cell used in our simulation. The corresponding 3D TCAD block is illustrated in Fig. 1 (b). The layout details of the 3D TCAD block were extracted by Memory Compiler based on a commercial 40-nm bulk CMOS technology that did not adopt the optimization methods

(such as High-K metal gate). The size of each transistor in a 6T SRAM cell is listed in Table I. The doping profiles of the 3D TCAD models are referred to Ref. [7], and are calibrated to the DC and AC electrical characteristics of the process development kit (PDK) supplied by the process foundry. The I-V characteristics between the 3D TCAD models and the SPICE models can be well matched. We simulate the hit of heavy ions with an electron-hole pair column, whose length and radius is $4.5\ \mu\text{m}$ and $0.05\ \mu\text{m}$, respectively. The physical models and other parameters used in our simulations are the same as Ref. [7, 8].

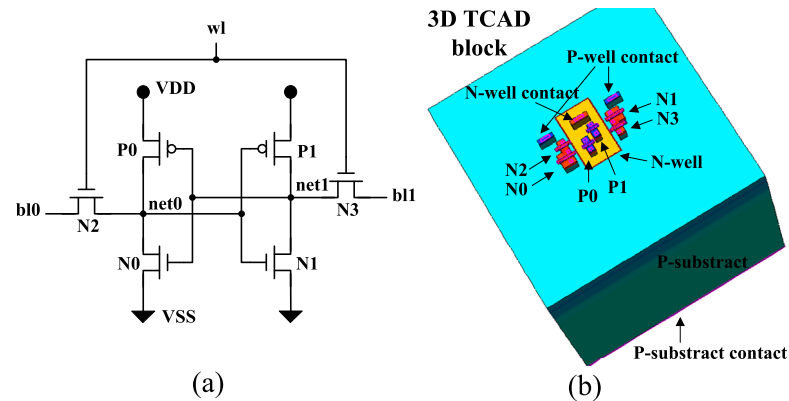


Fig. 1. (a) Schematic illustration of a 6T SRAM cell, and (b) 3D models for a 6T SRAM cell.

Table I. Size of each transistor in a 6T SRAM cell.

transistor	width(nm)	length(nm)
P0,P1	140	50
N0,N1	285	50
N2,N3	155	60

For each simulation, the storage state of net0 and net1 is initialized to low and high respectively, and N2 and N3 are Off in all simulations. The drain center of device is regarded as the center point of SEU sensitive area, and then the hit location is extended to eight directions (i.e., east, southeast, south, southwest, west, northwest, north and northeast). The extended step of the hit location is $0.05\ \mu\text{m}$ and the last hit location induced SEU is treated as the boundary of SEU sensitive area in each direction. SEU sensitive area of device can be got after confirming the boundary in eight directions by simulation.

To investigate the effect of charge sharing on SEU sensitive area further, we take another 3 simulation cases (case2-4 listed in Table II) in which the charge sharing is removed by taking electrical connection out [9]. Case1 is the normal case and contains all the 3D TCAD models in one cell. There are two SRAM cells in case2-4: one is Hit Cell and the other is Dummy Cell. The part of models in the 3D TCAD block, which are retained electrical connection, are put into Hit Cell to obtain SEU sensitive area without

charge sharing. The remanent models in the 3D TCAD block, which are canceled electrical connection, are put into Dummy cell to collect charge normally after particle striking. Both of Hit Cell and Dummy Cell are complemented by SPICE models, and the 3D device/circuit mixed mode is used in simulations.

Table II. Simulation cases adopted in this paper.

Case	Transistor(s) used 3D TCAD model in Hit Cell	Transistor(s) used SPICE model in Hit Cell	Transistor(s) used 3D TCAD model in Dummy Cell	Transistor(s) used SPICE model in Dummy Cell
case1	P0,P1,N0,N1,N2,N3	none	none	none
case2	P0	P1,N0,N1,N2,N3	P1,N0,N1,N2,N3	P0
case3	N1,N3	P0,P1,N0,N2	P0,P1,N0,N2	N1,N3
case4	P0,N0,N1,N2,N3	P1	P1	P0,N0,N1,N2,N3

According to the simulation results of case1 & case2 and case1 & case3, the effect of charge sharing on PMOS and NMOS's SEU sensitive area can be investigated, respectively. The difference between case1 and case4 is whether P1 in On-state is omitted from Hit cell as shown in Table II. It clarifies the influence of On-PMOS on SEU sensitive area. For each simulation, the CPU burden is around two days to simulate the 3D TCAD block with high performance workstations. Since the total amount of simulations is large, it has taken several months to get SEU sensitive areas for our studies.

3 Simulation results

Fig. 2 (a) shows SEU sensitive areas of P0 obtained in case1 and case2, while linear energy transfer (LET) is $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ making the charge sharing much more noticeable. SEU sensitive area of P0 (i.e., $0.14 \mu\text{m}^2$) in case2 is much larger than that (i.e., $0.08 \mu\text{m}^2$) in case1. It is indicated that the charge sharing between PMOS and its neighbors can reduce SEU sensitive area. Under the same simulation conditions, SEU sensitive areas of N1 obtained in case1 and case3 are shown in Fig. 2 (b). We conclude that the charge sharing also reduces SEU sensitive area of NMOS sharply. Interestingly, in Fig. 2 the largest SEU sensitive area reduction of P0 and N1 are all near to P1, so On-PMOS can help to reduce SEU sensitive area of both Off-PMOS and Off-NMOS synchronously in the 6T SRAM cells. It also concludes that the sensitivity of SRAMs in previous studies, which neglect the charge sharing among all transistors, lack enough accuracy.

Since the LETs of incident particles have great influence on charge sharing [10], changing LETs in simulations is an effective method to further confirm the contribution of charge sharing to SEU sensitive area reduction. Fig. 3 (a) shows SEU sensitive areas of P0 and N1 in case1 at LET of 40 and $10 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, respectively. SEU sensitive areas of P0 and N1 both increase with the value of LETs, but their changes rate is different. Fig. 3 (b) gives the statistic details of Fig. 3 (a). The most interesting phenomena are that SEU sensitive area of P0 is not increased with LETs in the east, north-east and north, which violates the general rules that the radiation sensitivity

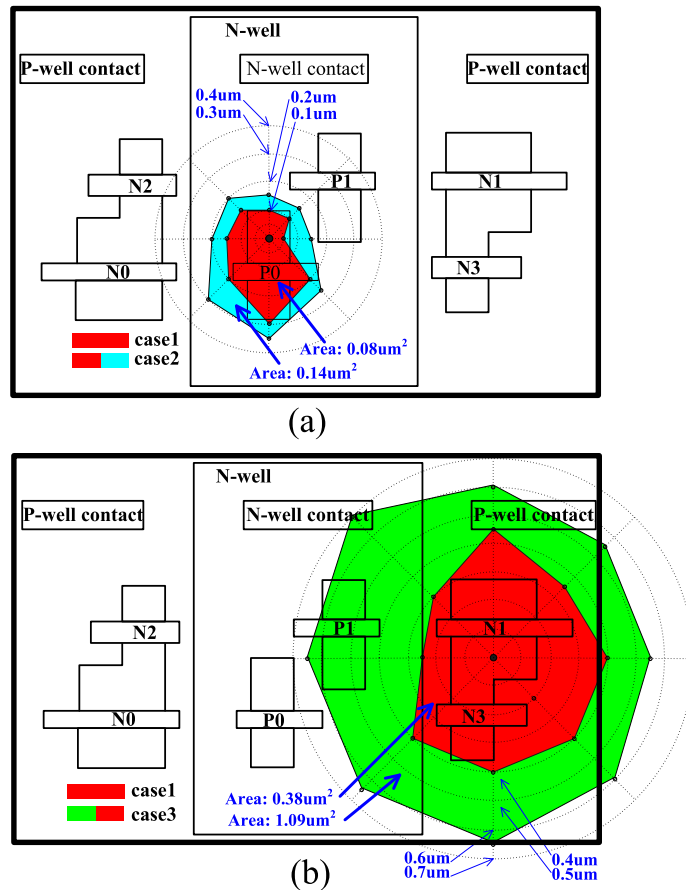


Fig. 2. SEU sensitive areas of (a) P0 in case1 and case2 and (b) N1 in case1 and case3 while the LET is $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

increases with LETs. It is indicated that P1 helps P0 to reduce SEU sensitive area exceedingly based on charge sharing, too. Moreover, there are only two directions (south and west) in which the increased area of N1 at different LETs is less than that of P0. It demonstrates that SEU sensitive area of NMOS has a stronger LET dependence than that of PMOS in SRAM cells.

4 Discussion

4.1 Effect of charge sharing on NMOS and PMOS in SRAM cells

In case1, after heavy ion hitting the region around N1, the charge collection of P1 not only helps to decrease the charge collection of N1 but also provides the compensation current for N1 to make their output node net1 more tolerant to upset [11]. In case3, although P1 helps to collect charge as well, it cannot provide the compensation current without electrical connection. It is the reason why SEU sensitive area of N1 in case3 is larger than that in case1 as shown in Fig. 2 (b).

To further confirm that P1 reduces SEU sensitive area of N1, the contrast simulations involving case1 and case4 are performed, and their results are shown in Fig. 4. After particles with LET of $40 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ hitting the

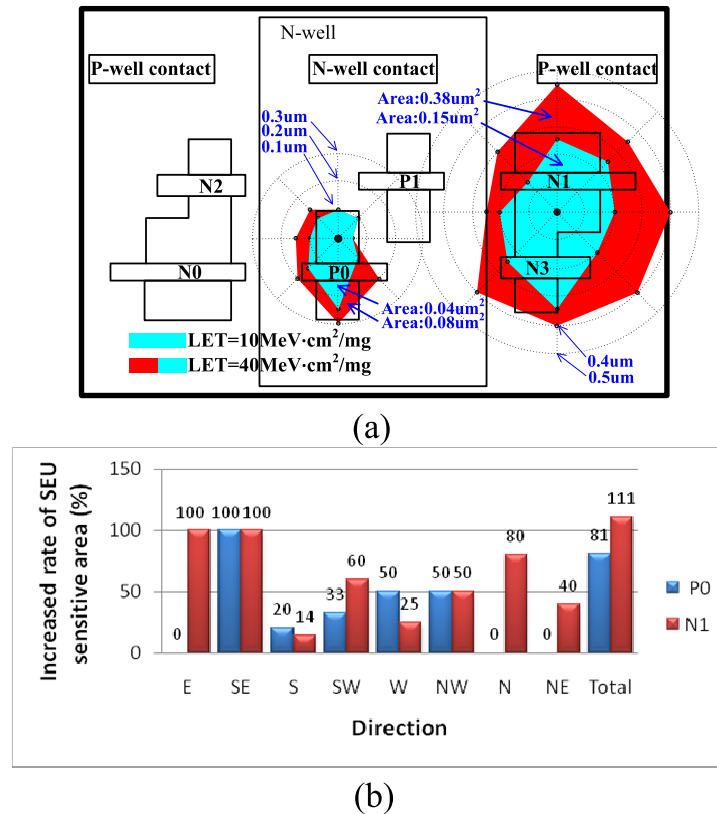


Fig. 3. (a) SEU sensitive area of P0 and N1 in case1 with LET of 40 and 10 MeV·cm²/mg, and (b) comparison of SEU sensitive area under these two conditions.

point 0.3 μm far away from west of N1's drain, the states of net0 and net1 upset in case4, but maintain the initial in case1. It is fully proven that the compensation current generated by On-PMOS due to electrical connection can restrain SEU for Off-NMOS.

SEU sensitive area of P0 has the largest increment in east in Fig. 2. It is because SEUR induced by charge sharing happens between P0 and P1 in

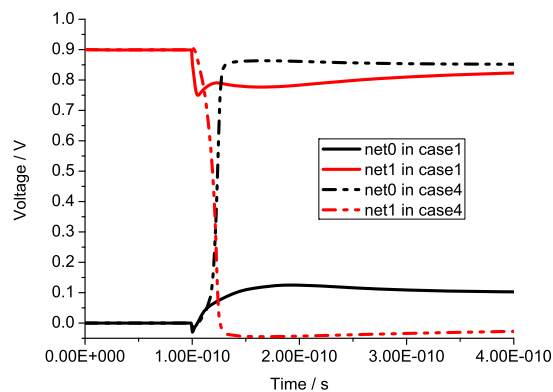


Fig. 4. Voltage pulses of net0 and net1 in case1 and case4, while the hit location is 0.3 μm far away from N1's drain in the west and the LET is 40 MeV·cm²/mg.

case1, but is restrained in case2 without electrical connection. The conclusions in Ref. [10] indicate that the occurrence rate of SEUR will increase with LETs. Thus, in Fig. 3(a), the increased LET enhances SEUR, which is triggered by charge sharing between P0 and P1, to restrain SEU sensitive area enlargement for P0 in the north, northeast and east.

Fig. 5 illustrates the state of net0 after the particles hitting the regions near to the drain of P0. SEUs occur when the space between the hit location and the center of P0's drain is no more than $0.05\ \mu\text{m}$. Single event transient (SET) is observed when the space is $0.1\ \mu\text{m}$, and it proves that SEUR comes forth. There is only small voltage disturbance when the space is no less than $0.15\ \mu\text{m}$. It is derived that the smaller the distance between the hit location and P1's drain, the larger the charge sharing, thus the strength of SEUR can be enhanced.

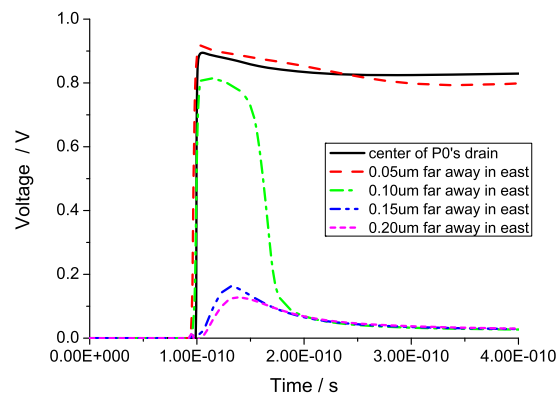


Fig. 5. Voltage pulses of net0 in case1, while the hit locations are in the east of P0's drain and the LET is $40\ \text{MeV}\cdot\text{cm}^2/\text{mg}$.

4.2 SEU sensitive area comparison

SEU sensitive area of NMOS is larger than that of PMOS in all the simulations with/without electrical connections and with different LETs. It is in agreement with the fact that NMOSs are more sensitive than PMOSs in SRAMs [4]. The reasons given in previous studies are two-folds: 1) the transient drain current in PMOS are lower magnitude and longer duration than that in NMOS; 2) NMOS size is much larger than PMOS size, and it makes NMOS more sensitive to particle striking. However, it is worth noting that these explanations did not consider the charge sharing in advanced technologies.

As shown in Fig. 3(a), the adjacent transistors of P0 are more than that of N1. In addition, the charge sharing between P0 and P1 is intense because of their short spacing. All of the above can reduce SEU sensitive area of P0. On the other hand, since N3 shares the same drain with N1, the charge generated by hit near to N3 can easily diffuse across the bottom of N3's source and gate to Off-drain of N1. It is the reason why SEU sensitive area

of N1 is much larger in the direction close to N3 as shown in Fig. 3 (a).

Since the charge sharing plays an important role on reducing SEU sensitive area of a single 40-nm 6T SRAM cell, we can increase the radiation immunity of SRAM cells by enhancing the charge sharing. For example, shortening the space between the drains of the two PMOSs can improve SEUR to reduce SEU sensitive area of PMOS in SRAM cells. Furthermore, the accuracy of SER prediction in 40-nm SRAMs can be improved if researchers fully regard that charge sharing can reduce SEU sensitive area of SRAM cells.

5 Conclusion

In this paper, we study the effect of charge sharing on SEU sensitive area of 40-nm 6T SRAM cells by using full 3D TCAD simulation. We compare SEU sensitive area obtained in a great deal of simulations with/without electrical connections and with different LETs, and find that the charge sharing can significantly reduce SEU sensitive area of SRAM cells. Through analyzing the effect of charge sharing on both NMOS and PMOS in details, it is indicated that SEUR plays an important role on reducing SEU sensitive area of PMOS. Moreover, On-PMOS can help collect charge and provide compensation current to reduce SEU sensitive area of NMOS. The previous conclusion that NMOS is more SEU sensitivity than PMOS in SRAM cells is also obtained in our simulations, and its reasons are further analyzed by charge sharing. Our work is a good guidance for SER prediction and hardened design of 40-nm SRAMs.

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