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A low-kickback-noise and low-voltage latched comparator for high-speed folding and interpolating ADC

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Abstract: A novel low-kickback-noise Class-AB latched comparator utilizing unilateralization technique is presented for high-speed folding and interpolating analog-to-digital converter (ADC). The load transistors are independent with the clock signal. So the comparator can suppress the kickback noise significantly and work at low power supply. Dummy transistors and neutralization technique are also introduced to further reduce the noise. The comparator is simulated in 0.18-μm standard digital CMOS technology. A very low kickback noise voltage of 0.14 mV is realized at the differential input voltage of 300 mV. The power dissipation is about 202 μW at 1.8 V supply voltage, 250 MHz clock frequency.

Keywords: latched comparator, kickback noise, analog-to-digital converters

Classification: Integrated circuits

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1 Introduction

Class-AB latched comparator can be introduced into the folding and interpolating analog-to-digital converter (ADC) for high speed and low power dissipation. However, the kickback noise can not be neglected. Due to the rail-to-rail signals at the regeneration nodes coupled directly to the inputs, it may make the ADC output code false and degrade the resolution efficiency. Fig. 1 (a) shows a traditional Class-AB latched comparator structure. Several approaches have been reported to reduce the kickback noise of the Class-AB latched comparator. Source followers are effective to reduce the kickback noise but induce more static consumption [1]. Neutralization technique can accomplish low kickback noise in some extent [2]. During the regeneration phase, the input nodes can be isolated from the regeneration nodes by using switches [3]. However, the input voltage is still disturbed when the sampling switches close. The isolation between the drains of differential pair transistors and the regeneration nodes reduces the kickback noise [4, 5]. However, it will make the input transistors go into the triode region easily, and the drain voltage variations will originate kickback noise in evidence. An improved circuit proposed by Figueiredo [6] can suppress the kickback noise significantly, as shown in Fig. 1 (b). Nevertheless, the circuit still needs to be improved further because there is still large kickback noise when transistors M_{11}/M_{12} are transiting between cutoff and saturation.

In this paper, a low kickback noise Class-AB latched comparator is proposed using unilateralization and neutralization techniques. Preamplifier and dummy MOS transistors are also introduced into the circuit to suppress the kickback noise. The comparator is simulated in 0.18-μm standard digital CMOS technology. A very low kickback noise voltage of 0.14 mV is realized at the differential input voltage of 300 mV. Under the 250 MHz clock frequency, low power dissipation can be achieved at 1.8 V supply voltage.

2 Proposed Class-AB latched comparator

Fig. 1 (a), (b) and (c) shows the traditional Class-AB latched comparator, an improved Class-AB latched comparator proposed by Figueiredo, and the propose Class-AB latched comparator in this paper respectively. Compared to the former two structures, we focused on suppressing the kickback noise in the circuit.

In the input stage of Fig. 1 (c), M_1 and M_{13}, M_2 and M_{14} form two pairs of source-coupled amplifiers, which can restrain the voltage variations at the sources of M_1/M_2. The diode-connected load transistors M_{11}/M_{12} operate in saturation region, not controlled by the clock signal in order to avoid the appearance of large instantaneous current. When the signal clk is low (reset phase), the differential input signals are amplified and applied to V_{op} and V_{on}. When clk goes high, nodes a_1/a_2 are disconnected from regeneration nodes. The latch circuit starts regenerating rail-to-rail output signals, which could not affect nodes a_1/a_2. M_{15}/M_{16} are used to reduce the clock feedthrough effects of M_9/M_{10}. M_{17} and M_{18} can neutralize the voltage variations at the

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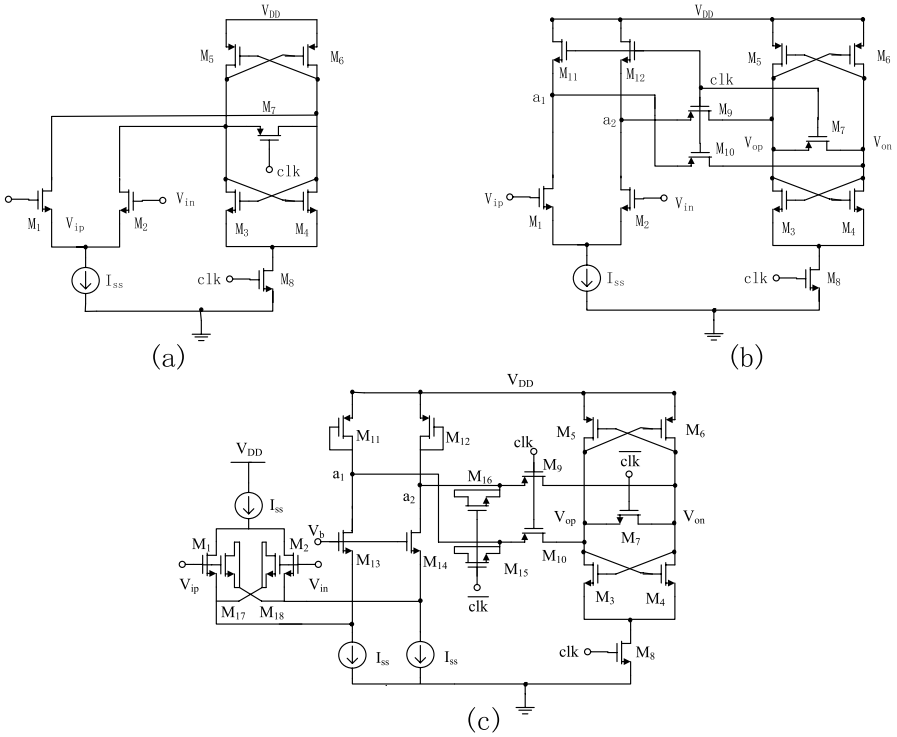

Fig. 1. (a) Traditional Class-AB latched comparator, (b) An improved Class-AB latched comparator proposed by Figueiredo [6], (c) The proposed Class-AB latched comparator in the paper

sources of M_1/M_2. The changement in our circuit compared to Fig. 1 (b) can suppress the kickback noise significantly, which will be illuminated later.

Considering the low supply voltage application, a source-coupled amplifier is used to achieve unilateralization. This can limit the direction of the signal-flowing which just flows from the inputs to the nodes a_1 and a_2. Therefore, the voltage variations at nodes a_1/a_2 is coupled to the inputs more slightly. Although the circuit would draw more current, lower supply voltage makes the whole comparator consume less power. The NMOS input transistors are designed to reduce parasitic capacitance of the input transistors to relieve the couple effects.

It is assumed that the voltage at node a_1 changes ΔV, the voltage variation ΔV_s at the source of M_1 is given by

$$\Delta V_s = \Delta V \frac{r_{o1}}{[1+(g_{m13}+g_{mb13})r_{o13}]r_{o1}+r_{o13}} \approx \frac{\Delta V}{(g_{m13}+g_{mb13})r_{o13}} \quad (1)$$

where, g_{m13} and g_{mb13} are respectively the transconductance and body transconductance of M_{13}. r_{o1}/r_{o13} are the output resistances of M_1/M_{13}. Usually, $(g_{m13}+g_{mb13})r_{o13} > 10$, so the coupling effects between $a_{1,2}$ and sources of $M_{1,2}$ can be reduced significantly, resulting in much lower kickback noise.

Diode-connected transistors are proposed as the loads of the input different pair. Firstly, they needn't switch between cutoff and saturation, avoiding large instantaneous current and large voltage variation at a_1/a_2. Thus, low kickback noise can be achieved. Secondly, the current flows through the load

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transistors M_{11}/M_{12} in Fig. 1 (c) during the whole clock period. The transistors M_{11}/M_{12} in Fig. 1 (b) are cutoff during half of the clock period. It looks like that the power dissipation would increase. Actually, when M_{11}/M_{12} cut off, M_5 and M_6 serve as the loads of the preamplifier, and hence there is still current in preamplifier. The power dissipation also remains. So the power dissipation in the proposed circuit doesn't increase in fact.

To ensure the small voltage variations at a_1/a_2, the load resistance of preamplifier should change as slightly as possible during the whole clock period. When clk is high, M_{11} and M_{12} serve as load and their resistances are defined as

$$R_{high} \approx \frac{1}{g_{m11,12}} \tag{2}$$

When clk is low, M_5 and M_{11}, M_6 and M_{12} are parallel connected as loads. The total load resistance is given as

$$R_{low} \approx \frac{1}{g_{m5,6} + g_{m11,12}} \tag{3}$$

So we design large $g_{m11,12}$ and small $g_{m5,6}$ to diminish the difference between R_{high} and R_{low} to reduce voltage variation at a_1/a_2. However, too large $g_{m11,12}$ may cause low gain of preamplifier, reducing the resolution and speed of the comparator. And, too small $g_{m5,6}$ would slow the latch. To make a compromise here, the size of M_{11}/M_{12} was about fourfold as that of M_5/M_6.

In addition, when clk is low, switch M_7 closes and V_{op} and V_{on} are reset. There will be ill-fitting voltage variation at a_1/a_2 with inconsistent V_{op} and V_{on}. Thus, proper size of M_3/M_4 and M_5/M_6 will be designed to ensure that the value of Vop and Von are close to the static operation point at a_1/a_2.

The dummy transistors M_{15} and M_{16} are added to offset the clock feedthrough effects, which makes voltage at a_1/a_2 vary suddenly when clk switches. The signal clk is coupled to the nodes a_1/a_2 through the gate-source capacitances of M_7/M_8 while the $\overline{clk}$ is coupled to a_1/a_2 through gate capacitances of M_{15} and M_{16}. According to

$$V_{clk}\frac{0.5W_{9,10}C_{ov}}{0.5W_{9,10}C_{ov} + W_{15,16}C_{ov}} - V_{clk}\frac{W_{15,16}C_{ov}}{0.5W_{9,10}C_{ov} + W_{15,16}C_{ov}} = 0 \tag{4}$$

where W and L is the width and length of MOS transistors, C_{ov} is gate overlap capacitance per width, and V_{clk} is the voltage amplitude of clk. The clock feedthrough effects can be minimized by setting $W_{15,16} = 0.5W_{9,10}$, $L_{15,16} = L_{9,10}$. Furthermore, the PMOS switch M_7 in Fig. 1 (b) was substituted to NMOS switch. So the NMOS switch can be controlled by $\overline{clk}$ and minimize the clock feedthrough effects.

When the source voltage of M_1/M_2 varies, preamplifier provides the charge current for the parasitic capacitance of M_1/M_2. Those charge currents will cause the kickback noise. As shown in Fig. 1 (c), two capacitances equal to the value of gate-source capacitance of M_1/M_2 are added to reduce the kickback noise. Because the currents are produced when the gate capacitance of M_{17}/M_{18} discharges, two capacitances equal to the gate-source capacitance of M_1/M_2 can be added to reduce the kickback noise as shown in Fig. 1 (c).

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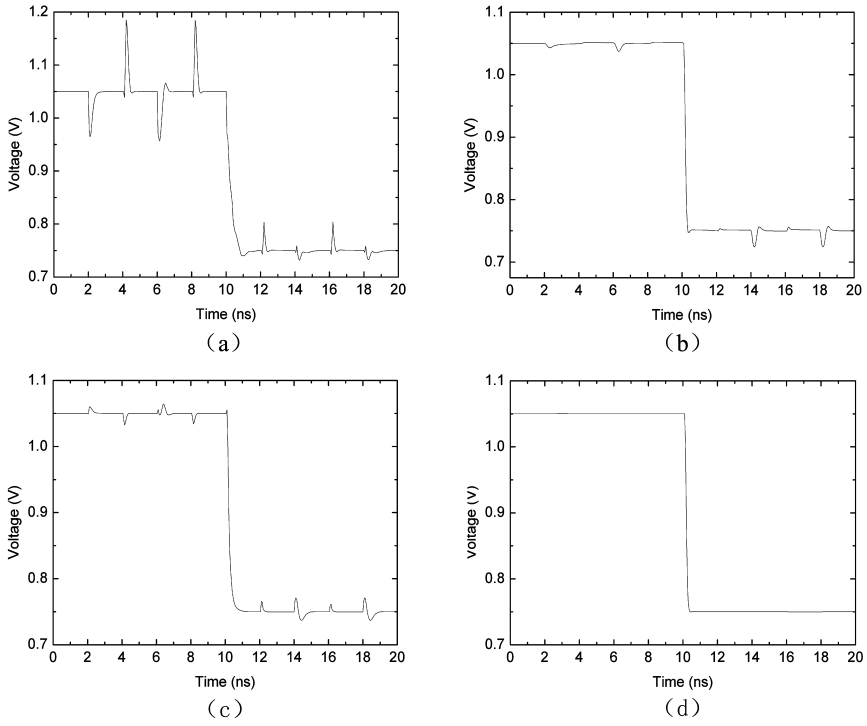

Fig. 2. The kickback noise from (a) the Fig. 1 (b) circuit, (b) improved circuit only use unilateralization technology, (c) improved circuit only use the load transistors independent with clock signal, (d) The proposed circuit

Table I. Summary of comparator's performances

	This work	[6]
Kickback noise(mV)	0.14	4
Power supply(V)	1.8	1.8
Power dissipation(μW)	202	268
Clock frequency(MHz)	250	200
Technology(μm)	0.18	0.18

3 Simulation results

The proposed comparator are simulated in 0.18-μm standard digital CMOS technology at 1.8 V supply voltage using HSPICE. The clock frequency is 250 MHz. The kickback noise is obtained by measuring the gate voltage of input transistors. An 8 kΩ resistance is inserted between the gates of input transistors and the signal source during the measurements.

The kickback noises in Figueiredo's circuit and ours are compared when the amplitude of input differential voltage is 300 mV. Fig. 2 (a) indicates that the comparator in the Fig. 1 (b) almost has no kickback noise during the regeneration phase. However, when clk is switching, it is still large kickback noise, about 136 mV. The kickback noise is about 25 mV only using unilateralization technique, as shown in Fig. 2 (b). The load transistors proposed here can also considerably reduce the kickback noise to 27 mV, as shown in

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Fig. 2 (c). Fig. 2 (d) shows the kickback noise in our proposed comparator. The value is just about 0.14 mV. It can be seen that the kickback noise was suppressed significantly here. Furthermore, the power dissipation of the whole comparator including the output latch is just about 202 μW. So, the circuit can work at lower supply voltage to improve the power efficiency further.

Table I summarizes a comparison on the performances with the comparator proposed by Figueiredo. According to simulation results of Hspice, our comparator can work at higher frequency but consume less power. Importantly, the kickback noise voltage is very low, just 4% of that of comparator in [6].

4 Conclusion

An improved low kickback noise and low voltage Class-AB latched comparator is discussed. The inputs and the regeneration nodes are isolated using the unilateralization technique. The source-coupled amplifier can work at low power supply. The load transistors independent with clock signal are introduced to avoid large instantaneous current. So the kickback noise is reduced significantly. In addition, the dummy transistors relieve the clock feedthrough effects and neutralization technique also helps to reduce further the kickback noise. According to simulation results, the comparator achieves a very low kickback noise voltage of 0.14 mV at the differential input voltage of 300 mV. Low power dissipation of 202 μW can be achieved at 1.8 V supply voltage while the clock frequency is increased to 250 MHz.

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