ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.11, No.9, 1–6

Extension method of tolerance to voltage and temperature variations in an injection-locked PLL

Jeonghoon Han[1a)], **Masaya Miyahara**[2], **and Akira Matsuzawa**[2]

[1] *Department of International Development of Engineering, Tokyo Institute of Technology, 2–12–1–S3–27 Ookayama, Meguro-ward, Tokyo 152–8552, Japan*

[2] *Department of Physical Electronics, Tokyo Institute of Technology, 2–12–1–S3–27 Ookayama, Meguro-ward, Tokyo 152–8552, Japan*

a) *hanjeonghoon@ssc.pe.titech.ac.jp*

Abstract: This article presents a method to enhance tolerance to voltage and temperature variations in an injection-locked PLL. The proposed method can enhance the tolerance to voltage and temperature variations by turning on or off a supplementary current source of the oscillator in the injection-locked PLL through the RC switch with a large time constant. This configuration increases the tolerance range to the supply voltage variation by 33.8%, compared to the conventional injection-locked PLL in [5]. The proposed method is verified by the calculation and simulations. They show that the PLL can maintain the stable lock state during the switching of the supplementary current source.

Keywords: voltage-temperature variations, tolerance, RC switch, ring oscillator, phase-locked loop

Classification: Integrated circuits

References

[1] Y. Kobayashi, S. Amakawa, N. Ishihara and K. Masu: European Solid-State Circuits Conference (2009) 440.

[2] J. Han, M. Miyahara and A. Matsuzawa: International Workshop on Millimeter Wave Wireless Technology and Applications (2010) 126.

[3] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara and K. Masu: IEEE Radio Frequency Integrated Circuits Symposium (2012) 189. DOI:10.1109/RFIC.2012.6242261

[4] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada and A. Matsuzawa: ISSCC Dig. Tech. Papers (2013) 248.

[5] J. Han, M. Miyahara and A. Matsuzawa: IEICE Trans. Electron. **E97-C** (2014) 316. DOI:10.1587/transele.E97.C.316

[6] F. M. Garder: *Phaselock Techniques* (Wiley-Interscience, New Jersey, 2005) 10.

[7] K. Shu and E. Sánchez-Sinencio: *CMOS PLL Synthesizers: Analysis and Design* (Springer, New York, 2005) 34.

[8] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa: Proc. A-SSCC (2008) 269. DOI:10.1109/ASSCC.2008.4708780

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014

1 Introduction

For the last few decades phase-locked loops (PLLs) have been remarkably developed to provide stable clock signals to various systems. Injection-locked ring oscillators and PLLs can achieve low phase noise performance [1, 2, 3, 4, 5].

The injection locked PLL in [5] has wide tolerance to wide supply voltage and temperature variations, which are 1.034–1.238 V of the supply voltage and 151.2 °C of the temperature variation in the simulations. Tolerance to the power supply voltage and temperature variations in the injection locked PLL almost depends on the coverage of the fine tuning range. In order to enhance the tolerance, the larger fine tuning range is required such that it results in larger oscillator gain and the larger chip area of the loop filter [6, 7]. Alternative method is to turn on a supplementary current source. However, abrupt change of the oscillation frequency due to turning on the supplementary current source will cause loss of lock and the PLL will suffer lock process again.

This article proposes a method to improve tolerance to voltage and temperature variations in the injection-locked charge pump phase-locked loop in [5] with relatively small area and low current consumption without loss of lock or re-lock process.

2 Extension of the tolerance to voltage and temperature (VT) variations in the PLL

The basic concept of extension of the tolerance to the VT variations is to turn on or off an supplementary current source, UP_{freq}, without interruption of the lock state in the PLL. Fig. 1 shows an injeciton-locked PLL with the VT variation compensator. When the supply voltage decreases or temperature increases, the oscillation frequency of the VCO decreases. When the oscilla-

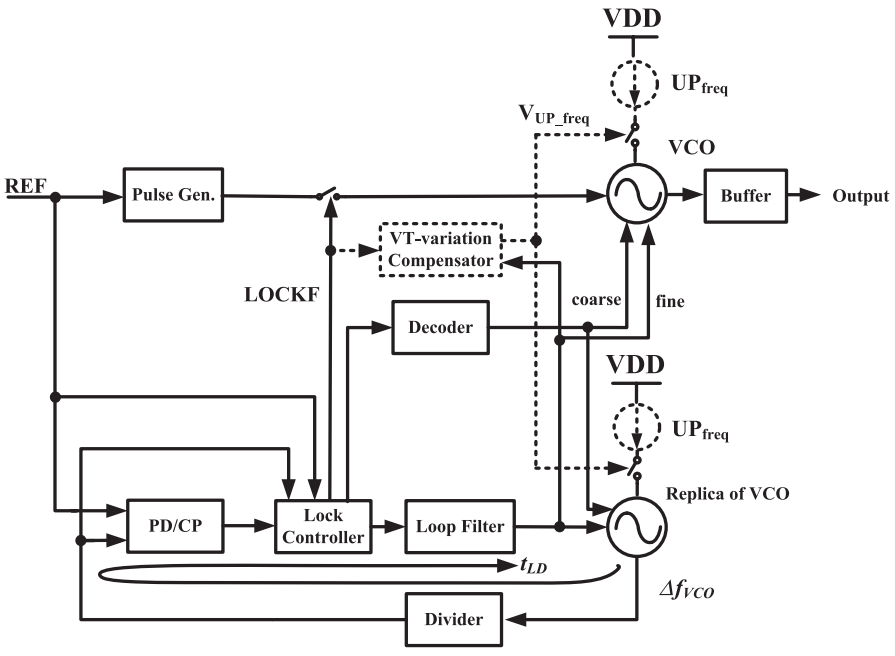

Fig. 1. Injection-locked PLL with the VT variation compensator.

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014

tion frequency changes by Δf_{VCO}, the PLL changes a control voltage by ΔV to compensate the deviation of the frequency after the loop delay time, Δt_{LD}. When the fine tuning coverage can not compensate the voltage supply drop, the PLL and the injection-locked oscillator will lose lock. The proposed method is to turn on an supplementary current source when the fine tuning voltage is out of the predetermined range. When the switching time to turn on the supplementary current is too short, the PLL will suffer lock procedure again. Meanwhile, when the switching time is long enough, the PLL can maintain the lock state to enhance the coverage of the VT variations. This method can be implemented by comparing between a fine tuning voltage and a certain reference voltage and turning on the supplementary current source through the switch with long switching time. The switch, called RC switch, is similar to a low pass filter composed of the large dynamic resistance of MOSFET and relatively small capacitor. The sample-and-holder and comparator compares the fine tuning voltage with the certain reference voltages.

3 Circuit configuration and operation

Fig. 2 shows a RC switch and a modified delay stage of the ring oscillator introduced in [5]. A supplementary current sources, $\mathrm{UP_{freq}}$, is used to compensate a drop of the oscillation frequency due to the supply voltage and temperature variations. Since the PLL is turned on, the coarse tuning code is selected and then the fine tuning operates. When the PLL is locked, the lock alarm, LOCKF, of the fine tuning is outputted and then the VT variation compensator starts to monitor the fine tuning voltage periodically with the sample-and-holder and comparator introduced in [8]. In order to prevent any disturbance to the PLL due to the sampling, the source follower is inserted between them.

When the supply voltage decreases and the VT variation compensator detects the predetermined voltage, $\mathrm{UP_{freq}}$ is turned on by the output voltage, $V_{UP_{freq}}$, of the RC switch. $V_{UP_{freq}}$ changes with the time constant, τ, of the RC switch.

$$V_{UP_{freq}}(t) = VDD \cdot e^{-t/\tau} \tag{1}$$

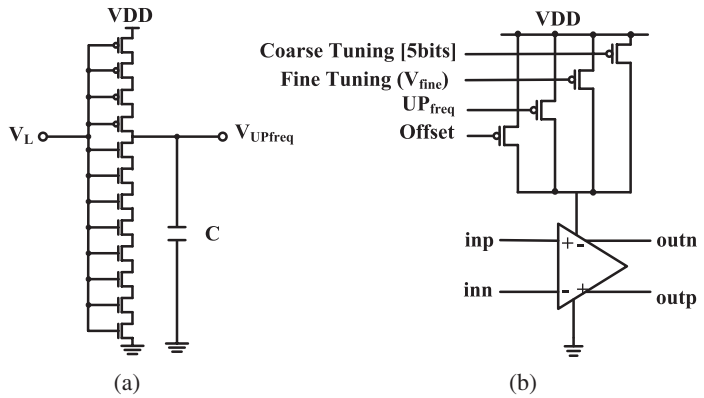

Fig. 2. (a) RC switch (b) delay stage of the ring oscillator.

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014

where VDD is the supply voltage. The reference voltage of the comparator is changed to prepare when the supply voltage is recovered. When the supply voltage is recovered, $\mathrm{UP_{freq}}$ will be turned off.

When $\mathrm{UP_{freq}}$ is turned on, the frequency of the oscillator is increased by the $\Delta f_{VCO\_UP}(t)$. When the oscillation gain, K_{VCO_UP}, of $\mathrm{UP_{freq}}$ is modeled to have a positive value, $\Delta f_{VCO\_UP}(t)$ is

$$\Delta f_{VCO\_UP}(t) = K_{VCO\_UP} \cdot (VDD - V_{UP_{freq}}(t)) \tag{2}$$

Since K_{VCO_UP} also depends on the $V_{UP_{freq}}$, it can expressed as follows:

$$K_{VCO\_UP}(t) = \mathrm{K_{VCO\_UP'}} \cdot (VDD - V_{UP_{freq}}(t)) \tag{3}$$

Thus, the incremented oscillation frequency, Δf_{VCO_UP}, by $\mathrm{UP_{freq}}$, is

$$\Delta f_{VCO\_UP}(t) = \mathrm{K_{VCO\_UP'}}\, VDD^2(1 - e^{-t/\tau})^2 \tag{4}$$

$$= \Delta f_{VCO\_UP\_MAX}(1 - e^{-t/\tau})^2 \tag{5}$$

where $\Delta f_{VCO\_UP\_MAX}$ is the maximum incremented frequency. Moreover, the frequency variation by $\mathrm{UP_{freq}}$ can be converted to the equivalent phase variation, $\Delta\Phi_{VCO\_UP\_MAX}$, which is

$$\Delta\Phi_{VCO\_UP}(t) \approx \Delta\phi_{VCO\_UP\_MAX}(1 - e^{-t/\tau})^2 \tag{6}$$

where $\Delta\phi_{VCO\_UP\_MAX}$ is the maximum phase variation with respect to the phase of the oscillation frequency. When a 3rd-order loop filter in the PLL is modeled as $(sk_3 + 1)/(s^3k_2 + s^2k_1 + sk_0)$, the phase variation in the oscillator, $\Delta\Phi_{VCO}$, and can be obtained as follows:

$$\Delta\Phi_{VCO}(s) \approx \frac{s^2k_1 + sk_0}{s^2k_1 + s(k_0 + K \cdot k_3) + K}\,\Delta\Phi_{VCO\_UP}(s) \tag{7}$$

where K is $I_{CP}K_{VCO}/N$, I_{CP} is the current of the charge pump, K_{VCO} is the oscillator gain, and N is the division ratio. From the above equations, the phase variation of the oscillator due to $\mathrm{UP_{freq}}$ can be calculated and then converted to the frequency variation, $\Delta f_{VCO}(t)$.

4 Simulation results

Fig. 3 and 4 show the simulation results of the compensator for voltage and temperature variations. The capacitance of the RC switch is 20 pF and all MOS sizes are the channel length of 300 µm and width of 300 nm as shown in Fig. 2(a). Its equivalent resistance is 0.66–0.9 MΩ and the loop bandwidth of the PLL is 480 kHz when the supply voltage is about 1.08 V and Vfine is 0.2 V. The channel width of $\mathrm{UP_{freq}}$ is a half of the fine tuning current source. When the clock for monitoring is 1 MHz, the total current consumption is 102.4 µA. Since the supply voltage does not drop in a short time, the monitoring period can be selected to be more lower frequency. Without the RC switch as shown in Fig. 3, the control voltage for the supplementary current source abruptly changes from VDD to ground and then the PLL suffers re-lock procedure. However, the PLL with the RC switch maintains the normal lock state. The tolerance to the supply voltage variation is 0.987–1.26 V. It occupies 22.8% of the regular supply voltage, 1.2 V.

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014

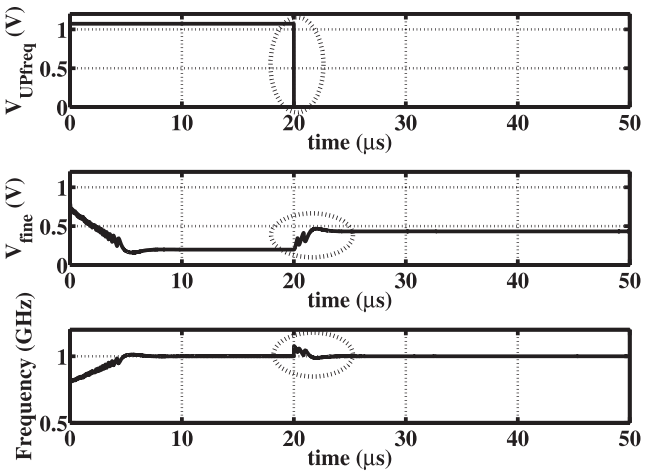

Fig. 3. Simulation results in the case of without the RC switch.

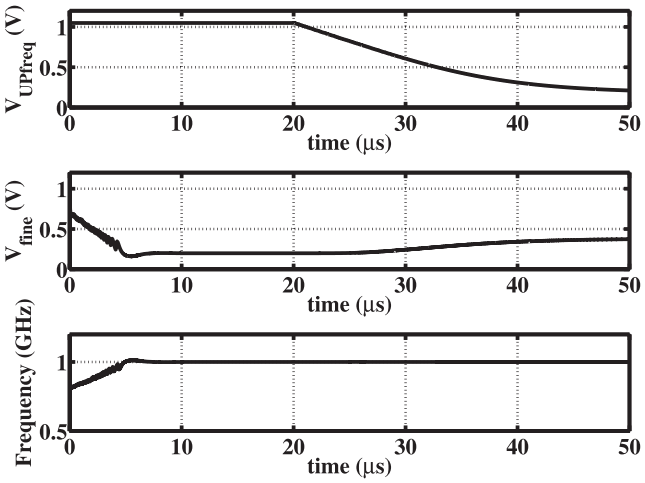

Fig. 4. Simulation results in the case of with the RC switch.

Fig. 5 and 6 show the calculation result of Δf_{VCO} and the the comparison between the calculation and simulation results when the oscillation frequency is 1 GHz, respectively. When the capacitances of the RC switch are 10, 15, 20, and 25 pF, the time constants are 6.6, 9.9, 13.2, and 16.5 μsec, respectively. The large difference between them is considered to be mainly due to the relatively low accuracy caused by tolerances in the simulation. It is hardly to simulate the PLL for long time with high accuracy. The simulation results show the maximum deviation of the output frequency is below 470 kHz when C = 20 pF. Thus, the injection locked PLL can maintain the lock state during the compensation.

It is also possible to obtain the same effect through the increase of sizes of the fine tuning range. It results in the increase of the oscillation gain and the additive capacitance about 100 pF is required for the loop filter. Thus, this method can achieve the extension of the tolerance to voltage and temperature variations with relatively small area and low current consumption.

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014

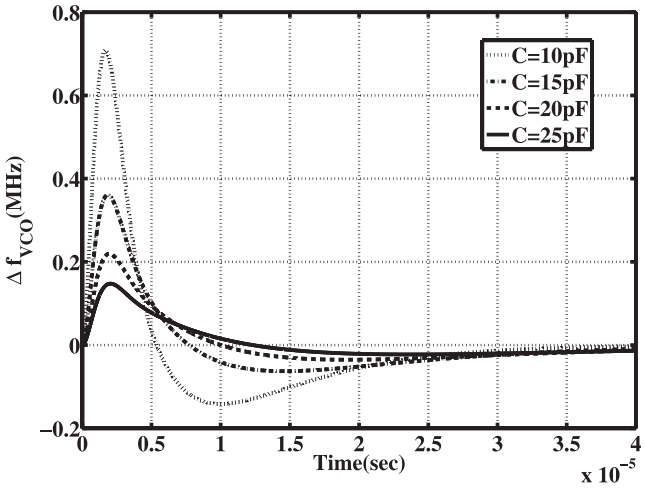

Fig. 5. Calculation results of Δf_{VCO}.

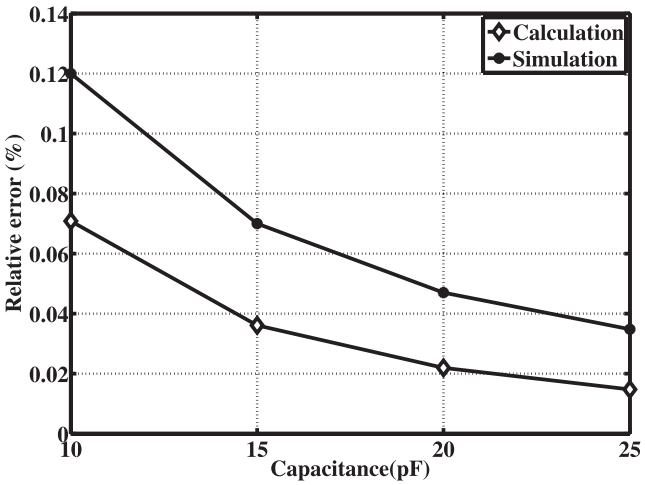

Fig. 6. Comparison between the calculation and simulation results.

5 Conclusion

The configuration proposed in this paper can provide the PLL with extension of tolerance to voltage and temperature variation. The tolerance range to supply voltage variation is 0.987–1.26 V with the regular supply voltage of 1.2 V and is thus increased by 33.8%, compared to 1.034–1.238 V in the conventional injection-locked PLL in [5]. Tolerance to temperature variation is considered to be enhanced by the same proportion when the supply voltage is not changed. Moreover, it can achieve it with relatively small area and low current consumption.

DOI: 10.1587/elex.11.20140127
Received February 12, 2014
Accepted March 14, 2014
Publicized April 17, 2014
Copyedited May 10, 2014