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Variable gain current mirror for high-speed applications

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Abstract: This paper presents a new high speed current mirror with continuous gain adjustment. Based on this current mirror, a variable gain current amplifier is designed in 0.18 μm CMOS technology. The current gain of the amplifier can be continuously varied from 0 dB to 20 dB while the bandwidth of the circuit remains above 100 MHz. The circuit consumes 0.9 mW from 1.5 V supply.

Keywords: CMOS, current mirror, current amplifier, tunable gain

Classification: Integrated circuits

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1 Introduction

Current mirrors are the basic building block of current-mode circuits, suitable for low-voltage high-speed analog signal processing [1]. Conventional CMOS current mirrors are not programmable and have a constant current gain which

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is defined by aspect ratios of comprising MOS transistors (Fig. 1 (a)). A variable-gain current mirror finds vast applications in a variety of circuits such as automatic gain control (AGC) [2], tuning of continuous time filters [3], trimming of precision analog circuits [4] and many more.

Different methods for designing a variable-gain current mirror have been reported in the literature [2, 3, 4, 5, 6]. The methods presented in [2, 3, 4] introduce level shifters in the signal path. This not only increases the minimum supply voltage of the circuit by about one threshold voltage (compared to a conventional current mirror) but also degrades the frequency response of the circuit. In [5] floating gate MOS transistors are used for programming the gain of the current mirror. However, this method suffers from complexity in the implementation and also limited tuning range. The method in [6] is suitable for low-voltage and high-speed applications but it is designed for a special form of input current and in general, linearity of the output current is degraded.

This paper presents a current mirror in which the current gain can be continuously changed. No additional nodes are introduced in the signal path and bandwidth of the circuit is close to that of a conventional current mirror which is potentially high. The circuit is also suitable for low-voltage applications and the minimum supply voltage is the same as for the conventional cascode current mirrors.

2 Circuit Description

The proposed circuit is based on the conventional cascode current mirror shown in Fig. 1 (a). The circuit in Fig. 1 (a) has a constant current gain of N. In order to introduce gain variability, the circuit is modified as shown in Fig. 1 (b). The current in the transistor M_5 of Fig. 1 (b) can be adjusted by changing the control voltage, V_C. Thus, the drain current of M_1 and M_2 will be a function of V_C as well. The role of the cascode transistors M_4 and M_6 in Fig. 1 (b) is to make the drain-source voltage of M_1 and M_2 equal. Therefore W/L of M_4 and M_6 is N times larger than that of M_3 and M_5, respectively. There is no special constraint on V_B and as in the cascode current mirror, V_B is selected such that no transistor goes into triode region.

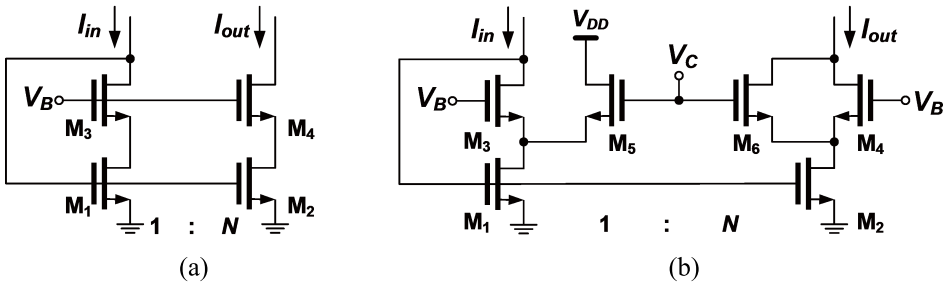

Fig. 1. (a) Conventional cascode current mirror, (b) Proposed variable-gain current mirror.

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To preserve the linearity of the current mirror, the size of M_3 and M_5 must be selected such that these two transistors operate in the weak inversion region. In the weak inversion region, the relation between drain current and gate-source voltage is [7]

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}}{nkT/q}\right). \tag{1}$$

where W denotes the channel width, L is the channel length of the transistor, k is the boltzmann constant, T is temperature and q is electron charge. I_0 and n are technology dependent parameters. The current in M_5 can be determined as follows.

From Fig. 1 (b) we can write

$$V_B - V_{GS3} = V_C - V_{GS5}. \tag{2}$$

With respect to (1), equation (2) can be written as

$$\frac{nkT}{q}\left(\ln\frac{I_{D5}}{I_0 W_5/L_5} - \ln\frac{I_{D3}}{I_0 W_3/L_3}\right) = V_C - V_B. \tag{3}$$

Then the current in M_5 can be derived as

$$I_{D5} = I_{D3}\frac{W_5/L_5}{W_3/L_3}\exp\left(\frac{V_C - V_B}{nkT/q}\right). \tag{4}$$

The output current, which is N times the current in M_1, can then be found as

$$I_{out} = N\left[1 + \frac{W_5/L_5}{W_3/L_3}\exp\left(\frac{V_C - V_B}{nkT/q}\right)\right] I_{in} = A_i I_{in}. \tag{5}$$

The current gain, A_i, is an exponential function of the V_C. The minimum gain of the circuit is N which is set when V_C is sufficiently lower than V_B. Current gain is increased by increasing V_C but to keep both M_3 and M_5 in weak inversion region, $V_C - V_B$ must be lower than about 0.15 V. When $V_C - V_B$ is larger than 0.15 V, the relation between I_{D3} and I_{D5} is no longer linear and output current will be distorted. This translates into more than two decades tuning range for the gain. Since parameter n in (5) is about 1.5 in our 0.18 μm process, we have a varying A_i in the range of N to $N(1 + 55W_5L_3/W_3L_5)$ for $(V_C - V_B) < 0.15$ V.

Considering the frequency response of the circuit, parasitic capacitances are the same as the circuit in Fig. 1 (a) except for parasitic capacitances at the source of M_3 and M_4. The increased parasitic capacitance at these two nodes has little influence on the bandwidth of the circuit, which is dominantly determined by the gate-source capacitances of M_1 and M_2.

In order to demonstrate the performance of the circuit, a fully differential current amplifier was designed as shown in Fig. 2. Transistors are sized as

$$\frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{W_{13}}{L_{13}} = \frac{W_{15}}{L_{15}}. \tag{6}$$

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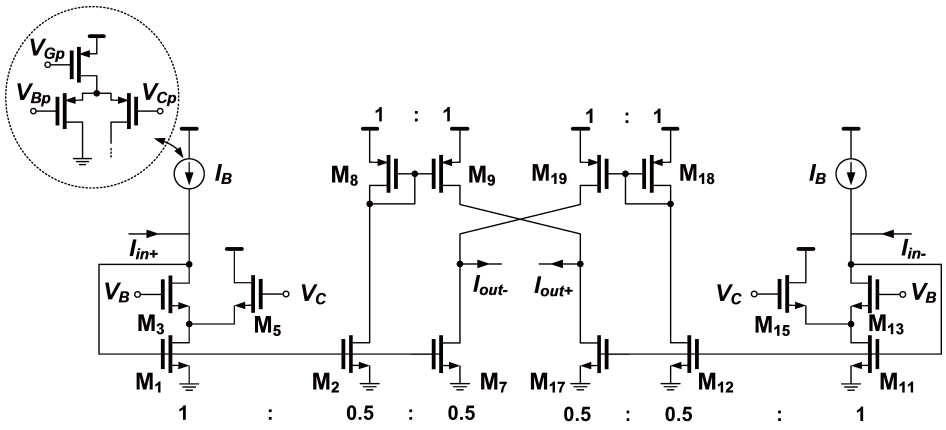
Cascode transistors for M_2, M_7, M_{12} and M_{17} are not shown for simplicity. PMOS current mirrors ($M_{8\text{-}9}$ and $M_{18\text{-}19}$) are used to set output common-mode level to zero. Output currents of the circuit are given by

$$I_{out+} = A\frac{I_{in+} - I_{in-}}{2} \qquad \text{and} \qquad I_{out-} = -A\frac{I_{in+} - I_{in-}}{2} \tag{7}$$

where current gain, A, is

$$A = 1 + \exp\left(\frac{V_C - V_B}{nkT/q}\right). \tag{8}$$

As in a conventional current amplifier, the minimum value of the bias current (I_B in Fig. 2) is determined by the maximum amplitude of the input current. Also, the bias current in the output transistors ($M_{7,9}$ and $M_{17,19}$) increases proportional to the gain of the circuit. If high current gains are only used when input level is small, considerable power saving can be achieved by adjusting I_B such that for large gains, I_B is automatically reduced. As shown in Fig. 2, bias current sources (I_B) are adjustable through changing V_{Cp}. In the designed circuit, V_{Cp} tracks the variation of V_C using a simple (common drain) level shifter. Hence, the bias current in $M_{1,2,7}$ (and $M_{11,12,17}$), and consequently power consumption of the circuit, remains almost constant for all values of the current gain A. However, a reduction in the bandwidth is the price for this power saving technique that one may not choose.



Transistor	M_1	$M_{2,7}$	$M_{3,5}$	$M_{8,9}$	Bias	$I_B(\mu A)$	$V_B(V)$
$\frac{W}{L}$	$\frac{16\mu}{0.5\mu}$	$\frac{8\mu}{0.5\mu}$	$\frac{36\mu}{0.18\mu}$	$\frac{16\mu}{0.25\mu}$	Value	20-80	0.95

Fig. 2. Fully differential variable-gain current amplifier

3 Simulation Results

The current amplifier of Fig. 2 was designed in 0.18 μm CMOS process. The input/output characteristic of the amplifier derived from HSPICE simulations using BSIM3v3 model is shown in Fig. 3 (a). The input/output relation is well linear and current gain can be changed from 0 dB to 20 dB by increasing V_C from 0.75 V to 1.05 V. The frequency response of the circuit is

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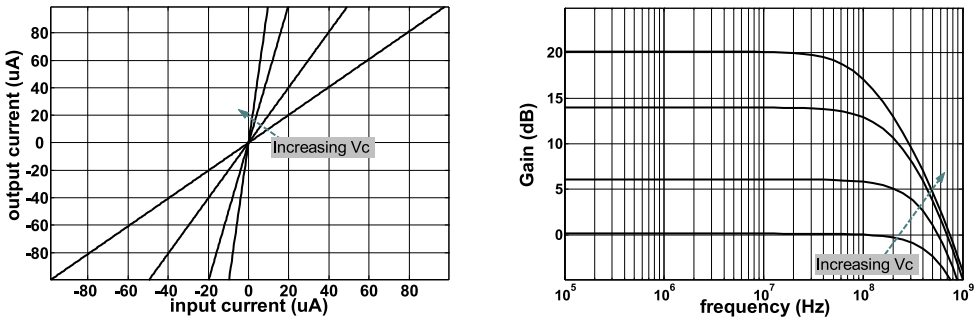
also shown in Fig. 3 (b). The −3 dB bandwidth of the circuit is higher than 100 MHz for differential gains up to 20 dB. The current gain can be increased to more than 40 dB by increasing V_C, however, the bandwidth would decrease accordingly.

Considering the step response, the worst case settling time (to 1% of the final value) of the output for a gain of 20 dB was found to be 12 ns. Total output noise of the amplifier in 100 MHz bandwidth is 0.08 μA_{rms} at 0 dB gain and 0.17 μArms at 20 dB gain. The maximum current consumption of the circuit is 600 μA and supply voltage of the circuit can be as low as 1.3 V.

The linearity of the circuit was also tested. At each gain setting, the input amplitude was selected so as to obtain output amplitude of 100 μApp. With a 10 MHz input sinusoid, the total harmonic distortion (THD) is −67.9 dB for a gain of 0 dB and −55.7 dB at the gain of 20 dB. The degradation in THD is due to deviation of I/V characteristic of MOS transistors from the weak inversion exponential relation given in (1).



(a) (b)

Fig. 3. (a) Transfer characteristics at different gains, (b) Frequency response at different gains.

4 Conclusion

A new high-speed and low-voltage variable-gain current mirror was presented and a fully differential current amplifier was designed and simulated based on the proposed current mirror. A tuning range of 20 dB for the current-gain, with a bandwidth of 100 MHz demonstrates the potentials of the proposed circuit for high-speed applications. The minimum supply voltage of 1.3 V in 0.18 μm CMOS process shows that the circuit is also well suited for low-voltage applications.

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