

Precise time-difference repetition for TDC with delay mismatch cancelling scheme

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Abstract: This paper presents a precise time-difference repetition technique to enhance the timing accuracy in repetition based time-to-digital converters (TDC). In the proposed scheme, any delay mismatches during timing difference repetition process can be removed. The proposed circuit could be used for multi-step TDC, delta-sigma TDC, and SAR-type TDC. The proposed scheme was designed and simulated with a 65-nm CMOS process. The proposed circuit shows a delay variation of about 100 fs in the presence of device mismatches, which is much less than that of conventional approaches. The input time range and the conversion rate is 480 ps and 100 Msps if applied to a 2-step TDC, respectively.

Keywords: time-to-digital converter (TDC), time amplifier (TA), successive approximation register TDC (SAR-TDC), digital PLL, delay mismatch

Classification: Integrated circuits

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1 Introduction

In order to increase the timing resolution in time-to-digital converters (TDC), various designs had been reported [1, 2, 3, 4, 5, 6]. Time amplification in a multi-step TDC [3, 4, 5, 6], time accumulation in a noise shaping TDC, and successive approximation TDC [2] are design examples for the better timing resolution.

Another approach to increase timing resolution is using a delay repetition method. Fig. 1 demonstrates how the delay repetition increases the number of conversion bits in TDC. As shown in Fig. 1(a), a cyclic SAR TDC can be designed by successive approximation of the time difference [2]. Two signal paths (INA, INB) are controlled and the delayed signals are compared. This process can be repeated in the cyclic loop and the repeating measurement makes the successive approximation process possible. The delay repetition also can amplify the timing difference of two input signals. A pulse-train amplifier used in a multi-step TDC is described [3]. As shown in Fig. 1(b), the pulse-train amplifier repeats a pulse generated by the timing difference of two inputs. The repeated pulse operates as EN (enable) signal in each gated delay cell. During the conversion period the SET signal is high and the received SET pulse in the gated delay cells is transferred whenever the EN is high. The falling edge of SET samples each node of the gated delay cells so that the total pulse width can be converted to additional digital bits. Since the pulse repetition method makes the time amplification rather simple, the pulse-train time amplifier shows the higher linearity and the wider input time range than the other approaches [4, 5, 6].

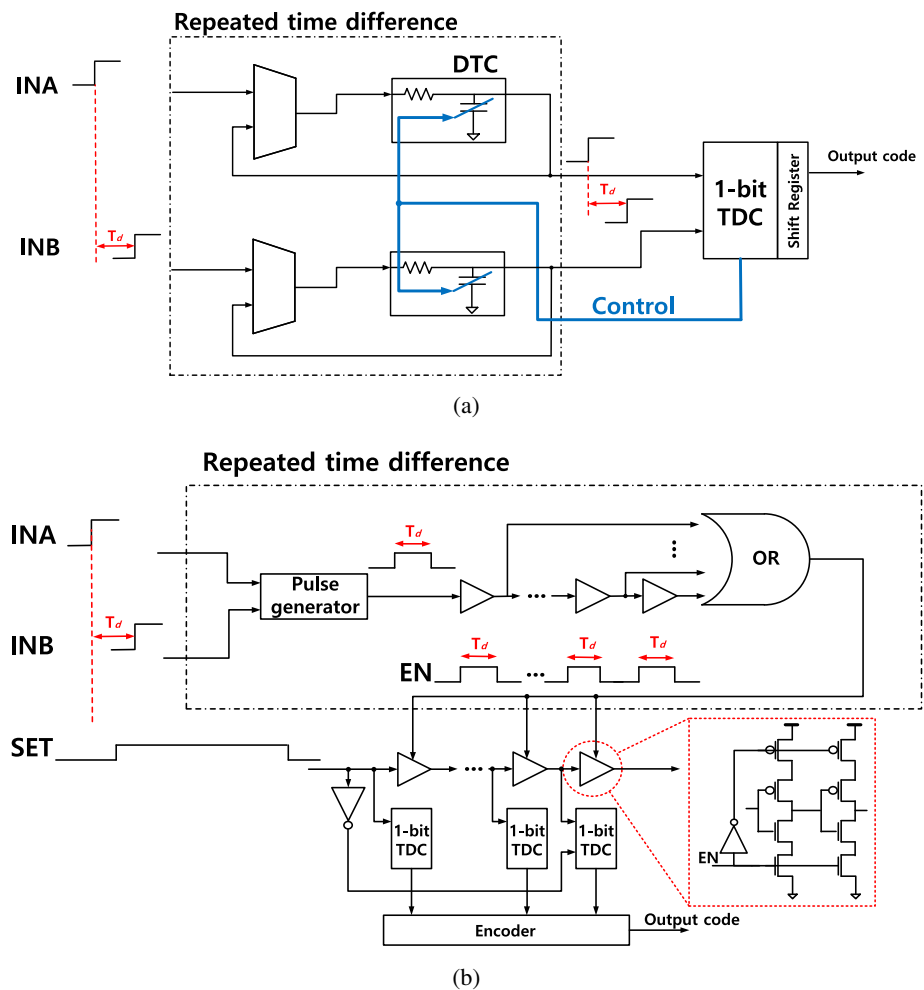


Fig. 1. Examples of repetition based approaches in TDC: (a) Repeated time-difference measurement in a cyclic SAR TDC [2] (b) Pulse-train amplifier in a 2nd step TDC [3]

Therefore the repetition of timing difference is the key function to improve the time resolution in TDC. The more accurate time difference repetition technique guarantees the higher resolution in multi-step or SAR-type TDC. The SAR TDC requires the less number of repetitions for the same number of conversion bits compared with the time amplifying TDC. For example, successive approximation for 4-bit needs 4 times repetition, in contrast to that the time amplification needs 16 times of that for the same bits. Fewer repetitions accumulate less random and deterministic jitter, which could produce more accurate output codes. However, the different paths of both input signals cause delay mismatch, which accumulates a time offset in repeated time difference. Fig. 2(a) illustrates that the different cyclic signal paths through digital-to-time conversion (DTC) and TDC accumulate the time offset and as a result the accuracy of SAR TDC could be decreased. The repetition using the timing pulse approach can also be affected by delay mismatches in the buffer chain and threshold variation in the logic path as shown in Fig. 2(b) if devices are not identical.

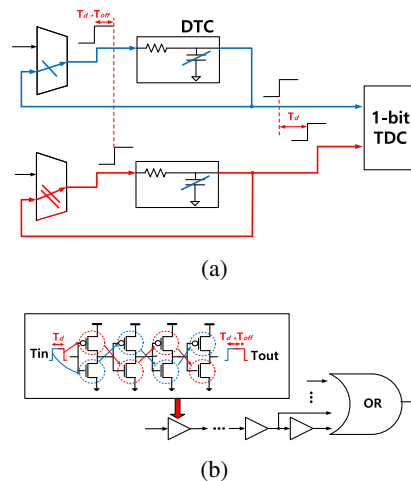


Fig. 2. Possible time-difference distortion by delay mismatch in the conventional approaches: (a) cyclic signal path mismatch in cyclic SAR TDC, (b) pulse signal path mismatch due to delay mismatches in the buffer chain

This paper proposed an accurate time-difference repetition (TDR) circuit. The proposed time-difference repetition circuit is able to cancel any delay mismatches during the time-difference repeating process. It also could be used as a time register by storing the time information in the loop.

2 The proposed time-difference repetition (TDR) circuit

Fig. 3(a) shows the structure of the proposed time-difference repetition circuit. With this proposed circuit, the delay mismatches are cancelled since two different timing signal paths are eventually going through the same delay buffers. Whenever the delay mismatch reaches a halfway point, it is cancelled automatically at the next halfway point. It is symmetrical and includes even number of buffer stages, repetition controllers, a time window filter, repetition counter, and dummy circuit.

The entries for the input signals (INA and INB) are different from each other. Therefore, the signals do not interfere with each other in spite of a fine timing difference. This approach also makes it possible to repeat the time difference without generating a timing pulse. The total delay of the buffer chains in TDR is more than 4 times the input time-difference range. The actual number of buffers to be used for repetition is not affected by the repetition number or gain, in contrast to the conventional pulse-train architecture. The structure of the repetition controller is shown in Fig. 3(b). The repetition controller has three different states, which include reset mode, input entering mode, and repetition mode. When EN is low, the circuit is in its initial conditions with Oscil_A and Oscil_B being “0” for reset mode. When EN goes to high, the input entering mode starts, and the input pulses pass through each multiplexer. After the delay in the input time range, nodes X and

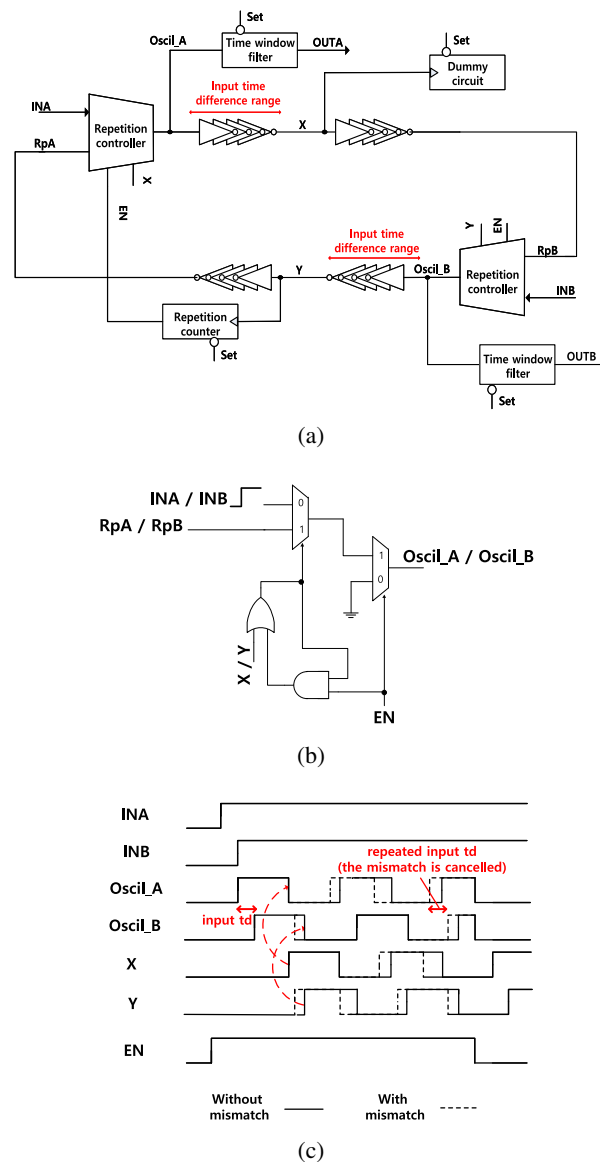


Fig. 3. The proposed time-difference repetition (TDR) circuit: (a) Block diagram of the proposed TDR circuit, (b) Repetition controller, (c) Time-difference repeating process by repetition controller

Y are turned on, which changes the state of TDR to repetition mode. The repetition mode does not change until the EN changes to low. To filter out redundant pulses, a time window circuit is added. Fig. 3(c) shows the time-difference repeating process in detail.

The proposed scheme repeats the time difference without delay mismatch and stores the time information more precisely than in other approaches. By circulating the two timing signals around the same delay buffer loop, the delay mismatches are cancelled. Therefore the proposed TDR can also be used as an accurate time register. The charges in capacitors are also used for accumulating the time information [4]. However, these approaches have distortions affected by charge redistribution and charge injection. In contrast, the proposed scheme stores time information without using the charges in capacitors.

Because the TDR creates repetition by letting both input signals circulate around the loop, there are redundant pulses that pass around only half of the loop. Time window filter is used for removing these pulses. As shown in Fig. 4(a), both falling edges of Oscil_A and Oscil_B switch the control signal of the MUX to eliminate the unwanted pulses. Fig. 4(b) describes the filtering out process of time window filter. The time difference output (t_d) is repeated in OutA and OutB while EN is high. The successive approximation in TDC is possible when it uses the repeated time difference output (t_d). Besides, adding or accumulating the time difference output (t_d) in a fixed number of times could make the time amplification or noise shaping. The repetition counter described in Fig. 5 counts the number of times that the pulse circulates around the loop. If the repetition number equals the intended number, “done” rises in the N_counter to switch the TDR to the reset mode.

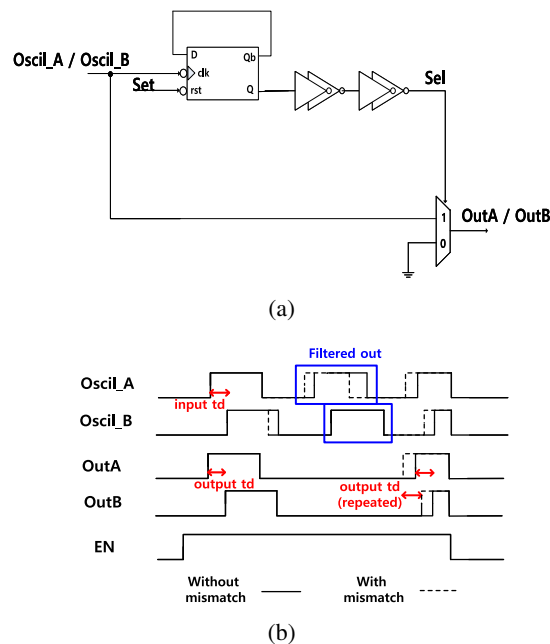


Fig. 4. The structure for the other sub-blocks of the TDR circuit: (a) Time window filter and (b) Operation of filtering out redundant pulses

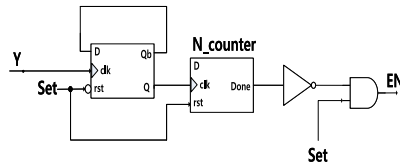


Fig. 5. Repetition counter

3 Simulation results

The proposed TDR circuit is designed for the 65-nm CMOS process. To verify the delay mismatch cancellation effect, we simulated the time-difference distortion while varying the size of the pMOS transistors intentionally to cause delay mismatch. The simulation verified that the output time-difference variation always remains within 100 fs, while the conventional scheme exhibits a 100 ps time-difference variation. To check the variation in the time difference between the

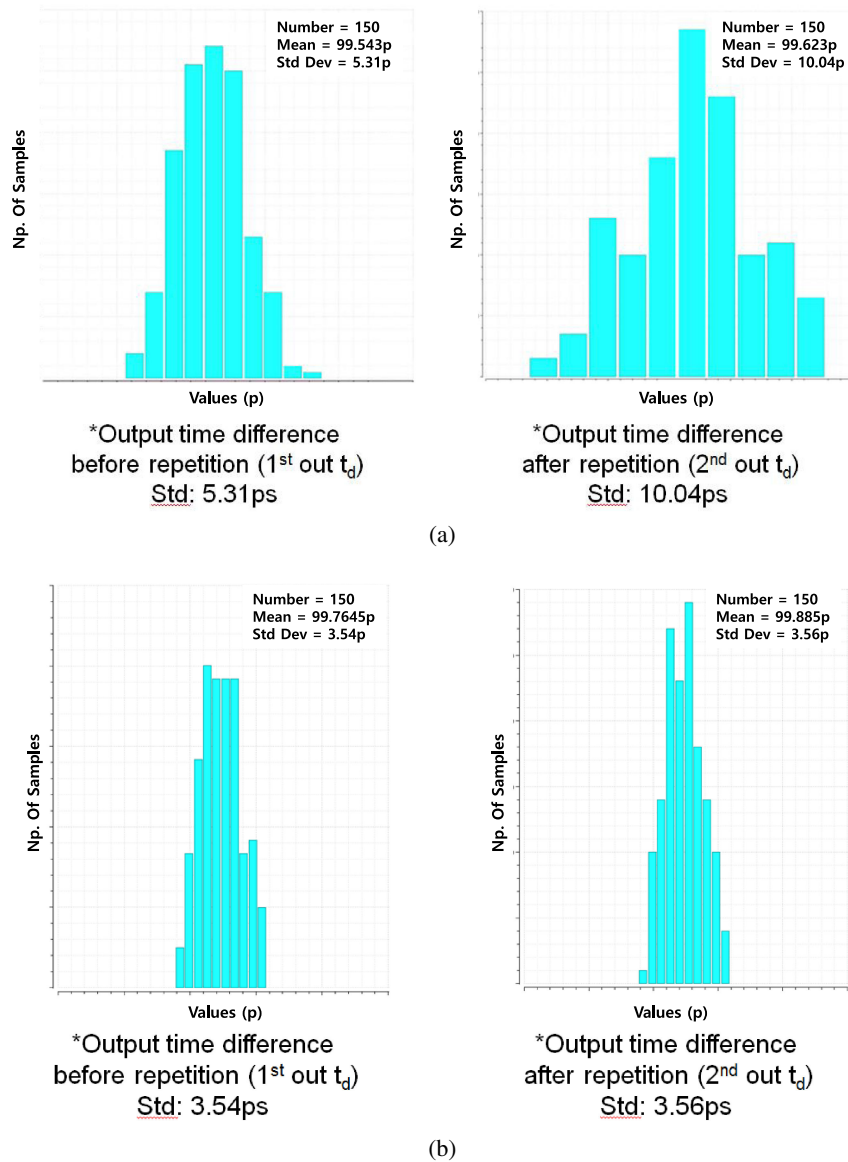


Fig. 6. Monte-Carlo simulation results to check delay variation: (a) Conventional pulse-train scheme, (b) Proposed TDR scheme

input and the repeated output, a Monte-Carlo simulation was performed at 150 counts. Fig. 6 shows the first (left side) and repeated (right side) distributions of the output time difference t_d . The standard deviation of the accumulated deterministic jitter (= time offset) varies by 0.02 ps (3.54 ps~3.56 ps), as shown in Fig. 6(b). This contrasts with the conventional approach, which has an increase of 4.69 ps (5.31 ps~10.04 ps) in the standard deviation, as shown in Fig. 6(a). Both results demonstrate the effectiveness of the proposed design. As described in Table I, the difference in distortion between the pulse-train and TDR grows with the number of pulse repetition. Our circuit eliminates the deterministic jitter in the loop. Accumulation of random jitter is another factor affecting the accuracy of TDC. Because the reset mode initializes accumulated jitter in the loop at every conversion, the random jitter accumulation is mostly affected by the length of delay path rather than the cyclic loop structure. The accumulated rms random jitter of our proposed TDR will be about 2 times as much as the conventional pulse-train scheme due to its 4 times longer delay path for a repetition cycle. However, since the accumulated random jitter caused by flicker and thermal noise contributes very small portion to total jitter, the proposed TDR shows the much smaller delay distortion compared to the pulse-train approach in ref. [3] under the same repetition process as shown in Table I.

Table I. Summary and comparison result from simulation (@20 MHz, 100 ps input t_d)

	Previous approach [3]		Our work	
Process	65 nm		65 nm	
Supply voltage	1.2 V		1.2 V	
	t_d distortion @last repetition	Power dissipation (Increment rate to 2× repetition)	t_d distortion @last repetition	Power dissipation (Increment rate to 2× repetition)
2× repetition	10.04 ps rms	13.53 μ W(1×)	3.56 ps rms	75.12 μ W(1×)
4× repetition	55.06 ps rms	60.50 μ W(4.4×)	4.22 ps rms	123.42 μ W(1.6×)
8× repetition	69.16 ps rms	274.32 μ W(20.3×)	5.34 ps rms	309.96 μ W(4.1×)

Additionally, the power dissipation of the conventional approach increases dramatically as increasing the repetition times. In comparison, the power consumption increment rate is much lower when the repetition count is increased in the proposed method. The proposed circuit operates at 500 M repeats per a second. In contrast to the conventional pulse train TA approach, the proposed scheme does not require additional buffers to increase the repetition gain.

With controlled power consumption in higher repetition and the less distorted output, our repetition technique shows an input time range of 480 ps and an estimated conversion rate of 100 Mbps if applied to the same 2-step TDC in ref. [3]. Compared to the repetition based time amplification in ref. [3], the conversion rate could be lower due to the required repeating duration time. However, compared with the latch-based time amplification schemes [5, 6], our approach shows the better performance as summarized in Table II.

Table II. Comparison of 2-step TDC using time amplification

	[3]	[5]	[6]	Our approach*
Time amplification scheme	Repetition based	Latch based	Latch based	Repetition based
Process	65 nm	90 nm	130 nm	65 nm
Input time range (T_{FS})	480 ps	640 ps	160 ps	480 ps
Conversion rate	200 Msps	10 Msps	100 Msps	100 Msps
# of bits	7	9	7	7

*Estimated values.

4 Conclusion and future work

A time-difference repetition circuit that includes a delay mismatch cancellation technique has been presented. By sharing signal paths, the delay mismatch can be cancelled during the repeating of the time difference. Also, the time-difference repetition could be used as a time register. The proposed circuit was designed and simulated in a 65 nm CMOS process and the simulation result shows a delay variation of about 100 fs with Monte-Carlo simulations. The input time range and the conversion rate is 480 ps and 100 Msps if applied in a 2-step TDC, respectively.

The proposed TDR can be used in various time-to-digital converters such as pipelined TDC and SAR TDC. The cyclic SAR TDC architecture applying the proposed TDR is shown in Fig. 7. The proposed TDR can be used as a time register, which repeats the time difference between INA and INB for successive measurement. It does not accumulate a time offset caused by the repetition path.

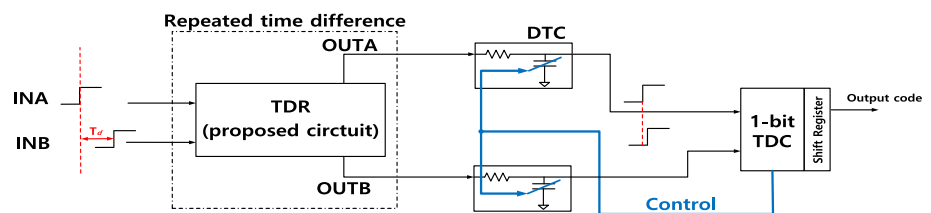


Fig. 7. Architecture of a cyclic SAR TDC including proposed TDR

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