ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.2, 1–6

Power switch implementation for low voltage digital circuits

Kyung Ki Kim[a)]

School of Electronic Engineering, Daegu University, Gyeongsan, 712–714, South Korea

a) *kkkim@daegu.ac.kr*

Abstract: This letter presents a novel power switch structure using only low threshold voltage MOSFETs to extend the power switch to ultra-low voltage region. The proposed structure deploys series-connected low-Vth footers with two virtual ground ports and selectively chooses the logic cells for connecting to each virtual ground port according to the delay criticality. Moreover, additional circuitries are designed to reduce not only sub-threshold leakage current, but also gate-tunneling leakage and to reduce wake-up time and wake-up fluctuation compared to the conventional power switch. The total power switch size of the proposed power switch structure including the additional circuits is less than the conventional one. The simulation results show that the proposed power gating structure has advantage of low leakage power, small footer size, and low wake-up time, but high-performance, low wake-up fluctuation, wake-up power for inverter chains and ISCAS85 benchmark circuits at 1.1 V and 0.6 V VDD which are designed using 45 nm CMOS technology.

Keywords: power switch, power gating, leakage power

Classification: Integrated circuits

References

[1] K. Shi and D. Howard, "Challenges in sleep transistor design and implementation in low-power designs," *IEEE DAC*, pp. 113–116, July 2006.

[2] K. Min and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Scheme with Self-Saturated Virtual Power Lines for Subthreshold-Leakage-Suppressed Sub-l-V-VDD LSI's," *ESSCIRC*, pp.679–682, 2002.

[3] S. Kim, C. Choi, D. Jeong, and S. V. Kosonocky, "Reducing ground-bounce noise and stabilizing the data-retention voltage of power-gating structure," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 197–205, Jan. 2008.

[4] S. Kim, S. Kosonocky, D. Knebel, et al., "A multi-mode power gating structure for low-voltage deep-submicron CMOS ICs," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 7, pp. 327–339, July 2007.

[5] P. Royannez, H. Mair, F. Dahan, M. Wagner, M. Streeter, et al., "90 nm low leakage Soc design techniques for wireless applications," *Proc. IEEE ISSCC*, pp. 138–139, Feb. 2006.

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013

[6] K. Usami, N. Kawabe, and M. Koizumi, "Automated selective multi-threshold design for ultra-low standby applications," *Proc. IEEE ISLPED*, pp. 202–206, Aug. 2002.

1 Introduction

The sub-threshold leakage power is significantly reduced by power switch structure (hereafter called PSS) in the standby mode [1]. However, the power switch is no longer effective in sub-1V region because the high threshold voltage (Vth) of the power switch degrades the operation frequency rapidly at the low voltage [2]. In this letter, in order to extend the power switch to sub-1V supply-voltage region and to reduce leakage during the sleep mode, low-Vth footers connected in series are deployed. For the speed improvement of the series-connected footer structure, the drain node of each footer is used as virtual ground pin, where the upper virtual ground pin is connected to the logic circuits on the non-critical paths, and the lower virtual ground pin is connected to the logic circuits on the critical paths.

2 Power switch implementation

Figure 1 (a) shows our new PSS consisting of nine low-Vth NMOS devices. In spite of using low-Vth footers, the series-connected low-Vth footer scheme can reduce leakage power by the stack effect and smaller footer size. However, it suffers from the reduced performance, increased ground bound, increased wake-up time, and increased wake fluctuation due to increased resistance. In order to compensate for the reduced performance, the proposed scheme uses two virtual lines as shown in Fig. 1 (a) in which M1 and M2 are strong devices (main footers), and the other weak devices are deployed for gate-tunneling leakage (hereafter called gate leakage) reduction, wake-up time, and wake-up fluctuation reduction. The first virtual ground Vvss1 is connected to the gates on the non-critical paths because two serial footers (M1 and M2) reduce leakage current during sleep mode but increase gate delay during active mode. On the other hand, the second virtual ground Vvss2 is connected to the gates on the critical paths because one footer (M1) reduces gate delay during active mode and still can reduce certain amount of leakage current during sleep mode.

In order to further reduce the delay and ground bounce for the critical paths, M2 size should be greater than M1; the total size of the proposed power switch consisting of NMOS is smaller than one footer size of the conventional power switch because the reduced width of the footer can be compensated with the low-Vth and thin oxide thickness. The reason is that in active mode the footer operates in the linear region and the footer current is given by:

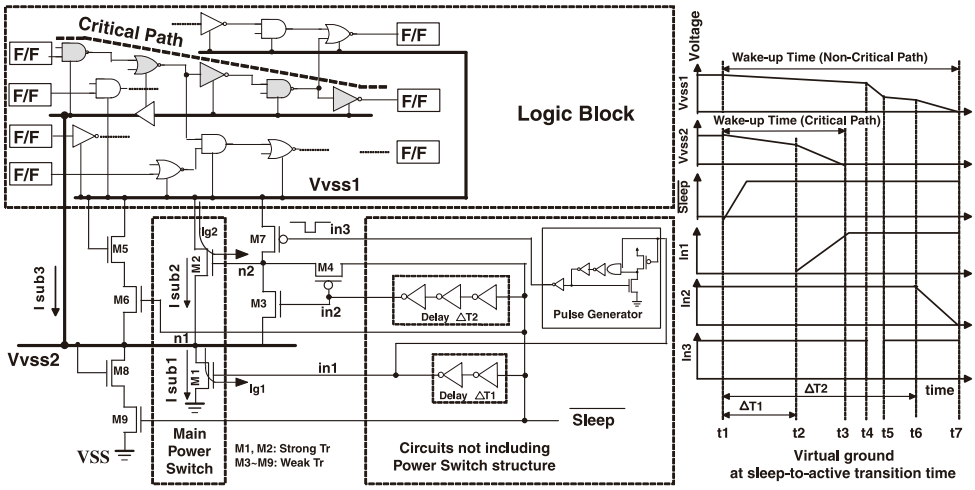
$$I_{footer} \approx \mu \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{th})V_{VSS} \quad (1)$$

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013

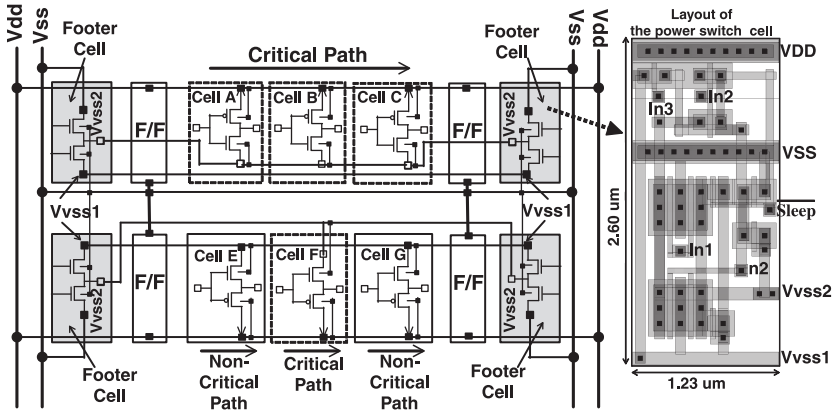
where ε_{ox} is the permittivity for SiO_2, t_{ox} is the oxide thickness, μ is the mobility, and V_{VSS} is the virtual ground voltage.

For the simple physical design of the new power switch, the new power switch cell can be placed in the same placement strategy as that of the conventional power switch except Vvss2: Vvss1 is connected to the local ground rail the same as the virtual ground of the conventional power switch, whereas Vvss2 is used as a pin to connect the ground pins of the modified logic cells on the critical paths. The lines between Vvss2 and logic cells on the critical paths are routed as inter-cell wires. Figure 1 (b) shows the conceptual power network for the new PSS.

The leakage current during sleep mode and the wake-up time depend on the potential of each virtual ground. Under the assumption that the logic circuit is a simple inverter and the footers are biased in the weak inversion region, the steady state of each virtual VSS can be obtained by matching the



(a)



(b)

Fig. 1. (a) Block diagram of the proposed PSS, (b) Conceptual power network for the new PSS

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013

leakage current the logic circuit with the leakage for the footers as follows:

$$Vvss1 = \frac{-Vth + 4\eta Vdd - S\log_{10}\left(\frac{W^2_{Footer(M1)}W_{Footer(M2)}}{W^3_{Circuit(Non-Critical)}W_{Circuit(Critical)}}\right)}{5\eta} \quad (2)$$

$$Vvss2 = \frac{-2Vth + 3\eta Vdd - S\log_{10}\left(\frac{W^2_{Footer(M2)}}{W_{Footer(M1)}W_{Circuit(Non-Critical)}W^2_{Circuit(Critical)}}\right)}{5\eta} \quad (3)$$

where η is the DIBL coefficient and S is the sub-threshold slope.

From Eqs. (2) and (3), Vvss2 can be changed depending on the footer size to reduce leakage current and wake-up time of the logic circuit on the critical paths. In order to reduce the dominant gate leakage (Ig2), M3 is deployed where the gate-to-source voltage of M2 is almost 0 V and M2 is turned off. The voltage difference between Vvss1 and the gate node of M2 is decreased from around Vdd to n2 voltage which makes Ig2 exponentially decrease according to gate leakage equation. During the short mode-transition time from sleep to active, the conventional power switch suffers from rush-thru current and large wake-up time [3]. In order to overcome this problem, it is suggested that the virtual ground voltage is gradually decreased using a new structure as shown in Fig. 1 (a). When M6 and M9 are turned on during short period of transition time, the two virtual grounds (Vvss1 and Vvss2) start to be discharged up to a small value. After $\Delta T1$ induced by a delay line, M1 is turned on, and Vvss2 is completely discharged to 0 V at t3 (wake-up time of the circuits on the critical paths), whereas Vvss1 is not fully discharged. From t4 to t5, Vvss1 goes down sharply through M7 where the input is a short negative pulse. After $\Delta T2$ induced by another delay line, M3 is turned off, and M4 is turned on. Finally, Vvss1 is completely discharged at t7 (wake-up time of the circuits on the non-critical paths). This gradual discharging approach considerably reduces the rush-current during mode-transition.

Figure 2 shows the delay dependence of the conventional power switch and the proposed power switch on power supply voltage for 20 inverter chains with 16 chains having 30 inverters and 4 chains having 40 inverters using 45 nm

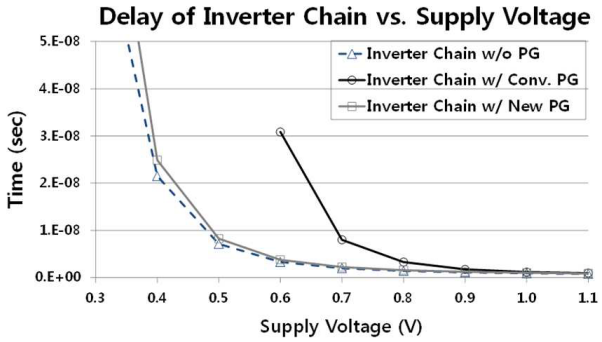


Fig. 2. Delay dependence on supply voltage of PSS

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013

Table I. Simulation results

(Inverter Chain) Simulation Conditions: low-Vth and high-vth are 0.165 V and 0.524 V for NMOS, (−0.165 V and −0.524 V for PMOS), t_{ox} of low-Vth and high-Vth MOS are 1.1 nm and 1.9 nm, and temperature is 25°C for sleep mode and 125°C for active mode						
PSS Scheme	Normalized by low-Vth Designed Logic Block			Normalized by Conventional PSS		
Vdd=1.1 V	Avg. Leakage Power	Delay (Longest)	Area	Avg. Wake-up Power	Wake-up Time	Wake-up Noise (Peak-to-Peak)
Low-Vth Inverter Chains without PSS)	1.000	1.000	1.000	N/A	N/A	N/A
High-Vth Inverter Chains without PSS)	0.002	6.993	1.000			
Dual-Vth Inverter Chains without PSS)	0.246	1.008	1.000			
Conventional PSS	0.024	1.197	1.100	1.000	1.000	1.000
Multi-mode PSS	0.015	1.195	1.103	1.219	1.083	1.070
Two-pass PSS	0.021	1.190	1.103	1.011	3.665	1.012
Zigzag PSS	0.171	8.342	1.150	0.577	0.818	0.919
Selective PSS	0.048	1.166	1.025	0.466	1.031	1.111
New PSS (vdd=1.1 V)	0.025	1.129	1.064	1.133	0.454	0.688
New PSS (vdd=0.6 V)	0.012	4.744	1.064	0.268	0.758	0.202

Note **: This simulation result shows the efficiency of the proposed power switch at 0.6 V supply voltage. For ultra-low voltage circuits such as below 0.6 V, previous high-Vth based PSS (Conventional PSS [1], Multi-mode PSS [4], Two-pass PSS [5], Zigzag PSS [2], and Selective PSS [6]) cannot be used due to the impractical delay increase and long wake-up time.

(ISCAS85 Circuits) Simulation Conditions: low-Vth and high-vth are 0.165 V and 0.524 V for NMOS, (−0.165 V and −0.524 V for PMOS), t_{ox} of low-Vth and high-Vth MOS are 1.1 nm and 1.9 nm, and temperature is 25°C for sleep mode and 125°C for active mode								
Circuit	# of Gates	Normalized by Low-Vth Designed Logic Block		Normalized by Conventional PSS				
		Avg. Leakage Power	Longest Path Delay	Avg. Leakage Power	Gate Leakage (Footer)	Longest Path Delay	Avg. Wake-up Power	Wake-up Time
C432	160	0.132	1.012	1.116	0.162	0.762	0.917	0.023
C880	383	0.168	1.081	1.151	0.397	0.346	0.912	0.021
C1355	546	0.127	1.018	0.884	0.395	0.627	1.003	0.025
C1908	880	0.096	1.034	0.865	0.097	0.655	0.991	0.017
C2670	1193	0.123	1.077	1.403	0.559	0.428	0.932	0.017
C5315	2307	0.021	1.027	0.990	0.326	0.858	0.949	0.015
C6288	2406	0.103	1.022	1.363	0.129	0.478	0.928	0.012
C7552	3512	0.200	0.992	1.156	0.399	0.919	0.361	0.016
Avg. Reduction Rate (%)		87.88	-3.29	-11.60	69.95	36.59	12.58	98.18

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013

CMOS technology. The area overhead of the each power switch is 10% of the total NMOS width in the inverter chain, the 16 chains having 30 inverters are connected to Vvss1, and the 4 chains having 40 inverters are connected to Vvss2. As the supply voltage decreases below 0.8 V in active mode, the inverter chain using the proposed power switch becomes more than twice faster than the circuit using the conventional power switch, and its delay decreases by 88.24% compared to the circuit using the conventional power switch at 0.6 V. Furthermore, the conventional power switch does not work correctly below 0.6 V.

3 Simulation results and evaluation

The proposed PSS using 45 nm predictive technology model has been implemented and evaluated using inverter chains which consist of 20 inverter chains with 16 chains having 30 inverters and 4 chains having 40 inverters. In order to show the good balance of the proposed methodology among wake-up time, delay, wake-up power, wake-up fluctuation and leakage power of the PSS, the inverter chains are simulated for 11 well-known schemes and compared among them as shown in Table I. In order to show the efficiency of the new power switch at 0.6 V supply voltage, the ISCAS85 benchmark circuits are simulated for low-Vth logic block, conventional power switch, and the proposed power switch at the same conditions as those of the inverter chains except that the total footer size of the proposed power switch is 5% of the total NMOS width. Table I also presents the simulation results for ISCAS85 circuits: the wake-up fluctuation items for the both structures are left out because it can be ignorable (less than 0.002 V), and the total leakage is a little increased by 11.60% on average under the influence of the sub-threshold leakage; but it is expected that the total leakage is reduced much more as the technology scales down and the gate tunneling leakage current increases.

4 Conclusion

This letter proposes a novel PSS using a single low threshold voltage in ultra-low voltage nanoscale CMOS circuits. In order for the PSS to be extended to sub-1V region, two serial footers with a single low-Vth are used. The simulated results show that the proposed PSS is a practicable solution for high performance circuits in ultra-low voltage nanoscale CMOS in terms of leakage power, operational circuit speed, wake-up time, and ground bounce.

Acknowledgments

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2011-0014255).

DOI: 10.1587/elex.10.20120757
Received October 04, 2012
Accepted November 08, 2012
Published January 21, 2013