IEICE Electronics Express, Vol.7, No.13, 931–935

A spread-spectrum clock generator for 6-Gbps Serial ATA transceiver

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Abstract: A transmitter-side spread-spectrum clock generator (TX-SSCG) with a second-order $\Delta\Sigma$ modulator is proposed for a 6-Gbps Serial ATA. Mixed-mode simulations show that a second-order $\Delta\Sigma$ modulator in TX-SSCG reduces the random jitter component of the receiver-side tracking skew through quantization noise shaping. Deterministic jitter is reduced with the loop bandwidth of RXPLL. A 0.13-μm CMOS prototype chip shows that the transceiver operates at 6 Gbps over an 8-m SATA cable in TX-SSCG on and off. With TX-SSCG on, the spectrum is down-spread with 11.7-dB peak reduction and 5000-ppm spread amount.

Keywords: spread-spectrum, $\Delta\Sigma$ modulator, jitter, Serial ATA, serial link

Classification: Integrated circuits

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DOI: 10.1587/elex.7.931
Received May 03, 2010
Accepted June 03, 2010
Published July 10, 2010

1 Introduction

Serial ATA (SATA) is a high-speed serial link replacement for the parallel ATA attachment of mass storage devices. The third generation SATA [1] is now being developed to provide large bandwidth up to 6 Gbps. The SATA structure connects the two devices with a SATA cable in a point-to-point fashion. Since EMI emission from the SATA cable is a major concern, SATA specification [1] defines various EMI reduction methods: TX rise/fall time control, spread-spectrum clocking (SSC), data scrambling, and so on. SSC reduces the peak EMI emission by spreading the carrier frequency. EMI reduction techniques using SSC have been studied and explored for 1.5-/3.0-Gbps SATA [3, 4]. However, it is more important to consider the time-domain impact of SSC on the receiver-side tracking skew since signal integrity, including jitter, is a critical concern in 6-Gbps SATA due to a reduced bit-time.

SSC techniques [4] for 3-Gbps SATA are adopted in this work. However, for 6-Gbps operation, jitter needs to be suppressed further. So, extensive simulations using a mixed-mode simulator are required to investigate the effects of SSC modulation frequency, the bandwidth of a receiver-side phase-locked loop (RXPLL), and the order of $\Delta\Sigma$ modulator on deterministic jitter (DJ), random jitter (RJ), and total jitter (TJ), respectively.

In this paper, we propose a spread-spectrum clock generator (SSCG) scheme for a 6-/3-/1.5-Gbps multi-rate application. The next section of this paper describes detailed circuit design and analysis. Section 3 gives the experimental results. Section 4 concludes and summarizes this paper.

2 Spread-Spectrum Clock Generator

Fig. 1 (a) shows the proposed transmitter-side SSCG (TX-SSCG). It consists of a transmitter PLL (TXPLL), 12-phase clock, and SSC Control. 12-phase

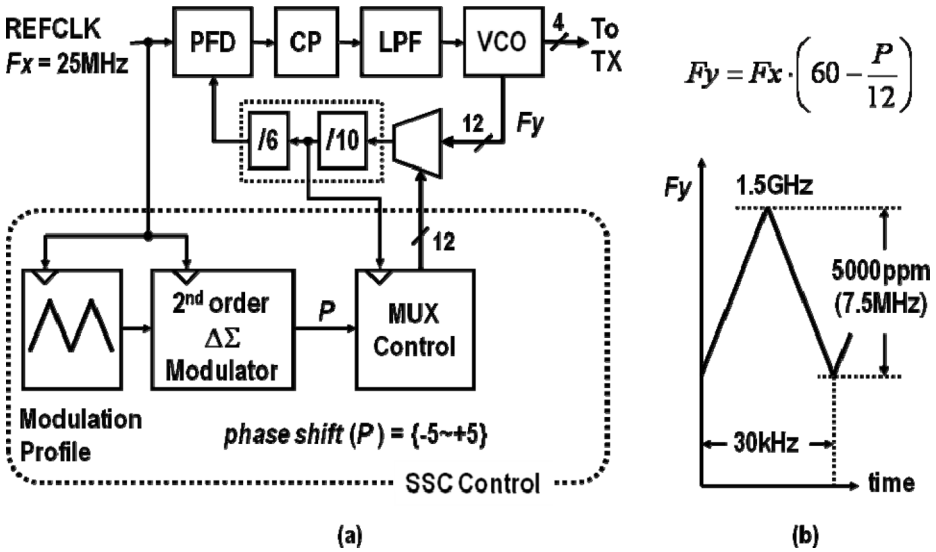

Fig. 1. TX-SSCG: (a) block diagram and (b) output frequency.

DOI: 10.1587/elex.7.931
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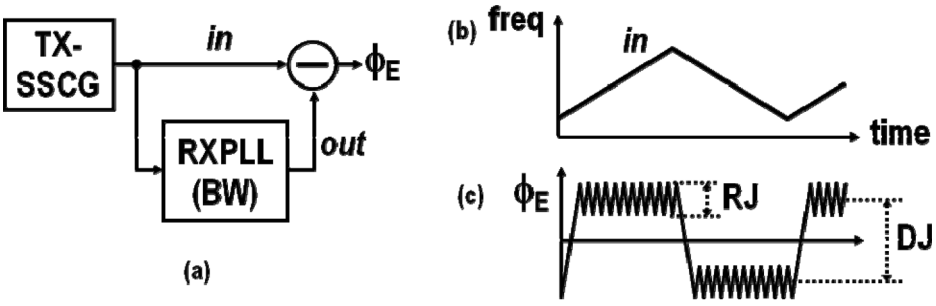
clocks operate at 1.5 GHz and four clocks of these clocks are selected as transmit clocks for a serializer in a transmitter. The modulation frequency is set to 30 kHz and the modulation amount is set to 5000 ppm. These are determined by a modulation profile. Based on the modulation profile, a $\Delta\Sigma$ modulator dynamically changes the phase shift amount (P), which has an integer value ranging from -5 to $+5$. MUX Control changes the clock phase by a minimum phase step equivalent to $T_{\mathrm{VCO}}/12$, rather than a full VCO period T_{VCO}. That is, using 12-phase clocks, the amount of phase jump in the feedback signal to the PFD can be only one-twelfth of a conventional multi-modulus frequency synthesizer, thereby generating significantly less jitter [2]. Since MUX Control operates at a six fold higher frequency (150 MHz) than the $\Delta\Sigma$ modulator (25 MHz), it can deal with any phase shift amount (P), which is updated by the $\Delta\Sigma$ modulator. For example, with $P = 5$, MUX Control changes the clock phase for five periods out of six consecutive 150-MHz clock periods. The output frequency is determined by the phase shift amount (P), as Eq. (1).

$$Fy = Fx \cdot \left(60 - \frac{P}{12}\right). \tag{1}$$

The divide ratio is $\left(60 - \frac{P}{12}\right)$. 12-phase clocks, MUX circuit, and SSC Control correspond to the fractional portion in the divide ratio while a divide-by-10 and a divide-by-6 circuits correspond to 60.

Fig. 2 (a) shows a mixed-mode simulation setup. This mixed-mode simulation reduces the simulation time compared to iterative methods by SPICE. In a PLL-based system like a SATA transceiver, a receiver PLL (RXPLL) has



SSC Mod. Freq.	30 kHz				100 kHz			
RXPLL (BW)	1.8 MHz		6.0 MHz		1.8 MHz		6.0 MHz	
ΔΣ Mod (Order)	1st	2nd	1st	2nd	1st	2nd	1st	2nd
TJ	88ps	60ps	32ps	24ps	175ps	165ps	36ps	32ps
DJ	40ps	40ps	4ps	4ps	130ps	130ps	10ps	10ps
RJ	48ps	20ps	28ps	20ps	45ps	35ps	26ps	22ps

(d)

Fig. 2. Simulation of receiver tracking skew: (a) mixed-mode simulation setup, (b) RXPLL input frequency (c) tracking skew components (RJ and DJ), and (d) simulation results.

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a limited loop bandwidth. As the input clock being modulated by TX-SSCG in Fig 2 (a), RXPLL cannot instantaneously update the output clock. The result is a slight difference between the periods of the RXPLL input clock and its output clock. As the frequency of the input SSC clock is modulated, the accumulation of the period difference can result in a significant amount of phase error between the RXPLL input clock and the output clock [5]. This phase error (ϕ_E) is defined as the PLL tracking skew. This tracking skew will decrease the setup/hold margins at a receiver-side clock-and-data recovery (CDR) circuit.

As shown in Fig. 2 (c), the tracking skew in a receiver side consists of DJ and RJ components. The DJ component varies with the same frequency as a 30-/100-kHz modulation frequency. The DJ component is reduced with the bandwidth of RXPLL, as shown in Fig. 2 (d). SSC modulation profiles contain higher-order harmonic contents as well as that of the fundamental modulation frequency. The maximum change of the frequency occurs when the modulation changes the polarity of its slope at the min/max corners, as shown in Fig. 2 (b). RXPLL needs to have a sufficiently large loop bandwidth to accurately track the sudden change of the input frequency and all the essential modulation harmonics.

When a second-order $\Delta\Sigma$ modulator is used instead of a first-order $\Delta\Sigma$ modulator, the RJ component is reduced while the DJ component is unaffected, as shown in Fig. 2 (d). Compared to a first-order $\Delta\Sigma$ modulator, a second-order $\Delta\Sigma$ modulator shapes more quantization noise to a high frequency. Therefore, in a second-order $\Delta\Sigma$ modulator, the power spectral density (PSD) of the quantization noise is attenuated in low frequencies but the PSD in high frequencies is increased by 40 dB per decade. However, since a third-order TXPLL in TX-SSCG has a jitter-transfer function of 40 dB/dec decrease at high frequencies, the high-frequency quantization noise of the $\Delta\Sigma$ modulator is filtered out. When $\Delta\Sigma$ modulators with orders higher than two are used, the PLL needs extra poles in the loop filter and PLL stability is hard to maintain. So, higher-order $\Delta\Sigma$ modulators are not considered in this analysis. In short, simulation results show that the tracking skew in RX can be lowered with a second-order $\Delta\Sigma$ modulator and higher RXPLL bandwidth.

3 Experimental results

A prototype chip with the proposed TX-SSCG with a second-order $\Delta\Sigma$ modulator was designed in a 0.13-μm CMOS technology [6]. The power supply voltage is 1.2 V. System tests show that the transceiver operates at 6 Gbps over a SATA connector and an 8-m SATA cable with no error detected (BER$<10^{-14}$) in both cases of TX-SSCG, on and off.

Fig. 3 shows spectra of a 3-GHz clock pattern, i.e. 6-Gbps 1010 pattern. With TX-SSCG off, 6-Gbps TX output has 3-GHz single tone. With TX-SSCG on, the spectrum is down-spread with 11.7-dB peak reduction and 5000-ppm spread amount using a 30-kHz triangular modulation profile. For

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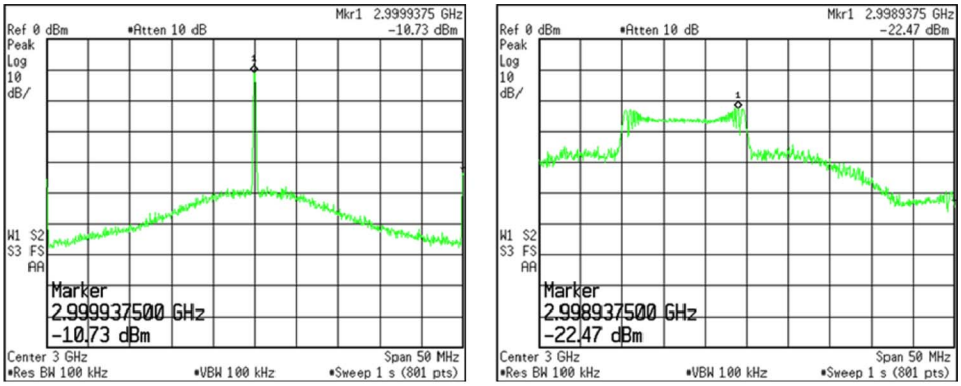

Fig. 3. Spectra of 3-GHz clock (1010) pattern in (a) SSC off and (b) SSC on.

this measurement, the resolution bandwidth of a spectrum analyzer is set to 100 kHz.

4 Conclusion

A transmitter-side spread-spectrum clock generator (TX-SSCG) reduces EMI emission from a SATA cable. However, the reduction of the receiver-side tracking skew also needs to be considered to increase receiver-side setup/hold margins for a 6-Gbps operation. Simulations using a mixed-mode simulator show that when a second-order $\Delta\Sigma$ modulator is used in TX-SSCG instead of a first-order $\Delta\Sigma$ modulator, more quantization noise is shifted to high frequency thereby resulting to low random jitter (RJ) due to the low-pass characteristic of TXPLL. Simulations also show that deterministic jitter (DJ) is reduced with the loop bandwidth of RXPLL since a high-bandwidth RXPLL accurately tracks the sudden change of the input frequency and all the essential modulation harmonics. System measurements show that the transceiver operates at 6 Gbps over a SATA connector and an 8-m SATA cable with no error detected (BER$<10^{-14}$) in both cases of TX-SSCG, on and off. With TX-SSCG on, the spectrum is down-spread with 11.7-dB peak reduction and 5000-ppm spread amount using a 30-kHz triangular modulation profile.

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