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# A 0.6 V passive mixer with high conversion gain in 65 nm CMOS process

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**Abstract:** A passive mixer with a complementary gm stage and a low voltage IF trans-impedance amplifier, which can operate under low voltage conditions, is proposed in this letter. With at most two transistors stacked between vdd and gnd, the proposed mixer can be realized in regular CMOS processes without reducing the threshold voltage of transistors. A high conversion gain is obtained thanks to the high utilization efficiency of the RF current generated by the trans-conductance (gm) stage. A prototype of the proposed mixer structure which works in the frequency band from 1 GHz to 2 GHz is designed and fabricated in SMIC 65 nm CMOS process. Measurement results indicate that, the prototype achieves a conversion of 22 dB and a noise figure of 15 dB. The power consumption is 1.2 mW under the supply voltage of 0.6 V.

**Keywords:** RF, mixer, conversion gain, low voltage

**Classification:** Integrated circuits

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## 1 Introduction

For the application of portable wireless consumer electronics, low power consumption is especially crucial to prolong the lasting time of the battery powered devices. Current reusing techniques which share the static current of several current-hungry modules, reduce the total power dissipation dramatically [1, 2]. However, the inter-module crosstalk cannot be completely avoided in the current reusing structures. Besides the current-optimizing approaches, another intuitive idea to cut down the total power consumption is reducing the supply voltage. Designing circuits under a supply voltage as low as 0.6 V has a great prospect for the possibility to be powered by one single solar-cell. But the 0.6 V inter-space between vdd and gnd can only accommodates two transistors working in saturated region. Some approaches use native transistors and bulk-injection technique [4, 5] to ease the voltage headroom problem, but they often face issues such as the leaking current and the increase of fabrication cost. In this letter, a low voltage passive mixer structure is proposed, which is designed with normal $V_{TH}$ transistors and is free from the problems mentioned above. By designing a complementary gm stage and a low voltage IF trans-impedance amplifier (TIA), the mixer can work properly under the 0.6 V supply voltage.

## 2 Proposed low voltage mixer designs

Fig. 1 shows the circuit schematic of the proposed low voltage passive mixer, which is composed of the gm stage, the double balanced switching pair and the trans-impedance stage. Complementary structure is adopted in the gm stage to improve the effective trans-conductance. Limited by the low supply voltage, the traditional self-biasing structure is replaced by a low voltage common-mode feed-

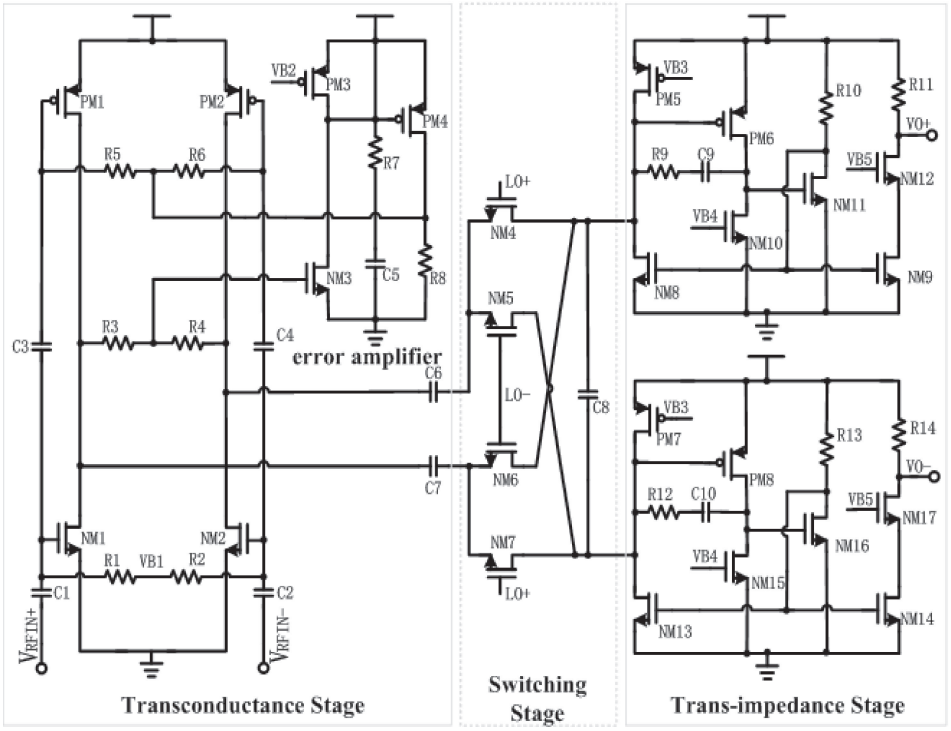


**Fig. 1.** Circuit schematic of the proposed mixer


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back circuit. The error amplifier in the feedback loop is built by a two-stage single-ended common-source amplifier which set the dc voltage at the output node of the gm stage equal to the quiescent $V_{GS}$ of NM3. NM3 is biased in sub-threshold region as to set the common-mode voltage near half of the supply voltage, keeping both the NMOS and PMOS gm transistors working in the saturated region.

The outputs of the gm stage are connected to a double balanced switching pair which operates the frequency conversion. Driven by LO signals, the switching transistors turns on and off alternately to perform the current steering. The LO signal is AC-coupled to the switching pair. By setting a proper dc bias voltage, the LO voltage applied to the gate of the on-state switching transistors can be higher than the supply voltage, ensuring a relatively low on-resistance under the insufficient supply voltage of 0.6 V.

In the proposed mixer, the low voltage TIA is used to create low input impedance and turns the down-converted current into output IF voltage. The TIA is a negative feedback structure which turns the input current into the VGS variations of NM8. The current of NM9 is mirrored from NM8, copying the IF current and converts it into output voltage on the load resistors R11/R14. The feedback loop in the TIA is constituted by cascading three common-source amplifiers end to end. For the ease of stability optimization, the value of R10 is minimized to limit the loop gain. There are at most two transistors stacked between vdd and gnd, which makes it suitable for the 0.6 V supply voltage.

In a passive mixer, transistors in the switching pair work in the triode region when the switch is on. The transistors can thus be regarded as a small resistor seen from both sides. With the LO signal commutating the polarity of the current which flows through the switching pair, the RF impedance at the output of the gm stage is pulled down by the small input IF impedance of the TIA due to the frequency-transformation effect. Capacitor C8 is connected between the input terminals of the TIAs, filtering out the up-conversion outcomes. The small RF impedance seen into the switching pair ensures most of the RF current generated by the gm stage are injected into the switching pair. The high utilization efficiency of the RF current guarantees a high conversion gain, with a relatively low bias current consumed in the gm stage.

The parameters of the used transistors, the capacitors and the resistors are listed in Table I.

**Table I.** Parameters of all the devices in the proposed mixer

| device | parameter | device | parameter | device | parameter |
|---|---|---|---|---|---|
| NM1,2 | 24 µm/0.13 µm | NM3 | 24 µm/1 µm | PM6,8 | 36 µm/2 µm |
| C1,2 | 2 pf | C5 | 6 pf | NM10,15 | 8 µm/2 µm |
| R1,2 | 52 kΩ | R7 | 11 kΩ | NM11,16 | 6 µm/1 µm |
| R3,4 | 20 kΩ | NM4-7 | 32 µm/0.13 µm | NM9,14 | 32 µm/2 µm |
| R5,6 | 20 kΩ | C6,7,9,10 | 2 pf | NM12,17 | 120 µm/0.13 µm |
| PM1,2 | 144 µm/0.13 µm | C8 | 4 pf | R10,13 | 5 kΩ |
| PM3 | 40 µm/2 µm | PM5,7 | 120 µm/2 µm | R11,14 | 2 kΩ |
| PM4 | 40 µm/2 µm | NM8,13 | 32 µm/2 µm | R9,R12 | 21 kΩ |


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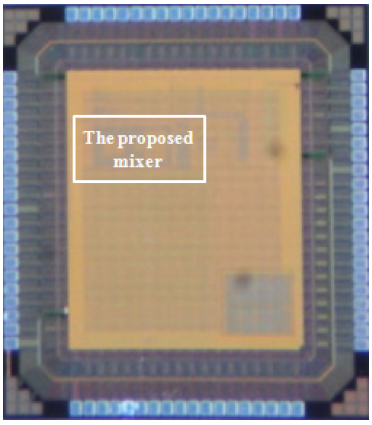


**Fig. 2.** Chip microphotograph of the proposed mixer

## 3 Measurement results

The proposed mixer is designed and fabricated in SMIC 65 nm CMOS process under the 0.6 V supply voltage. Fig. 2 shows the die photograph of the prototype. The active area of the proposed mixer is 220 μm × 130 μm. The total dc current of the mixer is 2 mA, among which is 1.5 mA consumed by the gm stage.

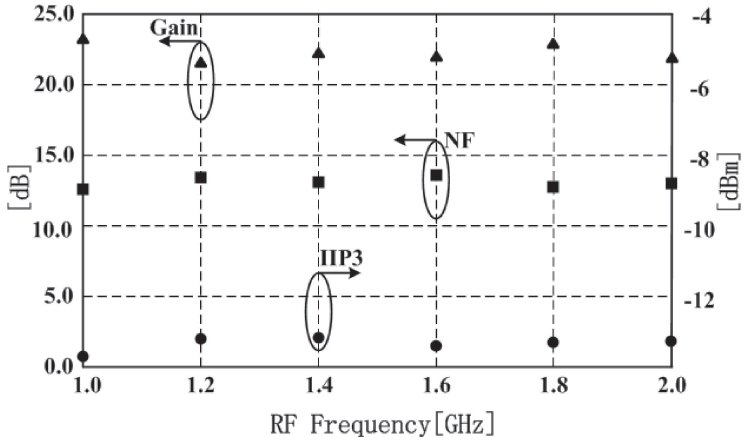


**Fig. 3.** Measured conversion gain, NF and IIP3 versus RF frequency at fixed 2 MHz IF frequency.

Fig. 3 shows the measured results of the proposed low voltage mixer. The mixer works in the frequency band from 1 GHz to 2 GHz with a fixed output IF frequency of 2 MHz. To test the conversion gain of the proposed mixer at different frequencies, the input RF signal is applied with the power of −50 dBm. The unified power of the down-converted output signal is measured at the output node to obtain the conversion gain. The maximum and minimum conversion gains are 24 dB and 22 dB respectively. The measured minimum IIP3 is −14 dBm and the NF is about 14 dB. The performance of the proposed mixer is compared with other previous works in Table II, which indicates that the mixer has an evident superiority in conversion gain, and FoM. For the proposed mixer, the relatively large bias current in the gm stage and the high linearity characteristic of the TIA helps to achieve a better OIP3 compared with the listed previous works.


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**Table II.** Performance comparison with other works

| | [4] | [5] | [6] | [7]* | This work |
|---|---|---|---|---|---|
| Frequency (GHz) | 0.5–7.5 | 0.2–13 | 2.1–3 | 0.48–0.86 | 1–2 |
| Supply voltage (V) | 0.77 | 0.88 | 0.6 | 1.2 | 0.6 |
| Conversion Gain (dB) | 5.7 | 9.9 | 5.4 | 21 | 22 |
| IIP3 (dBm) | −5.7 | −10 | −2.8 | 9 | −14 |
| OIP3 (dBm) | 0 | 0 | 2.6 | 30 | 8 |
| NF (dB) | 15 | 11.7 | 14.8 | 12.4 | 14 |
| Power (mW) | 0.48 | 0.88 | 1.6 | 5.4 | 1.2 |
| **FoM | 13.2 | 13.8 | 9.5 | 20.4 | 14.2 |

* is a regular passive mixer with normal supply voltage of 1.2 V
**The FoM is defined as what is shown in the reference [3].

## 4 Conclusions

This letter proposes a low voltage, high conversion gain passive mixer which is designed in SMIC 65 nm CMOS process. The mixer is based on the passive mixer structure with a complementary gm stage and low voltage TIAs. The proposed mixer can be realized in regular CMOS processes without reducing the threshold voltage of the transistors. A high conversion gain is obtained thanks to the high utilization efficiency of the RF current generated by the gm stage. Measurement results indicate that, the prototype achieved a conversion of 22 dB, the IIP3 of −14 dBm and the noise figure of 15 dB at the frequency band from 1 GHz to 2 GHz.

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