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A low-jitter pulsewidth control loop with high supply noise rejection

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Abstract: A low-jitter pulsewidth control loop (PWCL) with high supply noise rejection for high-speed pipelined ADC is presented in this letter. Based on the edge triggered PWCL, An improved charge pump, a novel control stage (CS) and delay compensation circuits (DCC) was utilized to decrease the supply-induced jitter. The experimental results demonstrate that within 180 ns the PWCL can lock the clock duty cycles for the accuracy of 50 ± 1% with 10%∼90% input duty cycle from 50 MHz to 500 MHz. The p-p jitter is 10.1 ps at 500 MHz, and the variation of duty cycle is less than 0.05% within ± 10% supply noise.

Keywords: PWCL, low-jitter, noise rejection, voltage substractor, DCC

Classification: Integrated circuits

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1 Introduction

To meet the high speed applications, the system clock with a duty cycle of 50% plays an important role in CMOS VLSI circuit. However, the duty cycle of clock is difficult to fix at 50% due to nonideal factors. Thus, the PWCL mechanism is developed to solve this problem.

Conventional PWCL designs can be divided into two categories, edge triggered PWCL [1] and voltage feedback PWCL [2, 3]. However, in [1, 2, 3], the time varying supply noise have not been investigated which can

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worsen the timing margin of critical paths by modulating period jitter. In this letter, an improved charge pump, a novel control stage (CS) and delay time compensation circuits are introduced to restrain the supply noise.

2 Topology of the proposed PWCL

For many applications, switching activity in large digital systems introduces power noise, which perturbs the more sensitive blocks in clock paths. Time varying supply noise, in particular, is the most disconcerting type of jitter for synchronous design styles. For a K stage clock distribution, the nth leading clock edge arrives at the first clock driver at time $t_{n,1}$. The arrival time of Kth stage is

$$t_{n,K}^{(r)} = t_{pLH}(v_{noise}(t_n, K-1)) + \cdots + t_{pHL}\big(v_{noise}\big(t_{n,1}\big)\big) + t_{n,1} \tag{1}$$

The recursive period jitter equation is formulated as

$$PJ_{n,K}^{(r)}\big(t_{n,1}, t_{n+1,1}\big) = t_{n+1,K}^{(r)}\big(t_{n+1,1}\big) - t_{n,K}^{(r)}\big(t_{n,1}\big) \tag{2}$$

Where t_{pLH} and t_{pHL} are propagation delays for high-to-low and low-to-high transitions with time varying supply noise and a, b, c, d the delay coefficients [4].

The proposed PWCL architecture is shown in Fig. 1 (a). The edge triggered PWCL [1] was adopted to acquire a high accuracy clock signal. It consists of the control stage (CS), charge pump loop (CPL), rising edge generator (RG), inverter delay time compensation circuit (DCC) and falling edge differentiator (FD). The FD generates a pulse at every rising edge of the input signal and the pulse width equals to the transmission delay of inverters. The pulse triggers the control stage to generate the falling edge of output clock. With a fixed-delay falling edge, the PWCL adjusts the duty cycle by controlling the delay of a low-level pulse (*up*) which triggers the control stage to generate the rising edge, and controlled by the voltage V_C generated from charge pump loop. DCC compensates the delay variation of inverters. The timing diagram is show in Fig. 1 (b).

3 Key circuits implementation and analysis

The structure of charge pump loop is shown in Fig. 1 (e), which mainly consists of an improved charge pump, low-pass filter, a supply noise canceling circuit and Wilson current mirror. The proposed charge pump adopts combined charge pump and self-biasing technique to guarantee the sourcing/sinking current matching. The combined charge pump structure uses the complementary signals *up* and *dn* (generated by *Clkout+* and *Clkout−*) as inputs, simultaneously, transmission gate switches are employed to reduce the effect of charge injection.

In addition, the proposed circuits introduce a Wilson current mirror (WCM) for further supply rejection, consisting of *M20* and *M22*. Moreover, an auxiliary
supply noise canceling circuit (*NCC*) (*M23, M24, M25, M26*) is added to compensate the residual variation of the output current I_{CP_up} and I_{CP_dn} due to supply noise. This circuit generates two compensator currents I_{cancel_up} and I_{cancel_dn} by mirroring a fraction of I_{OP}, then, I_{cancel_up} and

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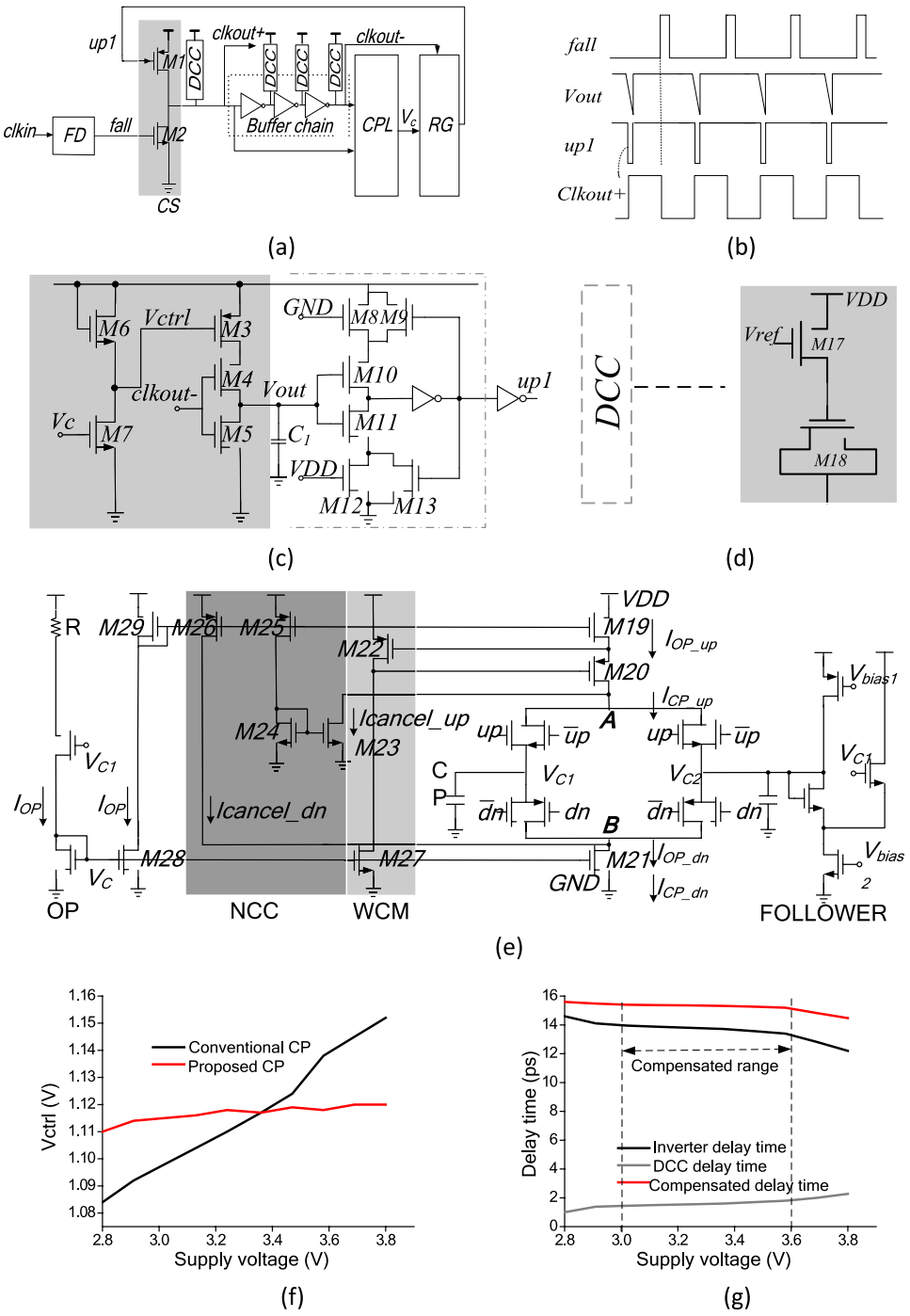

Fig. 1. (a) Proposed PWCL architecture, (b) The timing diagram of the overall PWCL, (c) RG, (d) DCC, (e) Improved charge pump loop, (f) Improved supply rejection of Vctrl, (g) Delay time compensation with DCC.

I_{cancel_dn} are subtracted from I_{OP_up} and I_{OP_dn}, respectively. Thus, the sourcing and sinking current are I_{CP_up}=I_{OP_up}−I_{cancel_up} and I_{CP_dn}=I_{OP_dn}−I_{cancel_dn}. If ΔI_{OP_up}=ΔI_{cancel_up} and ΔI_{OP_dn}=ΔI_{cancel_dn}, I_{CP_up} and I_{CP_dn} will be insensitive to supply noise. Where ΔI_{OP_up}, ΔI_{cancel_up}, ΔI_{OP_dn}, and ΔI_{cancel_dn} are the current variations due to supply noise, respectively. In this work,

$$\left(\partial I_{OP\_up}/\partial VDD\right)/\left(\partial I_{cancel\_up}/\partial VDD\right) = 8 \tag{3}$$

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$$(\partial I_{OP\_dn}/\partial VDD)/(\partial I_{cancel\_dn}/\partial VDD) = 2 \tag{4}$$

By setting the ratio of the mirroring R_{29}=R_{19}=$2R_{26}$=$8R_{25}$, and R_{28}=R_{27}=$8/11R_{21}$, where R is the transistor dimensions, the sourcing and sinking current will be equal, and variations of I_{CP_up} and I_{CP_dn} due to supply fluctuation is cancelled. Equation (5) shows the improved PSR (power supply rejection)

$$\begin{aligned} PSR_{CP} &= \left(\partial I_{CP\_up}/\partial VDD\right)\Delta T \\ &= (r_{ds19}g_{m22}r_{ds22}g_{m20}r_{ds20} - \beta r_{ds25} \| 1/g_{m24})\Delta T \end{aligned} \tag{5}$$

Where β is the ratio of I_{CP_up} and I_{cancel_up} and ΔT the charge time. The voltage sensitivities of V_{ctrl} in the proposed and conventional circuits are 0.005V-V_{ctrl}/1V-VDD and 0.07V-V_{ctrl}/1V-VDD, as shown in Fig. 1 (f).

The delay stage consists of voltage-subtractor, the delay inverter with V_{ctrl} as control voltage, and the capacitor C_1. By controlling the discharging speed of C_1 in delay stage, the PWCL can adjust the duty cycle of output clock to a precise 50% duty cycle. Fig. 1 (c) depicts the topology of the delay stage. The voltage-subtractor, consisting of M_6 and M_7, feed the supply noise directly into the feedback loop and modulate the gate with respect to the source terminals of PMOS transistor (M_3). Considering that transistors M_6 and M_7 carry equal currents I, the square law model is derived as follows

$$I = K_7/2(V_{GS7} - V_{THN})^2 = \mu_n C_{ox}(W/L)_7/2(V_C - V_{THN})^2 \tag{6}$$

$$\begin{aligned} I &= K_6/2(V_{GS6} - V_{THN})^2 \\ &= \mu_n C_{ox}(W/L)_6/2(VDD - V_{ctrl} - V_{THN})^2 \end{aligned} \tag{7}$$

Combining (6) and (7) now yields

$$V_{ctrl} = VDD - V_C \tag{8}$$

The improved PSR is as follow

$$PSR_{DS} = g_{m3}r_{o5}(1 - g_{m6}r_{o7}/1 + (g_{m6} + g_{mb6})r_{o7}) \tag{9}$$

The variation of delay time due to supply noise is suppressed, as $g_{m6}r_{o7}$>>1.

In Fig. 1 (a), the buffer chain consists of three stages, CMOS inverters have poor supply-induced delay sensitivity of approximately 1%-delay/1%-VDD, through a long buffer chain, poor supply noise rejection of the inverter will generate significant jitter. To compensate the variation due to supply fluctuation, *DCC* are introduced [5]. The *DCC* incorporates a variable MOS resistor (*M17*) and a MOS capacitor (*M18*) interpolated at the output of each inverter, as shown in Fig. 1 (d). The gate of *M17* is set to a constant voltage. With VDD increasing, the delay time of inverter reduces, while the source-gate voltage of the MOS resistor increases, resulting in the decreasing of resistance of MOS resistor. Thus, the time constant of *DCC* is boosted, which compensates for the reduction in the inverter's delay time. Fig. 1 (g) illustrates that the conventional inverters' delay time varies with supply voltage as a proportion of 0.5%-delay/1%-VDD, while the overall delay sensitivity of the compensated inverter with DCC is approximately 0.03%-delay/1%-VDD for VDD variation within

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±10% (The supply noise does not exceed ±10% normally).

4 Experimental results

The proposed circuit has been fabricated in SMIC 0.18 μm CMOS technology. A microphotograph of the proposed circuit is shown in Fig. 2 (d).

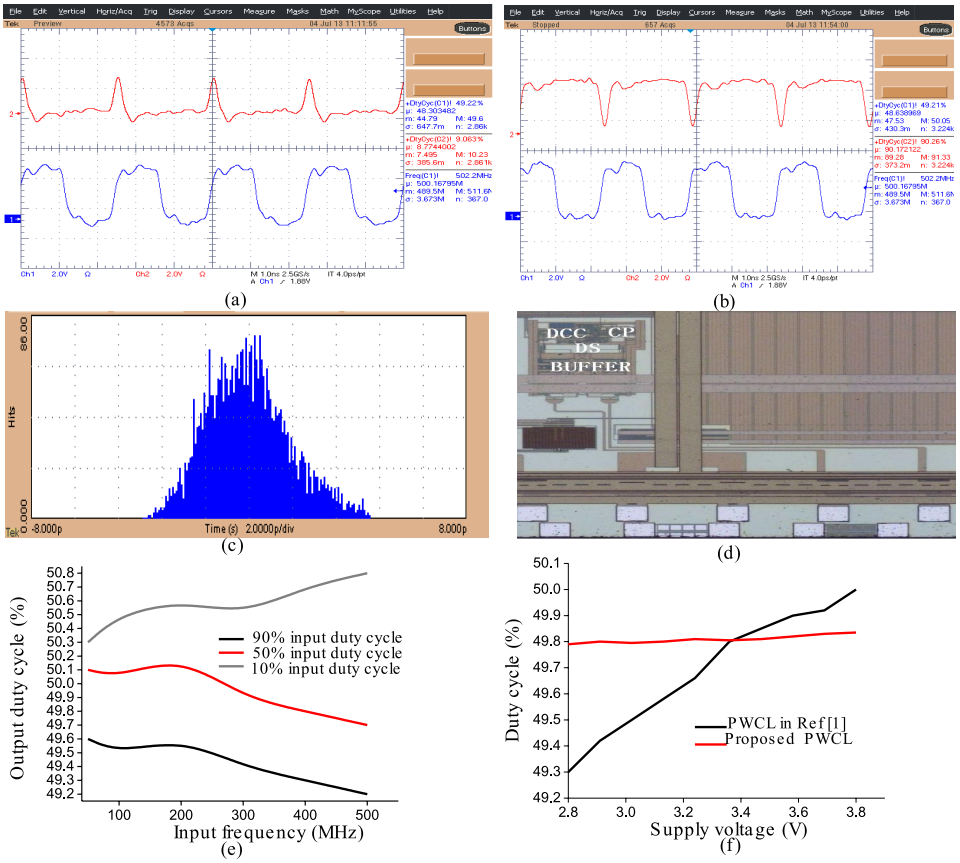

Fig. 2. (a) (b) Output duty cycle with 10% and 90% input duty-cycle (c) p-p Jitter with input 500 MHz frequency (d) microphotograph of the proposed circuit (e) pulsewidth control range (f) duty cycle versus supply voltage.

Table I. Performance comparisons of PWCLs.

	This work	[1]	[2]	[3]
Process	0.18μm	0.18μm	0.18μm	0.18μm
Input Duty	10~90 (%)	10~90 (%)	30~70 (%)	30~70 (%)
Output Duty	50±1 (%)	50±1 (%)	N/A	50±1.6 (%)
Clock Jitter	p-p jitter 10.1ps @ 500MHz	rms jitter 73fs@ 250MHz	p-p jitter 13.2ps@ 1GHz	p-p jitter 28.9ps@ 250MHz
Dynamic sensitivity (PSR)	0.05%-duty cycle/±10% supply	0.75%-duty cycle/±10% supply	1%-duty cycle/±10% supply	N/A
Active Area	0.027mm^2	0.023 mm^2	0.057mm^2	0.09mm^2

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The measured results demonstrate that the proposed PWCL can modulate the input clock with 10%∼90% input duty cycle from 50 MHz to 500 MHz as shown in Fig. 2 (a) and Fig. 2 (b). The pulsewidth adjustment results of the proposed PWCL are summarized in Fig. 2 (e). Fig. 2 (c) shows the peak-to-peak jitter for the 500 MHz output clock at 10.1 ps. Fig. 2 (f) depicts the duty cycle of the proposed PWCL versus VDD, and the variation of duty cycle is less than 0.05% within ±10% supply noise.

Table I summarizes the characteristics of our circuit in comparison with its counterparts reported in [1, 2, 3].

5 Conclusions

A high power supply rejection PWCL with improved charge pump, delay time compensation circuit, and a novel delay stage was presented in this letter. The inverter chain achieved a virtually constant delay time by utilizing DCC. The supply noise canceling circuits and voltage subtractor circuits are introduced to charge pump and delay stage, respectively, for a high supply noise rejection.

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