

A low jitter phase-locked loop based on self-biased techniques

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Abstract: A low jitter phase-locked loop (PLL) based on self-biased techniques was designed. The PLL achieves process independent and low input tracking jitter. A novel cascode charge pump (CP) is realized to improve the current matching so as to reduce the jitter of the system. A capacitor is employed in the second CP to make third order PLL. The PLL is fabricated in SMIC 0.13 μm CMOS process, which achieves a very wide tuning range from 625 MHz to 1.5 GHz. And the phase noise of the VCO at 1 MHz offset from the 1.25 GHz only has -94.66 dBc/Hz. The measured RMS jitter and peak-to-peak jitter at 1.25 GHz only have 3.53 ps and 21.19 ps.

Keywords: self-biased PLL, low jitter, VCO, cascode charge pump

Classification: Integrated circuits

References

- [1] J. G. Maneatis: IEEE J. Solid-State Circuits **31** (1996) 1723. DOI:10.1109/JSSC.1996.542317
- [2] J. G. Maneatis, J. Kim, I. McClatchie, J. Maxey and M. Shankaradas: IEEE J. Solid-State Circuits **38** (2003) 1795. DOI:10.1109/JSSC.2003.818298
- [3] B. Yuan and H. Liu: IEEE MMWCST (2013) 471. DOI:10.1109/MMWCST.2013.6814554
- [4] R. C. Chang and L. C. Kuo: IEEE ISCAS (2000) V-701. DOI:10.1109/ISCAS.2000.857586
- [5] F. M. Gardner: *Phaselock Technique* (Wiley, New York, 2005) 3rd ed. 10.
- [6] C.-C. Hung and S.-I. Liu: IEEE Int. Solid-State Circuits Conf. (2009) 400. DOI:10.1109/ISSCC.2009.4977477
- [7] C.-C. Hung and S.-I. Liu: IEEE Trans. Circuits Syst. II, Exp. Briefs **56** (2009) 525. DOI:10.1109/TCSII.2009.2020948
- [8] I.-T. Lee, Y.-T. Tsai and S.-I. Liu: IEEE J. Solid-State Circuits **47** (2012) 2693. DOI:10.1109/JSSC.2012.2209810
- [9] C.-Y. Li, C.-L. Lee, M.-H. Hu and H.-P. Chou: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **22** (2014) 2216. DOI:10.1109/TVLSI.2013.2285977
- [10] Z.-f. Hu, M.-d. Huang and L. Zhang: J. Chongqing Univ. Eng. Ed. **12** (2013) 97. DOI:10.11835/j.issn.1671-8224.2013.02.008

1 Introduction

PLL is a very important mixed-signal circuit widely used for frequency synthesis, clock generators, and clock data recovery circuits. The trend toward the high performance PLL is high speed, low power and low jitter, and with the nanoscale CMOS process, the design of the high performance PLLs is possible.

John. G. Maneatis proposed a PLL which is based on self-biased techniques in [1]. Both the damping factor and the loop bandwidth to operating frequency ratio are decided by the ratio of two capacitors, which is less affected by process offset. The self-biased techniques were both used in [2, 3]. But all mentioned above are second order PLL which are using first order low-pass filter (LPF). To design low jitter PLL, we also need to think about the current matching of CP. [4] proposed a cascode CP consisted of a wide-swing current mirror and a symmetric CP pair which is composed of pump-up and pump-down circuits. In the design, it uses two NMOS coupled pairs to control the switches go on or off, however, it adds the each branch mismatching.

This paper designs a low jitter PLL based on self-biased techniques and achieves super performance that goes by good circuit and layout design. In this design, it is using two capacitors, so that it can filter the voltage ripple of voltage controlled oscillator (VCO) effectively. And it applies a novel cascode CP which can reduce the current mismatching.

2 The theory of self-biased PLL

PLL is an automatic phase synchronous system. The charge pump PLL which has a second order closed response consists of phase frequency detector (PFD), CP, LPF, VCO, and divider [1].

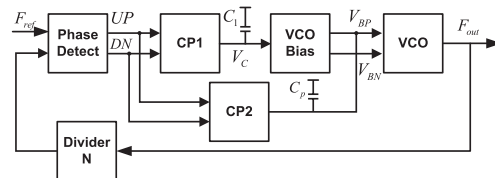


Fig. 1. The proposed PLL circuits

The proposed PLL adds the filter capacitor C_p in the second CP compared with [1] as shown in Fig. 1. We can analyze from Fig. 1 and Fig. 4 that the order of this PLL is three (type 2 in [5]) because it applies a second order LPF. And the analysis of open-loop transfer function is as follows.

The open-loop transfer function is given by Eq. (1).

$$G(s) = I_{CH} \frac{1 + \tau_2 s}{s(C_1 + C_p)(1 + \tau_1 s)} \frac{K_{VCO}}{s} \frac{1}{N}. \quad (1)$$

Where I_{CH} is the CP current, K_{VCO} is the VCO gain, $\frac{1 + \tau_2 s}{s(C_1 + C_p)(1 + \tau_1 s)}$ is the transfer function of LPF, $\tau_1 = \frac{RC_1 C_p}{C_1 + C_p}$, $\tau_2 = RC_1$, and R is the LPF resistor [Fig. 4]. Since $G(s)$ decreases to 1, we can get the open-loop bandwidth as Eq. (2).

$$|G(s)| = \left| \frac{I_{CH}K_{VCO}}{N \cdot j\omega_c} \frac{1 + \tau_2 j\omega_c}{j\omega_c(C_1 + C_p)(1 + \tau_1 j\omega_c)} \right| = 1. \quad (2)$$

$$\omega_c \approx \frac{I_{CH}K_{VCO}R}{N} \frac{C_1}{C_1 + C_p} \approx \frac{I_{CH}K_{VCO}R}{N}. \quad (3)$$

As the parameter given in [1], we can get $\frac{\omega_c}{\omega_{REF}} = \frac{x \cdot (2 \cdot I_D) \cdot k}{2\pi f_{REF} C_B} \cdot \frac{y}{\sqrt{8 \cdot k \cdot I_D}} = \frac{x \cdot y \cdot N}{2\pi}$.

Where x is the ratio of the CP current to VCO buffer bias current and y is the ratio of the LPF resistor to the symmetric load in the VCO buffer. So if N is a constant, we can get that open-loop bandwidth will track the operating frequency. Thus we can get the minimize jitter by setting open-loop bandwidth, the PLL also can operate at the same frequency of VCO. This PLL, taking advantages of third order PLL, not only increases the circuit ability to filter the ripple of control voltage but also need not to recalculate system parameter caused by adding the C_p .

3 The novel cascode charge pump

The proposed novel cascode CP in Fig. 2 applies the cascode structure to obtain a wide-swing current mirror. And pump-up and pump-down parts also use of cascode structure to improve the current matching. This structure decreases the open time of the switch, increases the speed and restrains the charge share effect and clock feedback effect.

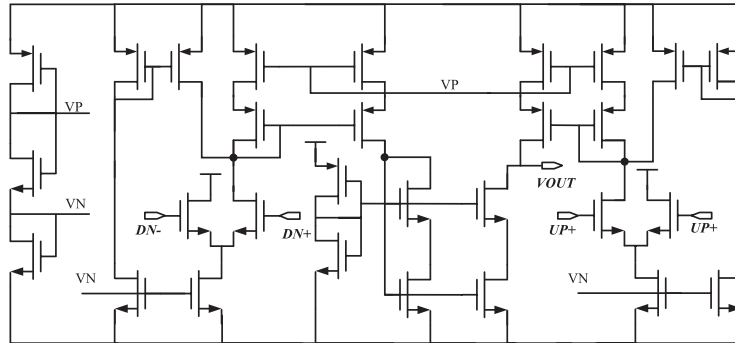


Fig. 2. The novel cascode charge pump circuit

Fig. 3 shows the simulation results of the CP. We can see that the charging and discharging current are matching well. When the output voltage range is from 0.3 V to 0.7 V, the mismatching current is less than 200 nA. It almost reaches the ideal matching degree.

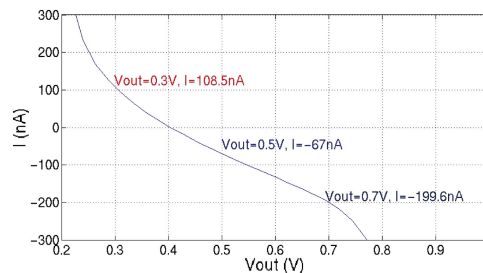


Fig. 3. The simulation results of CP

4 The self-biased PLL circuits design

To complete the self-biased PLL, some loop components are required as follows.

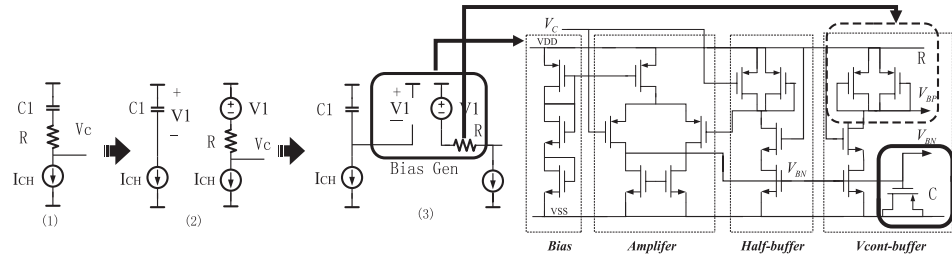


Fig. 4. Bias generator part

The biased condition depends on the circuit operating bias levels. So the critical theory of the self-biased PLL is the bias generator part as shown in Fig. 4. We can see that the controlled voltage of VCO is sum of the voltage drops across the capacitor and the resistor which consisted of LPF in series types. However, the voltage drops across the capacitor and resistor can be generated separately if only the same current across them. The resistor can be formed from the small-signal resistance for a diode-connected device which values is proportional to the square root of the bias current. Through calculation and simulation, the parameters of the LPF are as follows: $R = 937 \Omega$, $C1 = 633 \text{ pF}$, $C_P = 49 \text{ pF}$.

Bias generator can continuously adjust the controlled voltage and produces the bias voltage of buffer stage to adjust the bias current providing the correct swing limit for the VCO buffer stage. It is used of a differential amplifier and a half-buffer replica to realize a feedback path to produces V_{BP} and V_{BN} from V_C as shown in Fig. 4. It also uses an additional half-buffer replica providing a buffered version of controlled voltage at the V_{BP} output inducing controlled voltage from LPF to VCO. V_{BP} defines the lower voltage swing limit of the delay stage outputs. This output isolates controlled voltage from potential capacitive coupling in the buffer stages. We also add a capacitor which can filter the voltage perturbation.

5 Simulation and results analysis

A low jitter self-biased PLL is designed in SMIC 0.13 μm CMOS technology. It has been successfully demonstrated and its size is $750 \mu\text{m} \times 460 \mu\text{m}$. Fig. 5 shows the die photo, in the layout design the low frequency digital parts are on the bottom left while the high frequency analog parts are on right. Several MOS capacitors between them are introduced for isolating.

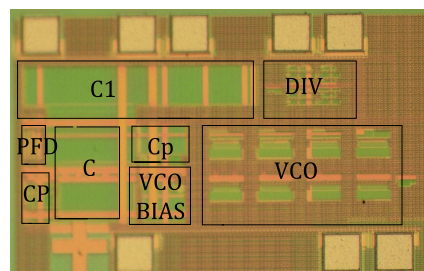


Fig. 5. Die photo of the PLL

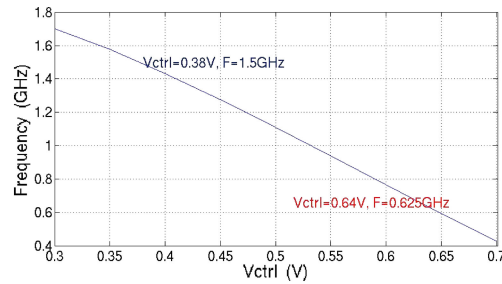


Fig. 6. Tuning curve of the VCO

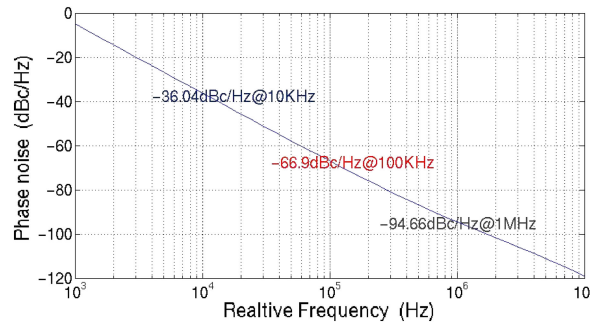


Fig. 7. VCO phase noise @1.25 GHz

As can be seen from Fig. 6 and Fig. 7, the tuning range of the VCO is from 625 MHz to 1.5 GHz, and phase noise of VCO at 1.25 GHz is -94.66 dBc/Hz at 1 MHz, -66.9 dBc/Hz at 100 kHz and -36.04 dBc/Hz at 10 kHz, respectively, satisfied with the specification of the low jitter. As can be seen from Fig. 8, the RMS jitter is 3.53 ps and peak-to-peak jitter is 21.19 ps at 1.25 GHz. All these measurement results show that the proposed circuit is a good choice for low jitter PLL.

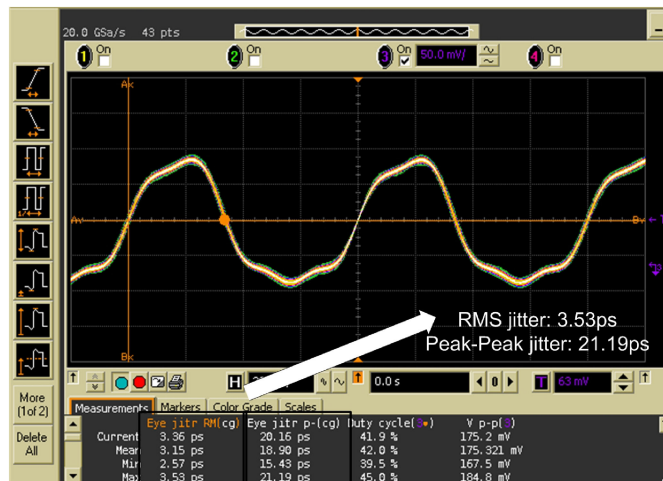


Fig. 8. The test results of PLL jitter @1.25 GHz

Self-biased PLL has the merit that can remove all of the process technology and environment variability. The performance summary and comparison with other PLL is shown in Table I. From Table I, we can confirm that the RMS jitter is much

less than the nearly frequency such as in [6, 8, 9], peak-to-peak jitter is much less than the nearly frequency such as in [6, 7, 8, 9]. And the VCO phase noise is much less than [8] at 1 MHz. This PLL has the same performance as the PLL in [10] with LC-VCO which has the large power and large area.

Table I. Performance comparison

	this	6	7	8	9	10
CMOS Technology	130 nm	65 nm	65 nm	65 nm	180 nm	180 nm
Frequency (GHz)	0.625–1.25	0.47–1.13	0.9–1	0.64	1.6	1.2–1.4
Phase noise of VCO	–94.66 dBc/Hz @1 MHz	—	–102 dBc/Hz @1 MHz	–88.6 dBc/Hz @1 MHz	—	–127.2 dBc/Hz @1 MHz
RMS jitter (ps@GHz)	3.53 @1.25	5.13 @0.8	3.10 @0.95	9.6@ 0.64	8.789 @1.6	—
P-P jitter (ps@GHz)	21.19 @1.25	46.2 @0.8	27.6 @0.95	52.2 @0.64	45 @1.6	13.65 @1.2

6 Conclusion

This paper proposed a low jitter PLL. Some new circuits were adopted to improve its performance. A novel charge pump was employed to reduce the current mismatching. And the second capacitor was added to filter the ripple of the controlled voltage. The simulation and test results show that at 1.25 GHz the RMS jitter is 3.53 ps, the peak-to-peak jitter is 21.19 ps and the phase noise of VCO at 1 MHz offset is –94.66 dBc/Hz.