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LETTER

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A large input range source-follower based bi-quad filter cell

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Abstract: A novel large input range source-follower based bi-quad filter cell is proposed offering an additional degree of freedom to the position of the poles and zeros. Simulation results of a 4th order fully differential elliptical filter in a 0.13 μm CMOS technology confirm a power consumption of 160 μA @ 1.2 V, an IIP3 of 6.3 dBm and a steepness of 177 db/decade.

Keywords: source-follower based filter, continuous-time filter, bi-quad, linearity

Classification: Integrated circuits

References

[1] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter With 79-db DR," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2713–2719, Dec. 2006.

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[3] Y. Chen, P. Mak, and Y. Zhou, "Source-follower-based bi-quad cell for continuous-time zero-pole type filters," *Proc. 2010 IEEE Int. Symp. Circuits and Systems*, pp. 3629–3632, June 2010.

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1 Introduction

Modern portable wireless communication devices suffer from limited battery autonomy, while new functionality is unceasingly added. To sustain this evolution, performance and power consumption of the circuits used must improve. Adequate filtering of incoming signals with high selectivity and high linearity increases the receivers' overall dynamic range and loosens linearity requirements of subsequent signal processing blocks, hence, allowing

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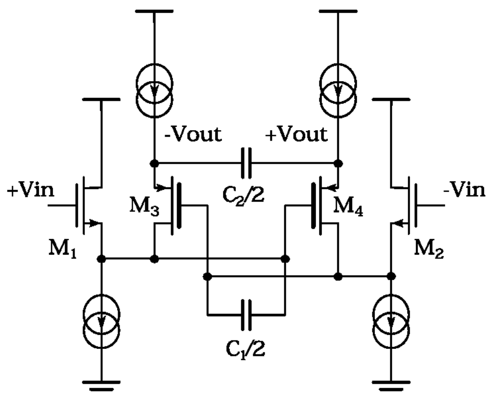
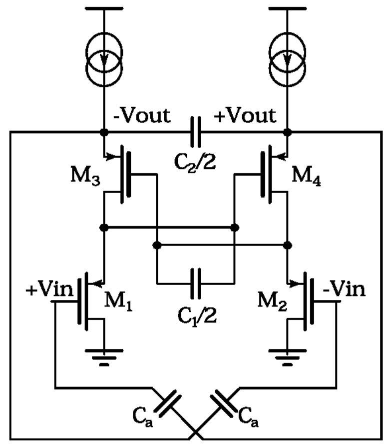
to increase the overall power efficiency. In [1], the authors present a source-follower based Gm-C topology to realize low-power active filters while keeping nonlinearity low (see Fig. 1.a).

In [2], the authors modified the topology presented in [1] to increase linearity for large input signals, increasing the dynamic range while maintaining the same lower power consumption (see Fig. 1.c). The topologies of both [1] and [2], however, clearly lack the possibility to offer zeros in their transfer functions, hindering implementation of e.g. Chebyshev II and elliptic filter stages. In [3], two cross-coupled feedthrough capacitors are added to yield those necessary zeros. Though only partly, as when the transconductances of the transistors are kept equal only imaginary zeros occur (see Fig. 1.b).

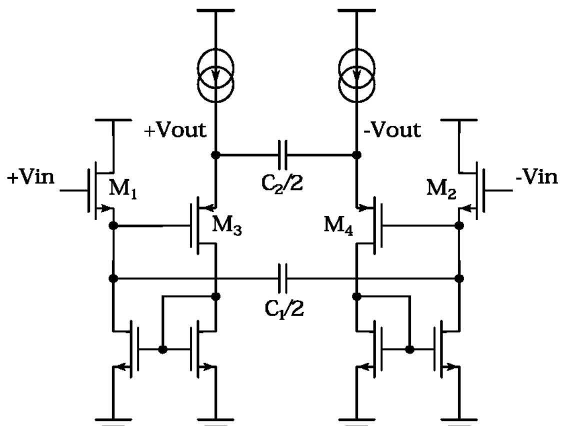
As is clear in [3], the transconductance of the pMOS and nMOS transistors could be used as an additional degree of freedom, though this would affect the noise performance. Furthermore, tuning the transconductance of pMOS and nMOS transistors separately is hard to realize in the improved topology of [2]. This letter proposes a new source-follower based filter architecture with large input range, that offers complex zeros, without relying on transconductance inbalance. Complex zeros are required for bandpass/bandstop filters.



(a) Folded version of source-follower-based filter in[1]



(b) Topology limited to imaginary zeros[3]



(c) Topology with improved input range[2]

Fig. 1. Comparison of previously published source-follower-based filters

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2 Proposed bi-quad cell

We propose the topology in Fig. 2.a. The transfer function of the circuit in Fig. 2 is found by applying Kirchoff's current law on V_x and V_{out}, yielding eq. (1), assuming $g_m = g_{m,n} = g_{m,p}$ for the transconductances of transistors M_{1-4}. It can easily be shown that mathematically either C_a, C_b or C_c could be omitted to obtain the desired zeros. Practically, however, the superfluous degree of freedom allows to find realizable values for the capacitances. Additionally, one could rewire C_a, C_b and/or C_c to be crosscoupled or not, yielding minor changes in the analytical transfer function below, but again increasing the likelihood to find manufacturable capacitance values. In case all crosscoupling can be avoided, the circuit becomes suitable for single-ended operation if desired.

$$TF = \frac{\frac{(-C_a+C_c)C_b+C_c(C_a+C_1)}{g_m^2}s^2 + \frac{C_a-C_b}{g_m}s + 1}{\frac{(C_a+C_c+C_1+C_2)C_b+(C_c+C_2)(C_a+C_1)}{g_m^2}s^2 + \frac{C_b+C_a+C_1}{g_m}s + 1} \qquad (1)$$

Expressing the coefficients of eq. (1) in terms of conventional 2nd order LTI system parameters and solving for a given value of C_a yields the following expressions for the remaining capacitances (with transconductances of transistors M_{1-4} equal and denoted by g_m, $\omega_{n,p}$ the angular resonance frequency of resp. zeros and poles, and $Q_{n,p}$ the quality factor of resp. zeros and poles):

$$C_1 = \frac{g_m}{\omega_n Q_n} + \frac{g_m}{\omega_p Q_p} - 2C_a \qquad (2)$$

$$C_2 = \frac{\omega_p g_m Q_p}{\omega_n^2 Q_n^2} + \frac{g_m}{\omega_n Q_n} - \frac{\omega_p Q_p g_m}{\omega_n^2} + \frac{g_m Q_p}{\omega_p} - \frac{\omega_p C_a Q_p}{\omega_n Q_n} - C_a \qquad (3)$$

$$C_b = C_a - \frac{g_m}{\omega_n Q_n} \qquad (4)$$

$$C_c = \frac{\omega_p Q_p C_a^2}{g_m} - \frac{\omega_p C_a Q_p}{\omega_n Q_n} + \frac{\omega_p Q_p g_m}{\omega_n^2} \qquad (5)$$

By varying C_a over a range of feasible values, the other capacitance values can be determined. If no desirable solution would be found, one can modify the crosscoupling as mentioned earlier and modify the above expressions accordingly. All capacitances should be large enough to limit the influence of parasitic –often strongly non-linear– capacitances.

3 Results

A two-stage, 4th order elliptical filter was implemented by cascading and correctly dimensioning two stages of the proposed architecture. These filters offer very steep slopes, because of the combination of closely spaced poles and zeros. The zeros are imaginary and complex conjugate. This constraint considerably reduces the complexity of the former equations, as from eq. (1) we obtain $C_a = C_b$ and in eq. (2)-(5) this corresponds to dropping all terms containing Q_n.

Initially, the poles of first and second stage are to be at $-43.7 \pm j38.2$ MHz and $-11.2 \pm j69.7$ MHz respectively, and the zeros at 225 MHz and 102 MHz respectively. For the sake of stability and improved linearity, the circuit was

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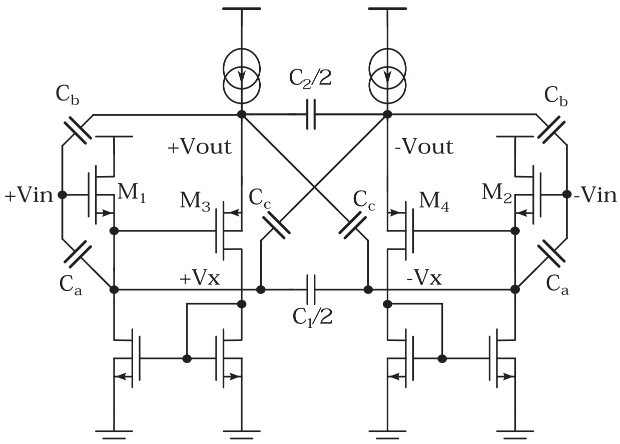
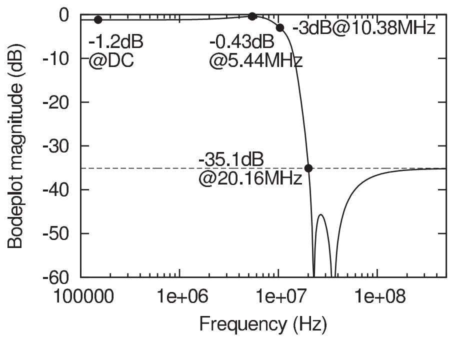


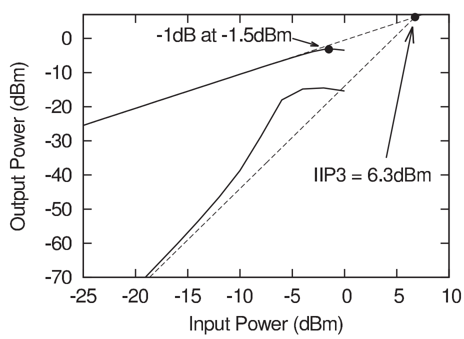
(a) Topology

	Stage 1	Stage 2
C_a	100 fF	100 fF
C_b	100 fF	100 fF
C_c	200 fF	2.2 pF
C_1	6.1 pF	1 pF
C_2	4 pF	2.1 pF
g_m	250 μS	250 μS

(b) Dimensioning



(c) Simulated response



(d) Simulated linearity

Fig. 2. Proposed source-follower based filter

manually fine-tuned to slightly reduce the Q factors of both stages, limiting peaking in the frequency response of the individual stages. As peaking corresponds to amplification, higher Q factors result in higher voltage swings on internal nodes (for a given input signal strength), which drastically reduces linearity and possibly causes stability issues because of the positive feedback [4]. The new locations of the poles for first stage and second stage are at $-29.1 \pm j38.2$ MHz and $-28 \pm j104.6$ Mhz respectively, the zeros at 225 MHz and 153 MHz respectively. The corresponding component values are listed in Fig. 2.b. Additionally, the mirrors were dimensioned to have a high output impedance to reduce the impact of channel length modulation on the linearity.

The design has been validated by means of simulations in a 0.13 μ CMOS technology, with 1.2 V supply voltage. The filter consumes merely 80 μA (=96 μW) per stage and consists of 2 stages. Cut-off frequency is at 10.4 MHz, the pass-band ripple equals 0.8 dB and 35 dB supression is reached at 20 MHz. The input referred noise is 318.5 μVrms. In a 100 ohm environment, the 1 dB compression point is reached at -1.5 dBm input power, and the input referred IP3 point is estimated around 6.3 dBm for two equally strong tones at 4.7 MHz and 5 MHz respectively. The frequency response and linearity figures are shown in Fig. 2.c-d. Table I compares these results to previously published results.

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Table I. Performance Comparison

	This work	[1]	[2]	[3]
Technology	0.13 μm	0.18 μm	0.13 μm	0.18 μm
Supply (V)	1.2	1.8	1.2	2
Current (μA)	160	2280	80	1500
Cut-off (MHz)	10.4	10	250	2.75
Steepness (dB/decade)	177	66 (est.)	63	66 (est.)
1-dB compression point (dBm)	-1.5	-4	-0.3	-
Input referred IP3 point (dBm)	6.3	17.5	22	5
Input referred noise (μVrms)	318.5	24	444	70
Poles and zeros	4P+4Z	4P	4P	4P+4Z*
# biquad stages	2	2	2	2

* only purely imaginary zeros

Clearly different trade-offs were made for the 4 filters in the comparison. The particular technology node in which the filters were implemented has little impact on the filter performance, as none of the transistors is given minimum dimensions, as the transistors in de current mirrors need a sufficiently high output impedance and the filter linearity improves by reducing the effect of channel length modulation in the source followers [1]. Power consumption, however, directly influences the noise performance. In [1], D'Amico shows that noise decreases as the size of the capacitors increases and eq. (1) clearly shows that scaling up all capacitors requires the transconductance to be scaled up by the same factor to obtain the original transfer function, i.e. increasing the current. The cut-off frequency also has an impact on this trade-off as it is proportional to the ratio of the transconductance and the capacitors.

The most notable result, however, is the selectivity. The steepness reported in the table was estimated close to cut-off frequency, where supression is most cricital. The table shows that a low-power filter has been realized with an abrupt frequency response using a single bi-quad cell, while previous work would require far more stages to obtain a similar selectivity. Obviously increasing the number of stages increases power consumption and noise, and impacts linearity. Additionally, limiting the number of stages will reduce the number of capacitors, and the associated die area. This is especially important considering the previously mentioned relation between capacitor size and noise performance.

4 Conclusion

A true biquad, source-follower based filter with improved large signal linearity is presented. The filter offers 2 complex poles and 2 complex zeros in a single biquad stage, without increasing the power consumption with respect to previous work [1, 2, 3]. A 4th order elliptical filter was designed based on this new topology and simulations were performed to confirm correct

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