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A novel methodology for speeding up IC performance in 32 nm FinFET

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Abstract: This paper presents a novel methodology for IC speed-up in 32 nm FinFET. By taking advantage of independently controlling two gates of IG-FinFET, we develop the boosting structures that can improve the signal propagation on interconnect significantly. Furthermore, the circuit area and power dissipation issues are also taken into account. With the addition of boosting path, the full booster can reduce the delay of interconnect as much as 50% while consuming merely more than 18% of power. In the high-speed and low-power IC designs, the proposed boosting structure gives circuit designers several options in the trade-off between the power consumption and high performance which play an important role in application-specific integration circuits in the 22 nm node and beyond.

Keywords: FinFET, double gate, high performance, booster, speed up

Classification: Integrated circuits

References

[1] F. He, et al., "FinFET: From compact modeling to circuit performance," *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, pp. 1–6, 15–17, Dec. 2010.

[2] M. C. Wang, "Independent-Gate FinFET circuit design methodology," *IAENG International Journal of Computer Science*, vol. 37, no. 1, 2010.

[3] M. Fan, et al., "Investigation of Cell Stability and Write Ability of FinFET Subthreshold SRAM Using Analytical SNM Model," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1375–1381, June 2010.

[4] A. Datta, A. Goel, R. T. Cakici, H. Mahmoodi, D. Lekshmanan, and K. Roy, "Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, pp. 1957–1966, Nov. 2007.

[5] E. G. Friedman and M. A. El-Moursy, "Optimum wire sizing of RLC interconnect with repeaters," *Integration, the VLSI Journal*, pp. 205–225, 2004.

[6] Y. Cao, PTM, [Online] http://ptm.asu.edu/

[7] M. Alioto, "Comparative Evaluation of Layout Density in 3T, 4T, and MT FinFET Standard Cells," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 5, pp. 751–762, May 2011.

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1 Introduction

The rapid development of digital IC nowadays has made a great demand on chip manufacturers in speeding up the performance while consuming no extra energy. There are numerous approaches to enhance the chip operation and the interconnect delay has become one of the biggest bottlenecks in high speed ICs. Therefore, dealing with interconnect lines is crucial for speed-up. The conventional CMOS repeater was introduced as a promising technique to reduce the delay of signal propagation. Furthermore, the emergence of FinFET provides a thriving solution in the scalability of IC designs to replace the traditional MOSFET because of its powerful ability in controlling leakage and minimizing short channel effects while delivering a strong drive current [1]. The additional back gate of FinFET gives IC designers more alternatives. For instance, if the transistor is ON (the front gate voltage is V_{DD} for N-type), the back gate can be biased to V_{DD} to generate a bigger current that can speed up the switching. Similarly, the back gate can be biased to GND (or even negative) when the transistor is OFF (the front gate voltage is 0 for N-type) to alleviate leakage current. To achieve this, we can simply tie the front gate and back gate together. The FinFET configured this way is called a shorted-gate FinFET or SG-FinFET [2]. On the other hand, with two separate gates, FinFET can be controlled flexibly, and most recent circuit research, such as SRAM [3], concentrate on exploiting the back gate biasing to improve the circuit performance.

From an interconnect perspective, we develop a novel architecture to boost the signal propagation speed by using the repeater that consists of two independent gate (IG) FinFET inverters. The back gates of P-type and N-type FinFET are tied together to form the back gate of IG-FinFET inverter as shown in Figure 1 a. The proposed architecture is validated by comparing the performance and power consumption with the conventional CMOS repeaters and SG-FinFET repeaters. The paper is organized as follows: Section 2 briefly introduces the characteristics of IG-FinFET. Section 3 proposes the boosting structures to improve IC performance, and Section 4 concludes our work.

2 IG-FinFET Characteristics

Flexible controlling of threshold voltage (V_{TH}) is known as a noteworthy attribute of IG-FinFET for IC designers to apply in high performance IC fabrication. Our research focuses on using such properties, particularly, utilizing one gate to control the threshold voltage of the other gate to speed up the chip operation dynamically. Extracted from the I-V characteristic with constant current approach, the front gate's threshold voltage as a function of back gate voltage (V_{bg}) for 32 nm N-type FinFET is illustrated in Figure 1. It clearly demonstrates that the front gate's threshold voltage is drastically decreased if V_{bg} is high or the threshold voltage increases as the V_{bg} decreases. Increasing V_{bg} to more than 0.3 V leads to a 40% reduction in V_{TH} meaning that switching takes place faster. The researchers in [3] and [4]

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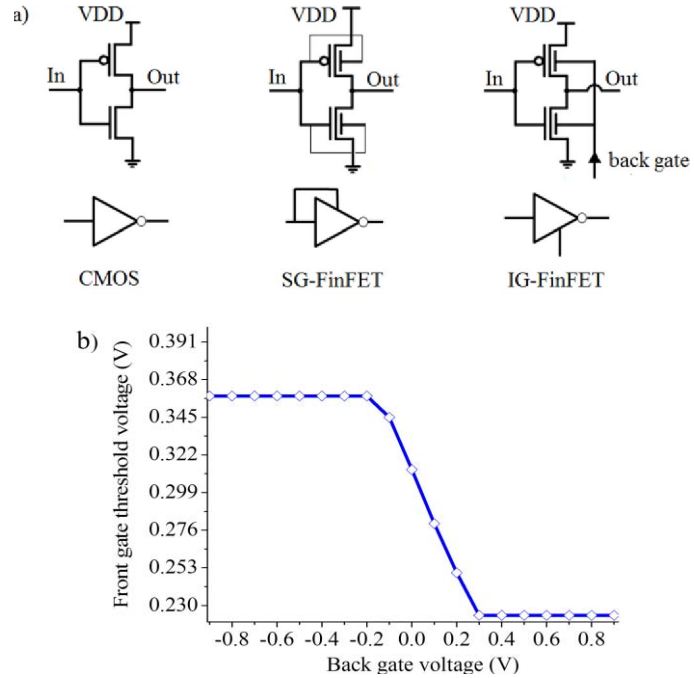

Fig. 1. a) Three types of inverters in this paper b) The front gate's threshold voltage as a function of back gate voltage for N-FinFET

succeeded in taking advantage of this characteristic of FinFET to synthesize the circuitry, therefore, significantly reducing the number of transistors.

From circuit design perspective, a double-gate FinFET can be considered as two MOS transistors connected in parallel. Hence, the overall switching speed of the FinFET device depends on the V_{TH} of the front gate that drives signals while the back gate takes on the responsibility of adjusting V_{TH}. This observation of the controllable threshold voltage of FinFET reveals that the signal transmission on the critical path can be boosted as long as we lower the V_{TH} of the front gate before the signal reaches the gate terminal.

3 Novel structure for high performance digital IC

The foregoing discussion demonstrates that if the V_{TH} of IG-FinFET is forced to be reduced before the arrival of the input signal at the front gate, the propagation through the transistor will happen more rapidly. The key point is that the V_{TH} is already controlled to wait for the propagating signal in the critical path. Based upon this observation, we propose a novel architecture to boost the speed of signal, thus improving the performance of digital IC.

Figure 2 a shows the conventional repeaters to drive a long interconnect using CMOS or SG-FinFET devices. Each segment of interconnect with a specific dimension (0.116 *um* thickness and height, 0.061 *um* width and space, variable length (i.e. *L um*) and 2.8 dielectric constant) is inserted between two repeaters by the distributed RC model and computed as in [6]. For high performance, as shown in Figure 2 b, we develop a novel configuration by forming the first stage with a SG-FinFET repeater while IG-FinFET

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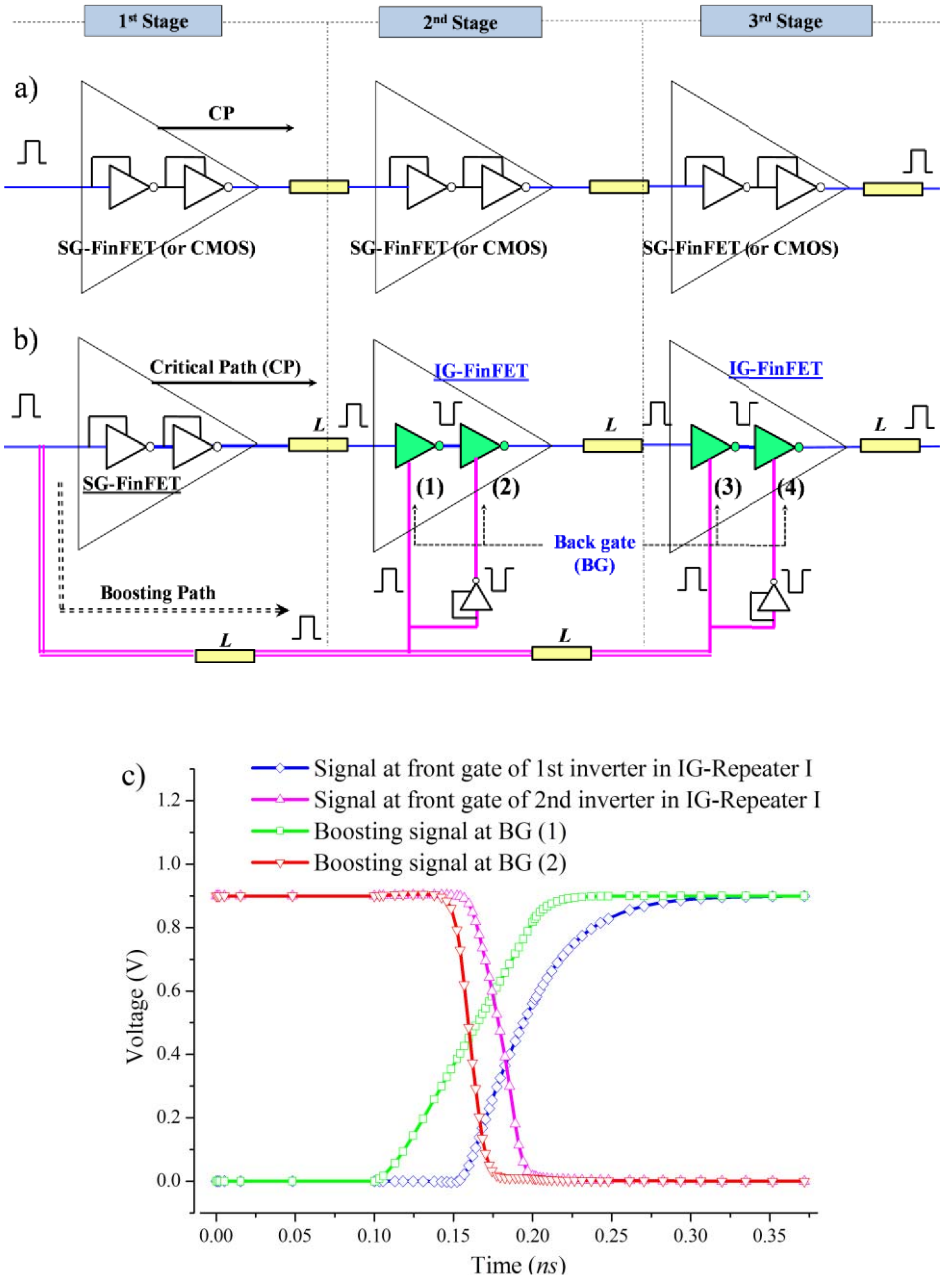

Fig. 2. The structures to improve the signal propagation: a) Repeaters with SG-FinFET (or CMOS), b) Full booster with IG-FinFET; c) Signals at front gates of 1st, 2nd inverters of IG-Repeater I and the boosting signals at BG (1) and BG (2)

repeaters are utilized for the second and third stage. These repeaters are named IG-Repeater I and IG-Repeater II, respectively. Each IG-Repeater has two back gates from two inverters inside it, namely BG (1), BG (2) of IG-Repeater I, and BG (3), BG (4) of IG-Repeater II (Figure 2 b). In addition, another path called a boosting path is extracted from the input and ends at IG-Repeaters' back gates. This boosting path runs parallel to the critical path. From Figure 2 b, it is noted that the length of the boosting path ($2L$) equals two-third lengths of the critical path ($3L$). One more SG-

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FinFET inverter is added before BG (2) and BG (4) so that the boosting signal has the same value as the input signal of the second inverter in each IG-Repeater. This configuration is named the full booster.

As can be seen in Figure 2 b, the input signal follows two directions: the critical path and the boosting path. Assuming that the delay of inverter and interconnect segment are t_{inv}, t_i, respectively. The signal on critical path spends $(2t_{inv} + t_i)$, $(3t_{inv} + t_i)$ arriving at the first and second inverters of IG-Repeater I, and $(4t_{inv} + 2t_i)$, $(5t_{inv} + 2t_i)$ arriving at the first and second inverters of IG-Repeater II, respectively. Meanwhile, it merely takes t_i, $(t_{inv}+t_i)$, $2t_i$, and $(t_{inv}+2t_i)$ for the signal on the boosting path to appear at BG (1), BG (2), BG (3), and BG (4), respectively. Note that the signal on the boosting path arrives at IG-FinFETs' back gates in advance, as a result, lowering the V_{TH} to accelerate the transmission of the signal on the critical path.

Using HSPICE, we generate the netlist of the booster structure with 32 nm FinFET that is extracted from [6]. Since the designs of IG-Repeater I and IG-Repeater II are identical, we only show the waveforms of the input and the boosting signal of IG-Repeater I (Figure 2 c). As expected, the boosting signals at BG (1) and BG (2) arrive earlier than the input signals of the first and the second inverters of IG-Repeater I, thus our preceding claim is verified. To provide circuit designers more options regarding the trade-off between performance and circuit area, a simpler boosting configuration is created by employing only BG (1) and BG (3), it is named single booster. Particularly, instead of boosting both inverters of IG-Repeater in the full booster, the single booster only affects the first inverters in each repeater, thus saves the circuit area by eliminating the SG-FinFET inverters before BG (2) and BG (4). The following section will discuss the performance, circuit layout, and power consumption of proposed booster in more detail.

4 Experimental evaluation and simulation results

We compare the performance of the repeater structures (two conventional designs: 32 nm MOSFET, 32 nm SG-FinFET and two novel designs: 32 nm IG-FinFET with a single booster and a full booster) to evaluate our proposals.

Normalized delay measurements for a wide range of the interconnect lengths including the proposed structures are shown in Figure 3. At a short interconnect (i.e., $L = 100\,um$), while using repeaters with SG-FinFET brings only a 10% speedup compared to the bulk CMOS technology, the single booster can reduce the delay as much as 40%; especially, the full booster alleviates it by over 50%. When each segment becomes longer (i.e. $L = 500\,um$), our proposed structures still enhance the repeaters' speed effectively by 20% and 30% with less propagation delay of single booster and full booster scheme, respectively.

From a circuit layout perspective, in Figure 2 b, the boosting architecture has a large circuit area as a result of the addition of the routing and SG-FinFET inverters in the boosting path. Furthermore, the utilization

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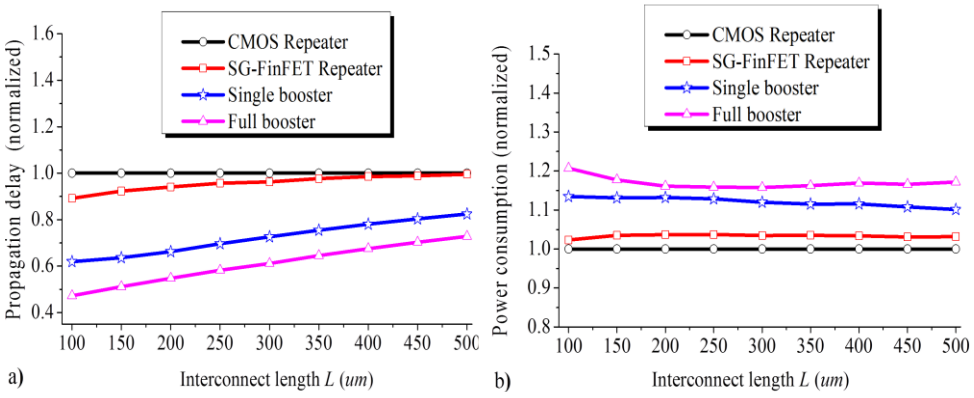

Fig. 3. a) Propagation delay comparison, b) Power consumption comparison

of FinFET technology instead of conventional bulk CMOS also leads to the growth of the layout area. Particularly, in comparison with 4X 32 nm-CMOS inverters, the specifications of 32 nm-FinFET devices (for both SG- and IG- FinFET) are set up as follows: $L_{FIN} = 32\,nm$, $H_{FIN}/T_{Si} = 2$, $W_{FIN}/W_{FIN\text{-}min} = 4$ where L_{FIN}, H_{FIN}, W_{FIN} are the length, height, width of the fin, respectively; and T_{Si} is the thickness of the silicon. By such given parameters, it is demonstrated in [7] that the layout area of IG-FinFET is roughly equal to 1.5 times one of 4X CMOS whereas SG-FinFET and CMOS device occupy the same area. Note that IG-FinFET has larger layout since in addition to three conventional terminals (i.e., gate, drain and source) of bulk CMOS as well as SG-FinFET, the appearance of back gates necessitates more occupation for their contacts. Additionally, the increment of layout area causes more power being consumed and Figure 3 b shows the power consumption comparison of boosters' architectures normalized to CMOS repeater. It is indicated that the single booster and the full booster consumed about 10% and 18% more power, respectively than the CMOS repeater scheme at 1500 um of total interconnect length ($3L$).

In general, to employ the booster circuits to drive a long interconnect (i.e., $3L > 1500\,um$), the boosters can be assembled in series such that each one only takes responsibility to drive a short interconnect (300-1500 um). As a result, this booster technique can be applied to any interconnect line with an arbitrary length.

5 Conclusion

This paper has introduced a novel methodology for IC speed-up in 32 nm FinFET. By taking advantage of independently controlling two gates of IG-FinFET, we developed the boosting structures that can improve the IC performance significantly. Moreover, the circuit area and power dissipation issues are also considered. With the addition of a boosting path and the 1.5 times larger layout of the 32 nm IG-FinFET compared to 32 nm bulk CMOS, the full booster can reduce the delay of interconnect as much as 50% while consuming merely more than 18% of power than the conventional CMOS.

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Therefore, the proposed technique may play an important role in high speed IC, especially since the critical path delay lowers overall performance of the chips. The effect of this technique on overall power consumption and layout optimization requires further research.

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