

LOW POWER ANALOG MULTIPLIER USING MIFGMOS

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Received 2012-07-07, Revised 2012-09-09; Accepted 2013-05-14

ABSTRACT

A novel 4-quadrant analog multiplier using Floating Gate MOS (FGMOS) transistors operating in saturation region are implemented. Floating gate MOSFETs are being utilized in a number of new and existing analog applications. These devices are not only useful for designing memory elements but also we can implement circuit elements. The main advantage in FGMOS is that the drain current is proportional to square of the weighted sum of input signals. By using conventional transistors we obtain only few hundred mill volts range of the supply voltage and when we go for square law devices we obtain up to 50%. So in order to get 100% range of the supply voltage we go for FGMOS. This can be obtained by the control voltage applied at the gate of the FGMOS. This simulation is done with the SPICE tools.

Keywords: VLSI, MOSFET Circuits, MOS Logic Circuits, MOS Integrated Circuits, Transistors Operating, Quadrant Analog, Drain Current, Supply Voltage, Saturation Region, Voltage Applied

1. INTRODUCTION

Four quadrant analog multipliers are important building blocks neural networks, fuzzy controllers, wireless communications and electronic systems such as voltage controlled oscillators and filters, modulation and demodulation circuits, adaptive filters, automatic gain control, frequency mixers. They can be used for waveform generation and modulation and power measurements. Other typical applications also include the implementation of dividers and square-rooters, through feedback configuration. Several techniques of implementing four-quadrant analog multipliers, using MOS technology, have been reported. They are the variable transconductance technique (modified Gilbert cell) (Liu and Hwang, 1994; Pena-Fino and Connelly, 1987; Song and Kim, 1990) the voltage-controlled transconductance technique, which employs MOS transistors operating in the triode region (Kim and Park, 1992; Saxena and Clark, 1994; Bult and Wallinga, 1986) the bias feedback technique (Wong *et al.*, 1986), techniques based on square-law characteristics of MOS transistors operating in the saturation region,

implementing either the quarter-square identity (Wang, 1991; Garimella *et al.*, 2008; Jamuar *et al.*, 2011) or other algebraic identity. The Gilbert Six Transistors Cell (GSTC), using the variable transconductance technique, is very popular in bipolar technology since its output current has a linear relationship with the tail current source which allows the nonlinear relationship with the input signals, V_x and V_y , to be compensated simply by an appropriate pre-distortion circuit. However, the output current of a MOS transistor multiplier, based on the modified GSTC, has a nonlinear relationship with the tail current source and makes compensation by a pre-distortion circuit very difficult (Pena-Fino and Connelly, 1987). This limits the linear input range of the multiplier to only a few hundred mill volts (Liu and Hwang, 1994). On the other hand most of the square-law based multipliers reported so far have input signal range limited to about 50% of the supply voltage.

In this study, a novel four-quadrant analog multiplier using Floating-Gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS

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transistor is used to implement the quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0078% and THD of maximum 2.74% (while the inputs are at their maximum values) Rest of the study is organized as follows. In section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS four-quadrant analog multiplier and. Simulation results of the proposed circuit are shown in section III and conclusion in section IV the reference for this research work is available in section V.

1.1. The FGMOS Transistor

The basic structure of the FGMOS transistor is shown in Fig. 1a. It consists of a-channel MOS transistor with a floating gate (first polysilicon layer) over the channel and in some cases extending over to the field oxide area.

An array of control gates (multiple input gates) are formed by the second polysilicon layer over the floating-gate. The capacitive coupling between the multiple input gates and floating-gate and the channel is shown in Fig. 1b.

Figure 1a An illustration of the cross-section structure of a MF MOS transistor with three inputs. (b) Capacitive model of the MF MOS transistor. (c) Symbolic representation of a three input MF MOS transistor. The large signal behaviour of an FGMOS can be obtained by combining a standard MOS model for the same technology with the equation that relates VFG to Vi, Vd, VS, Ci, CGD, CGS and CGB. This equation can be obtained by applying the charge conservation law to the Floating node (FG). If there is an infinite resistance between the FG and all the surrounding layers, there will be no leakage current between them and so, the FG will be perfectly isolated. Under this assumption the voltage at the FG is given by Equation (1):

$$\left[V_{FG} = \sum_{i=1}^N (C_i / C_T) V_i + (C_{GS} / C_T) V_S + (C_{GD} / C_T) V_D + (Q_{FG} / C_T) \right] \quad (1)$$

where, term CT refers to the total capacitance seen by the FG and is given by Equation (2):

$$C_T = C_{FD} + C_{FS} + C_{FB} + \sum_{i=1}^N C_i \quad (2)$$

The equations modelling the large signal behaviour of the FGMOS can now be obtained by replacing Vgs in the equations describing the large signal behaviour of the MOS transistor, with the expression describing the voltage between the FG and source which can be obtained by referring VFG to the source terminal rather than the bulk.

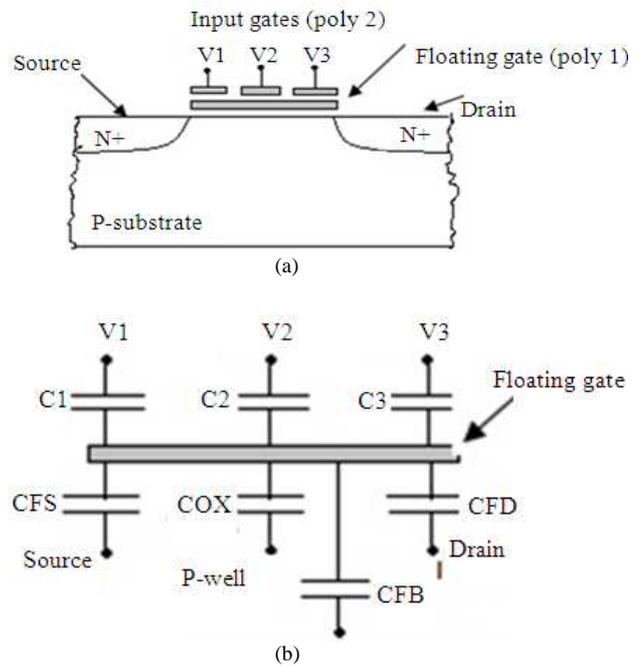


Fig. 1. MOS structure

The equation for the drain current of the FGMOS transistor in saturation is Equation (3):

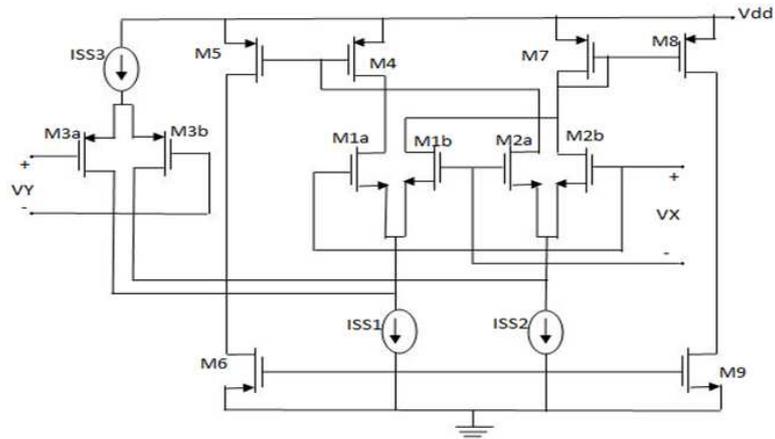
$$I_d = 0.5k \left(\sum W_i V_i + W_b V_b - W_s V_s - W_T V_T^* \right)^2 \quad (3)$$

where the capacitive coupling ratios:

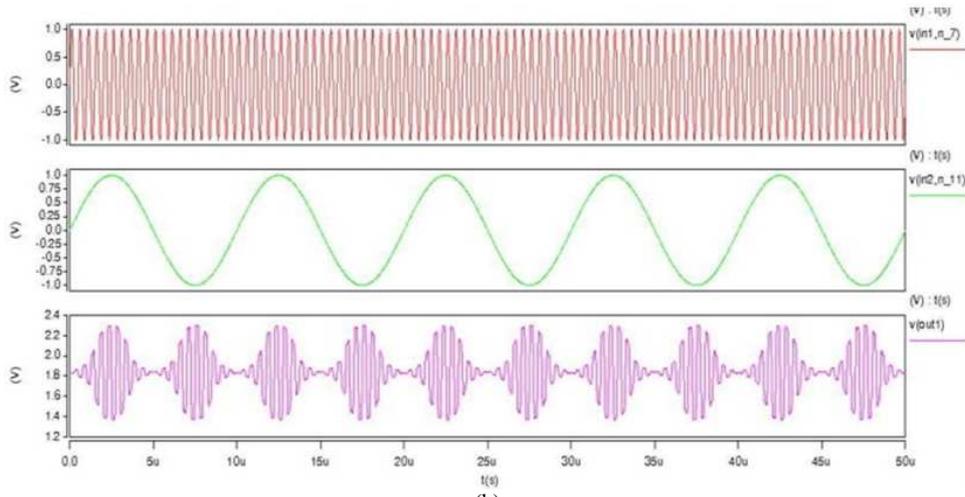
$$\begin{aligned} W_i &= (C / C_T), \\ W_b &= (C_{FB} / C_T), \\ W_s &= [1 - (2/3) (C_{FS} / C_T) - (2/3) (C_{ox} / C_T)] \\ W_T &= 1 - (2/3) (C_{ox} / C_T) \end{aligned} \quad (4)$$

where, VT* is the threshold voltage seen from the floating-gate, K = μn COX (W/L) is the trans-conductance parameter, μn is the electron mobility and L is the channel length. CT is the total capacitance associated with the floating gate.

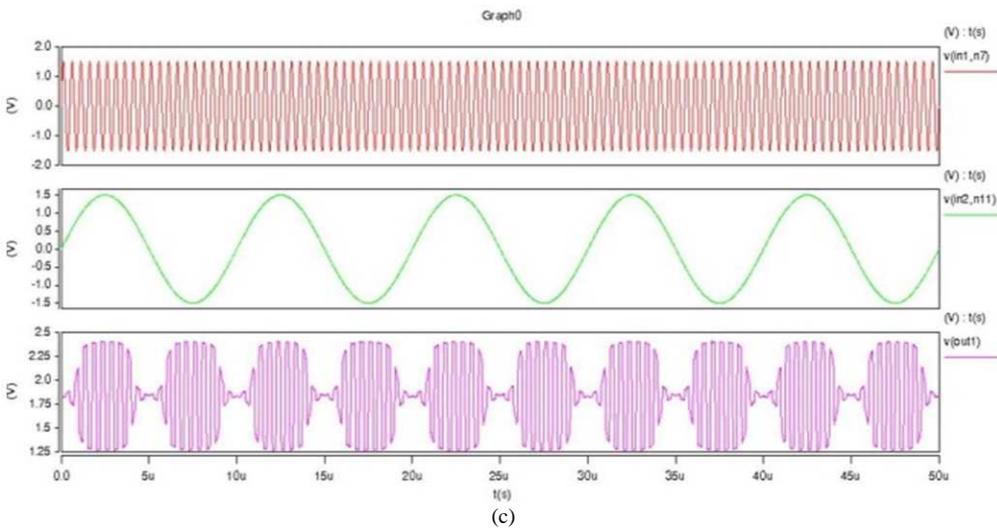
Equation 4 shows that the FGMOS transistor drain current in saturation is proportional to the square of the weighted sum of the input signals, where the weight of each input signal is determined by the capacitive coupling ratio of the input.



(a)



(b)



(c)

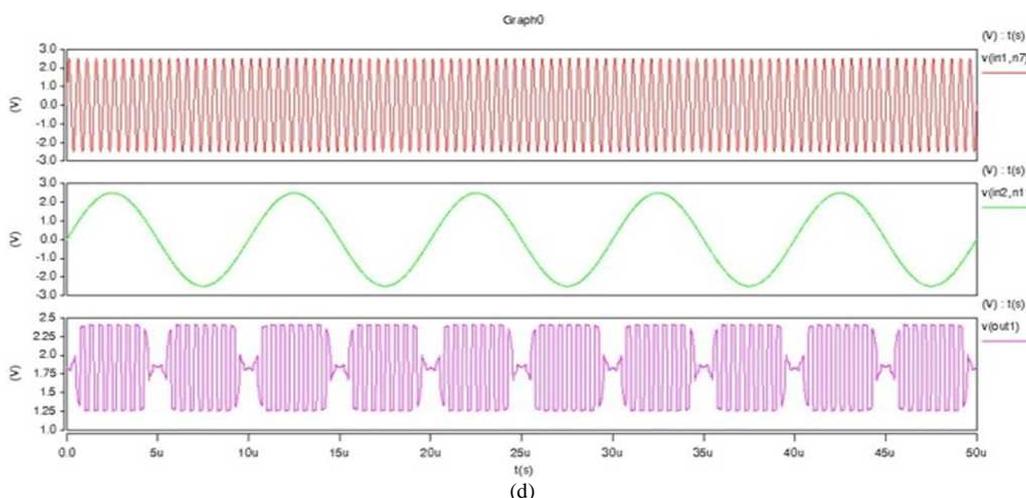


Fig. 2. Conventional multiplier

2. EXISTING FOLDED COMS-MULTIPLIER

Figure 2a shows the conventional multiplier circuit based on the folded CMOS Gilbert Cell while Fig. 3a shows the proposed floating gate multiplier circuit which is based on the topology given in (Pena-Fino and Connelly, 1987), employing FGMOS differential pairs instead of conventional pairs to improve the circuit behaviour. M1a, M1b transistors form one differential pair where as M2a, M2b form the other. They are cross connected by connecting the drains of the transistors M1a, M2a and M1b, M2b together. A differential input VX is applied to the cross connected differential pairs while the other differential input VY is applied to the differential pair formed by M3a and M3b. M3a and M3b transistors form tail transistors for the two differential pairs. The bias currents (ISS1, ISS2 and ISS3) are provided as tail currents to the differential pairs.

2.1. Simulation Results

The proposed circuit Fig. 3 was simulated using MCNC 1.25um CMOS Process. The supply voltage is $V_{DD} = 5V$, VGC is set to 0.5v the tail currents are $I_{SS1} = I_{SS2} = 350 \mu A$ $I_{SS3} = 100 \mu A$. The input capacitor value is taken $C_i = 4pF$ while the C_{FGD} and C_{FGS} values are calculated as 59.24f and 0.5540p, respectively. The dimension for cross connected differential pair transistors M1a, M1b, M2a and M2b is $W/L = 2.5 \mu m/250 \text{ nm}$, for M3a and M3b is $W/L = 2.5 \mu m/250 \text{ nm}$.

For conventional multiplier, when the linear input range is limited to the 50% of the supply voltage range. Simulation results at input range less than 50% of supply voltage is shown in Fig. 2b.

For conventional multiplier, when the linear input range is limited to the 50% of the supply voltage range. Simulation results at input range equal to the supply voltage is shown in Fig. 2c.

For conventional multiplier, when the linear input range is limited to the 50% of the supply voltage range. Simulation results at input range greater than the supply voltage is shown in Fig. 2d.

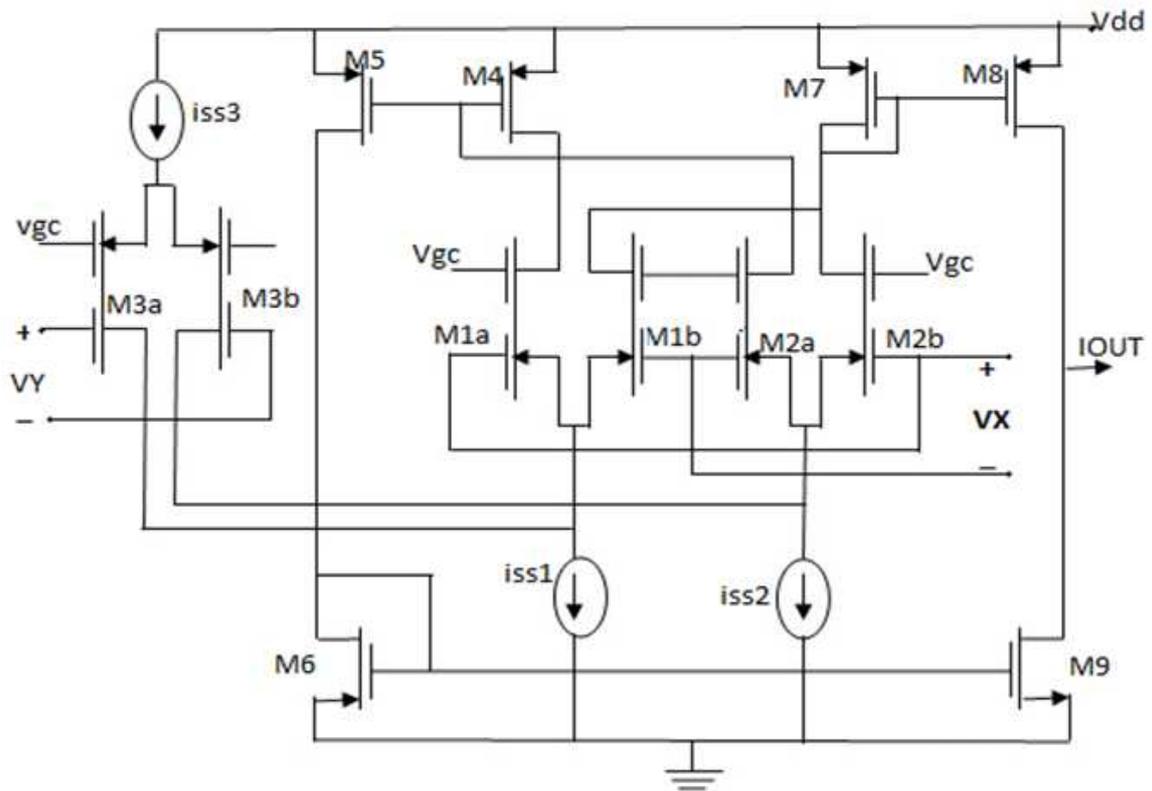
3. PROPOSED FGMOS TRANSISTOR-MULTIPLIER

Each transistor in differential pairs has two inputs which are applied through two equal sized capacitors, C_i . The differential signals of the inputs are applied to one of the floating gates in the differential pairs. VX and VY act as input signals while VGC as a control voltage to the floating gates.

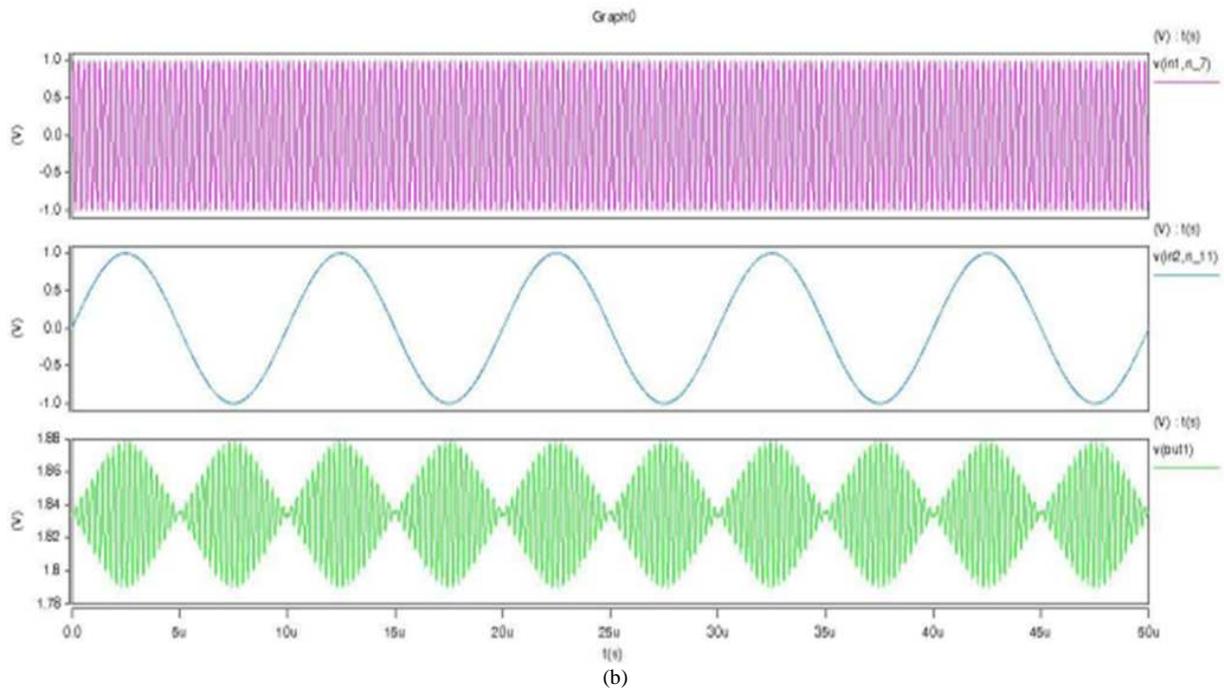
Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

3.1. Simulation Results

For proposed multiplier, large input signal range equal to 100% of the supply voltage. Simulation results at input range less than 50% of supply voltage is shown in Fig. 3b.



(a)



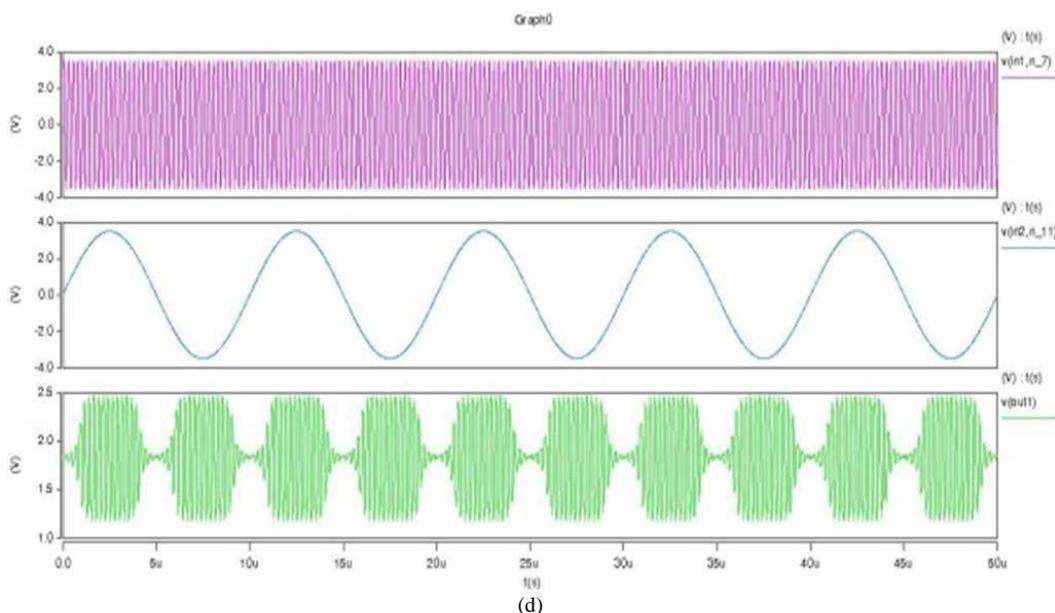
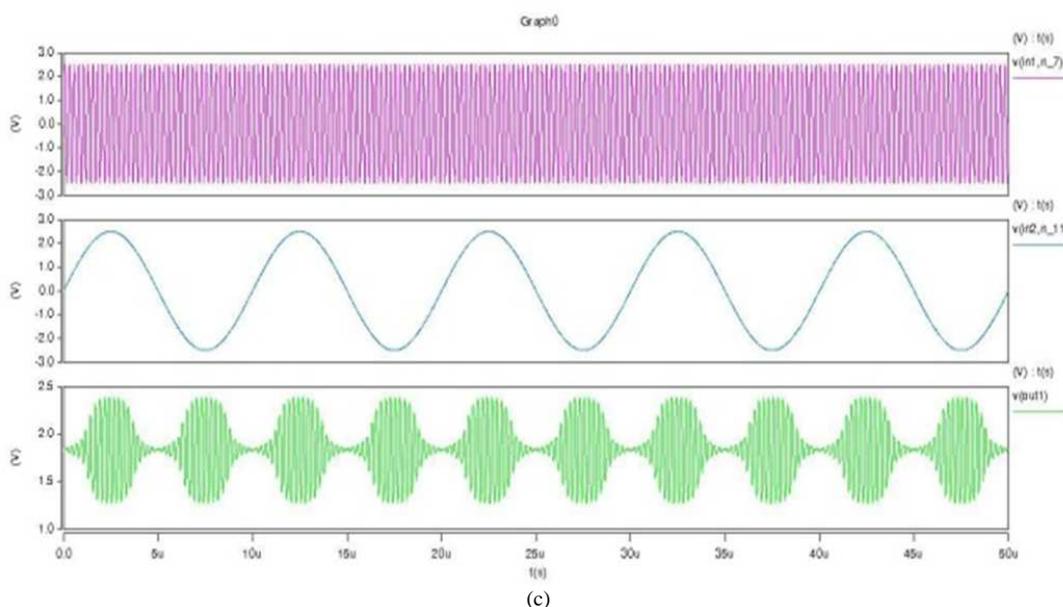


Fig. 3. Proposed multiplier

For proposed multiplier, when the input signal range is equal to 100% of the supply voltage. Simulation results at input equal to the supply voltage is shown in **Fig. 3c**.

For proposed multiplier, when the input signal range is equal to 100% of the supply voltage. Simulation results at input greater than the supply voltage is shown in **Fig. 3d**.

3.2. Power Analysis

For conventional multiplier, when the linear input range is limited to the 50% of the supply voltage range:

- VVy1 from time 1e-009 to 5e-00
- Average power consumed -> 4.441178e-012 watts
- Max power 1.094650e-008 at time 4.56687e-006

- Min power 1.976560e-021 at time 5e-005

For proposed multiplier, when the input signal range is equal to 100% of the supply voltage range:

- VV1 from time 1e-009 to 5e-005
- Average power consumed -> 1.250723e-008 watts
- Max power 1.516830e-004 at time 2.52469e-006
- Min power 4.881126e-017 at time 5e-005

4. CONCLUSION

A novel FGMOS four quadrant multiplier has been designed and simulated. It is based on the square law dependence of the drain current on the weighted sum of the input signals. The circuit configuration is remarkably simple. It has a large input voltage range equalling the supply voltage. The measured nonlinearity and total harmonic distortion are 0.0078 and 2.74% under full scale input conditions, respectively. With low power consumption for high power input range.

5. REFERENCES

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