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A low noise regulated charge pump circuit

Wonseok Oh[a)] **and Praveen Nadimpalli**

RF Micro Devices, Inc.

6825 W. Galveston Dr. Chandler, AZ. 85248 U.S.A

a) *wonseok.oh@rfmd.com*

Abstract: In this work, a low noise regulated charge pump circuit is presented. The proposed charge pump uses a digital frequency shaped clock scheme to spread tonal energy of the oscillator to overall frequency ranges, and reduces the output noise of the charge pump, and improves the power efficiency. To achieve constant output voltage during an over loading condition, the proposed charge pump utilizes feedback. The proposed charge pump generates 4.1 V $\sim$ 4.4 V output voltage and provides 30 mA current driving capability with 30 mV ripple at 2.5 V $\sim$ 3.5 V supply line. At 800 MHz $\sim$ 2.2 GHz ranges, the output noise power of the proposed charge pump is at least 11.4 dBm less than that of a charge pump with normal clock.

Keywords: charge pump, low noise, frequency shaped clock, regulator

Classification: Integrated circuits

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1 Introduction

The tonal energy of switching clock from the oscillator leaves its signature at the charge pump output. Its signature introduces the output ripple voltage of charge pump and deteriorates the performance such as linearity and noise figure of the circuitry (LNA, Mixer, synthesizer, and so on) that uses the output of the charge pump as a supply line, and a regulator is usually followed to suppress the ripple voltage [1, 6]. The output ripple voltage is determined by the output capacitor and switching clock of the charge pump. The ripple voltage can be reduced by increasing switching frequency or by increasing output capacitance. Each scheme has its own limitations and drawbacks. Switching frequency cannot be blindly increased without decreasing the charge pump's efficiency since the efficiency is inversely proportional to switching clock frequency. Also, increasing the output capacitance will reduce the output ramp-up time adversely. In addition, the tonal energy of switching frequency and its harmonics appear as noise at the output of the charge pump. The tonal energy of the switching frequency and its harmonics should be minimized to reduce the output noise of the charge pump at high frequency. Therefore, switching clock, output ripple, speed and efficiency are trade-offs in charge pump design [2, 3, 4, 5, 6]. In addition, the charge pump circuit should provide constant output voltage while the supply line and load condition vary.

This paper proposes a low noise charge pump circuit. The proposed charge pump circuit utilizes a frequency shaping clock scheme to minimize switching clock tonal energy at the output of the charge pump with improving the charge pump's efficiency. To achieve constant output voltage, a regulated charge pump circuit is presented utilizing a feedback scheme like low dropout (LDO) regulator configuration.

2 Circuit design

Figure 1 shows the single phase charge pump model and its output and clock spectrum according to normal clock and proposed frequency shaped clock. As seen in Fig 1, the normal clock signal, $Clk(t)$, injected into the charge pump has a very high energy tone and harmonics. This clock energy and its spurs appear at the output of the charge pump. In single phase charge pumps, highest energy component at the output of charge pump is the same frequency as the injected clock signal. These spurs deteriorate the performance of the system at high frequencies, especially LCD driver, antenna switch modules and power amplifiers (PAs) of RF systems.

To minimize the tonal energy of clock and its spurs, frequency shaped clock signal, $FS(t)$, is utilized the $\Delta\Sigma$ modulator which spreads tonal energy to overall frequency ranges. The modulated clock (driver) is called a frequency or noise shaped clock (driver). The proposed charge pump improves power efficiency since the $\Delta\Sigma$ modulator is digital logic which means there is no static current consumption and clock frequency spread the overall frequency range. This section describes the frequency shaped clock driver and

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regulated charge pump architecture in detail.

2.1 Digital frequency shaped clock driver

The digital frequency shaped clock driver is implemented by using ΔΣ modulation technique. The power consumption of digital frequency shaped clock driver does not consume static power. Figure 1 (b) shows the model of the first-order frequency shaped ΔΣ modulator. The 1-bit pseudo-random bit signal (PRBS) functions as a pseudo-random dither input to the digital ΔΣ modulator. The digital adder produces a 1-bit signal, which is the MSB of the output of the 2-bit adder and hence is equal to the sum of the 1-bit digital signal and the 2-bit error feedback data on the 2-bit bus. As such, the MSB of the adder output signal actually functions as a digital quantizer, and then is connected directly to the first adder. The output signal is applied to

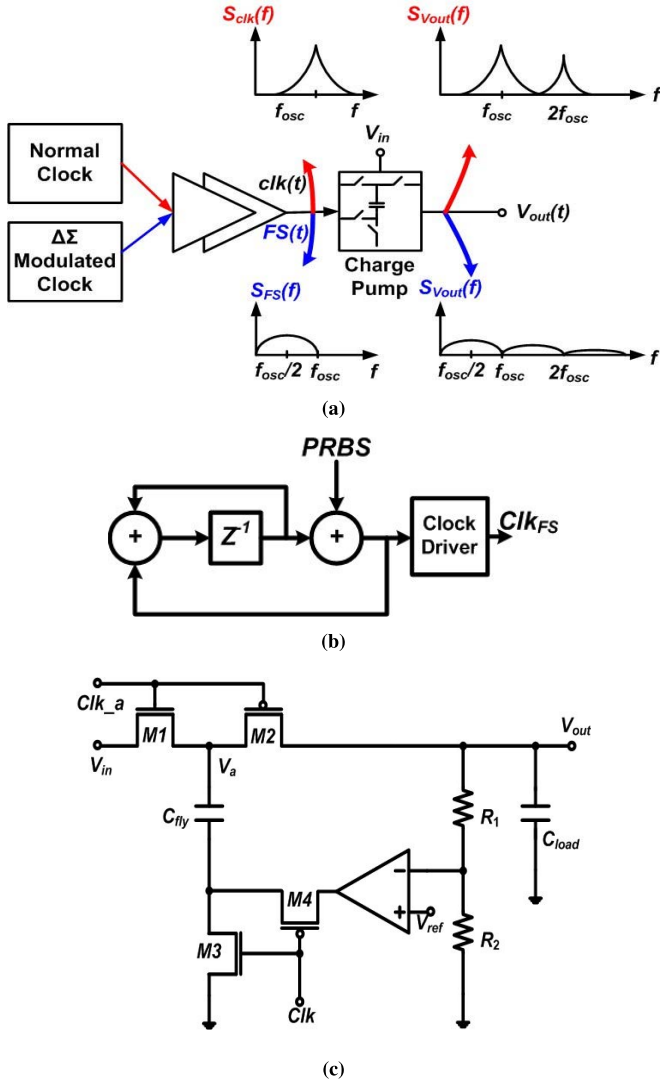

Fig. 1. (a) The charge pump model with clock and output spectrum according to normal and frequency shaped clock, (b) The model of first order frequency shaped ΔΣ modulator, (c) The proposed regulated single phase charge pump architecture

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the (-) input of the 2-bit digital adder to provide the feedback necessary to accomplish the frequency shaping referred to above. The output of the ΔΣ modulator is also connected to the input of a digital logic circuit, which is a clock driver that generates the switching clock of the charge pump. As the power spectrum of the frequency shaped clock, $S_{FS}(f)$, shows in Fig 1 (a), a frequency-shaping pseudo-random clock generator attenuates low frequency noise. In the high frequency region, the high frequency tone coupling is minimized at f_{clk} where the largest high-frequency tones are observed. After passing through the first order digital frequency shaper (ΔΣ modulator), the PSD of the frequency shaped clock $S_{FS}(f)$ becomes

$$S_{FS}(f) = \left|1 - z^{-1}\right|^2 S_{PN}(f) = \frac{1}{f_s}\left|2\sin\left(\frac{\pi f}{f_s}\right)\right|^2 \left|\frac{\sin\left(\pi f/f_s\right)}{\pi f/f_s}\right|^2$$

As seen from the equation, the DC component of the clock is eliminated by high pass filtering provided by the first order digital frequency shaper, and fundamental and higher harmonics of the clock are spread over a broad frequency spectrum between DC to the sampling frequency ($f_s = f_{clk}$) in Fig 1 (a) and 2 (a). In other words, modulation clock frequency is dithered from DC to oscillation frequency. Therefore, the efficiency of charge pump with frequency shaped clock should be improved than that of charge pump with normal clock in the cost of low frequency noise.

2.2 Single phase regulated charge pump circuit

The DC supply circuitry should provide constant voltage at any battery voltage and load conditions. In order to achieve the constant output of a charge pump in any condition, a regulated charge pump utilizing feedback network is proposed. The proposed charge pump can be configured as a single or bi-phase architecture. The single phase charge pump is shown in Fig 1 (c). The op-amp has rail-to-rail input and output stages based on current-mirror amplifier architecture and its unity gain frequency is twice higher than sampling frequency of ΔΣ modulator (fosc). The output voltage line of the op-amp varies from VDD−0.5 V ∼ VDD−1.5 V depending on the VDD line (2.5 ∼ 3.5 V) according to supply line (2.5 ∼ 3.5 V) due to feedback network. The clock signals, Clk and Clk_a, are the same phase, but Clk_a has twice the voltage swing ($0 \sim 2 * V_{in}$) of $Clk(0 \sim V_{in})$. M1 and M2 do not turn off if Clk is injected to their gate, since V_a and V_{out} are always higher than V_{in}. The output voltage, V_{out} is a function of R_1, R_2, and V_{ref} and is expressed as $V_{out} = (1 + R_1/R_2) * V_{ref}$. When Clk and Clk_a are high, M1 and M3 are on and M2 and M4 are off, and the fly capacitor (C_{fly}) charges V_{in}. The charge Q_C_{fly} stored at C_{fly} is $C_{fly} * V_{in}$. When Clk and Clk_a are low, M2 and M4 turn on. At this time, the stored charge is distributed to C_{load}. Total charge stored to C_{fly} and C_{load} is the same and defined as $(V_{in} + V_b) * C_{fly}/(C_{fly} + C_{load}) = V_{out} * C_{eq}$, where $C_{eq} = C_{fly}/(C_{fly} + C_{load})$ and V_{out} is set as $V_{in} + V_b$ and this output voltage is also the same as $V_{out} = (1 + R_1/R_2) * V_{ref}$. Therefore, the voltage of the

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bottom plate of C_{fly}, V_b, varies depending on V_{ref} and the ratio of R_1 and R_2.

The proposed charge pump architecture has two important characteristics. The first important feature is that $\Delta\Sigma$ modulator can be n-th order. Second, the maximum output power spectrum is at half of the clock frequency. If using a first order $\Delta\Sigma$ modulator, that is, $f_{\Delta\Sigma\_clk} = f_{osc}/(2n)$; n is number of order. In addition, a frequency shaped clock can be applied to bi-phase as well as single phase charge pump architectures.

3 Simulation and comparison

The proposed low noise regulated charge pump circuit is designed using 0.5 um standard digital CMOS process and the designed proposed charge

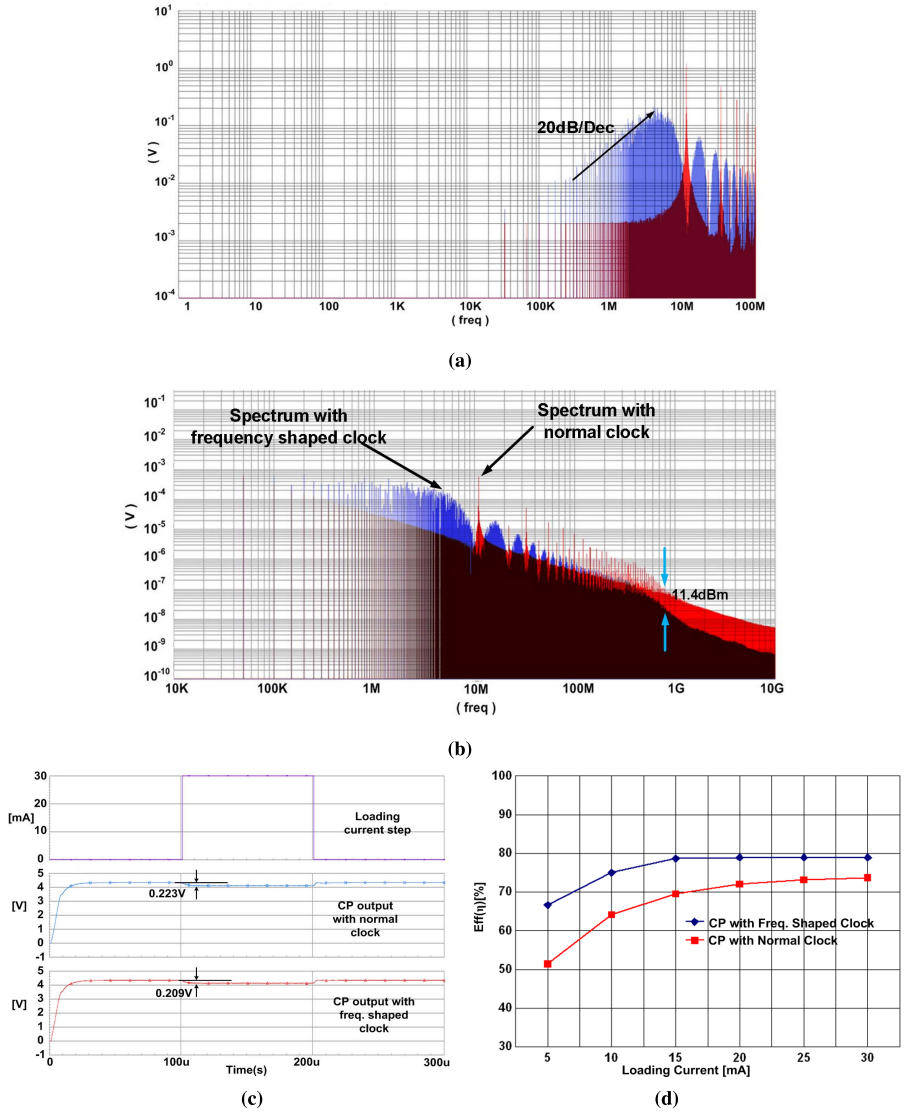

Fig. 2. Power spectrums of (a) the normal clock and frequency shaped clock for charge pump and (b) output power spectrums of charge pump using normal clock and frequency shaped clock (c) load transient response (d) efficiency comparison

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Table I. The performance comparison

	Regulated charge pump with normal clock	Regulated charge pump with frequency shaped clock
V_{in}	2.5~3.5V	
C_{fly}	50nF	
C_{out}	200nF	
I_{load}	0~30mA	
V_{out}	4.1~4.4V	
Max. Efficiency	73.5%	79.2%
Load Regulation	7.433mV/mA	6.967mV/mA
Max. Output Spurs	-41.4dBm @ f_{osc}=11MHZ <-127.8dBm @ 0.8~2.2GHz	-51.89dBm @ f_{osc}/2 <-139.2dBm @ 0.8~2.2GHz

pump is simulated using Cadence Spectre. In order to compare the performance of the proposed charge pump, the simulation has been done on the same charge pump circuit with a normal clock. The flying capacitor and load capacitor are 50 nF and 200 nF external components, respectively. Figure 2 (a) show the overlapped spectrum of the normal clock ($f_{osc} = 11$ MHz) and its frequency shaped clock, respectively. The tonal energy of the normal clock is spread over the frequency range and the slope of the output spectrum is 20 dB/dec. The frequency shaped clock shows less energy at the fundamental and harmonic frequencies compared to the normal clock. The peak energy of the normal clock is 1.199 V (14.59 dBm) at the fundamental frequency (f_{osc}) and the peak energy of the frequency shaped clock is 207.2 mV (−0.661 dBm) at half of the fundamental frequency ($f_{osc}/2$) due to the first order $\Delta\Sigma$ modulation technique. The peak energy of the frequency shaped clock is around 7 times less than that of the normal clock. Figure 2 (b) shows the output spectrums of the charge pump with normal and frequency shaped clock in the condition of maximum load (30 mA). The output power with normal clock is −41.4 dBm (1.902 mV_{rms}) and −61.78 dBm (182.1 uV_{rms}) at f_{osc} and 3rd harmonic ($3 * f_{osc}$), respectively and the output power with frequency shaped clock at $f_{osc}/2$ and the 3rd harmonic are −51.89 dBm (569.1 uV_{rms}) and −82.45 dBm (16.87 uV_{rms}), respectively. At high frequency ranges between 800 MHz ∼ 2.2 GHz, the highest output spectrum of the charge pump with frequency shaped and normal clock is −139.2 dBm (24.46 nV) and −127.8 dBm (91.08 nV), respectively. From the simulation, the output spurs of the charge pump with a frequency shaped clock is reduced by the factor of 3.4 ∼ 11.8 in the overall frequency ranges. The output voltage of the proposed regulated charge pump is achieved 4.1 V∼4.4 V range with 0 ∼ 30 mA current capability at 2.5 V to 3.5 V supply line. As seen in Fig. 2 (c), load regulation of the charge pump with a frequency shaped and normal clock is 6.967 mV/mA and 7.433 mV/mA, respectively. Fig. 2 (d) shows the comparison of efficiency. The efficiency of the charge pump with a frequency shaped clock improved 6% at heavy loading condition. Table I shows the performance comparison of the regulated charge pump with normal and frequency shaped clock.

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4 Conclusion

In this paper, a novel regulated charge pump circuit with a digital frequency shaped clock is presented. The proposed charge pump has less effect on the ripple voltage and does reduce spurs significantly owing to digital frequency shaped clock generator using $\Delta\Sigma$ modulation technique. In addition, the proposed charge pump has better power efficiency. Owing to feedback scheme, the proposed charge pump provides regulated output voltage while supply line and load condition vary.

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