ELectronics EXpress

IEICE Electronics Express, Vol.7, No.16, 1175–1181

Novel Eight-Transistor SRAM cell for write power reduction

C.M.R. Prabhu[a)] **and Ajay Kumar Singh**

Faculty of Engineering & Technology, Multimedia University

Jalan Ayer Keroh Lama, 75450 Melaka, Malaysia

a) *c.m.prabu@mmu.edu.my*

Abstract: This paper presents a novel 8T SRAM cell which contains two tail transistors in the pull-down path of the respective inverter to minimize the write power consumption. The simulated results show that the proposed cell consumes about 57.87% lower power and gives faster response compared to the conventional 6T SRAM cell during a write operation. To compensate the read delay and static noise margin (SNM) losses due to the two extra tail transistors in the proposed cell, we have to enlarge the width of these two tail transistors.

Keywords: low power, SRAM cell, write/read delay, write power, stability and static noise margin

Classification: Integrated circuits

References

[1] N. S. Kim, D. Blaauw, and T. Mudge, "Quantitative analysis and optimization techniques for on-chip cache leakage power," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 10, pp. 1147–1156, 2005.

[2] C. Senthipari, K. Diwakar, C. M. R. Prabhu, and A. K. Singh, "Power deduction in digital signal processing circuit using inventive CPL subtractor circuit," *ICSE 2006*, proc. 2006 Kuala Lumpur, Malaysia, pp. 820–824, Dec. 2006.

[3] M. Yamaoka, R. Tsuchiya, and T. Kawahara, "SRAM circuit with expanded operating margin and reduced stand-by leakage current using Thin-BOX FD-SOI transistors," *IEEE J Solid-State Circuits*, vol. 41, no. 11, pp. 2366–2372, Nov. 2006.

[4] S. Inaba, H. Nagano, K. Miyano, I. Mizuushima, Y. Okayama, T. Nakauchi, K. Ishimaru, and H. Ishiuchi, "Low-power logic circuit and SRAM cell applications with silicon on depletion layer CMOS (SODEL CMOS) technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1455–1462, June 2006.

[5] A. Chandrakasan, W. J. Bowbill, and F. Fox, "Design of High Performance Microprocessor Circuits," *Wiley-IEEE Press*, p. 584, 2000.

[6] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of SRAM cells for nanometer technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, Nov. 2006.

[7] Y. Chang, F. Lai, and C. Yang, "Zero-aware asymmetric SRAM cell for reducing cache power in writing zero," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 8, pp. 827–836, Aug. 2004.

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010

[8] R. E. Aly and M. A. Bayoumi, "Low-power cache design using 7T SRAM cell," *IEEE Trans. Circuits Syst.*, vol. 54, no. 4, pp. 318–322, April 2007.
[9] Z. Liu and V. Kursun, "Characterization of a Novel Nine-Transistor SRAM cell," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 4, pp. 488–492, Aug. 2008.
[10] E. Sicard, "Microwind and Dsch version 3.0," Published by INSA Toulouse France, April 2005. [Online] http://www.microwind.org.
[11] E. Seevinck, "Static noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 5, pp. 748–754, Oct. 1987.
[12] A. Bhavnaganwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, April 2001.

1 Introduction

SRAM represents a major portion of chip, and it is expected to increase in portable devices and high performance processors in the future. To achieve a high-performance, a higher stability for portable devices and a longer lifetime of the battery, low power circuit design is a necessity [1, 2]. Low voltage configurable SRAM cells with low-power consumption are mainly desired. Over the years, SRAM has undergone tremendous advancement [3, 4]. Low power design techniques [5, 6] are based on reducing the voltage swing level and capacitance. SRAM cells include both read and write operations. Since, read operations occur more frequently than the write operations, most low power techniques focus on read power saving. However, the write power consumption is usually higher than the read power consumption due to the large power dissipation in driving the cell bitlines to full swing. Recently, there have been efforts in characterizing cell stability and power reduction during a write '0' operation [7, 8, 9].

A new 8T SRAM cell with reduced write power consumption and write access delay is proposed in this paper. The proposed SRAM cell contains two extra nMOS tail transistors in the pull-down path of their respective inverter. The pull-down path of one of the inverter is disconnected to avoid discharging of the respective bitline during a write operation. All the results are simulated in a CMOS 0.12 μm technology using MICROWIND3 CAD tools. The write power consumption of the novel 8T SRAM cell is roughly reduced by 57.87% compared to the conventional 6T cell.

2 Proposed circuit description

The schematic of the proposed cell, which contains two nMOS tail transistors N5/N6 in the pull-down path of their respective inverter, is shown in Fig. 1 (a). The switching behavior of these two transistors is controlled by the logic levels at BL and nBL. The write operation of the 8T SRAM cell depends on disconnecting the pull-down path of one of the inverter. In the novel 8T cell, no extra signal is used as proposed by others [7, 8]. The layouts of the 6T and 8T SRAM cells, as shown in Fig. 1 (b), are drawn in

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010

standard 0.12 μm CMOS design technology. Our proposed SRAM cell has an area overhead of 16% due to additional two tail transistors. Compared to the conventional cell, the wordline and the bitlines interconnect capacitances are increased in the proposed cell due to increase in horizontal and vertical dimensions. Because, the percentage of cell array to cache area is about 70%, the overall cache overhead is roughly (16% x70%) = 11.2% due to the proposed cell. The detail operation of the 8T SRAM cell is presented in the following.

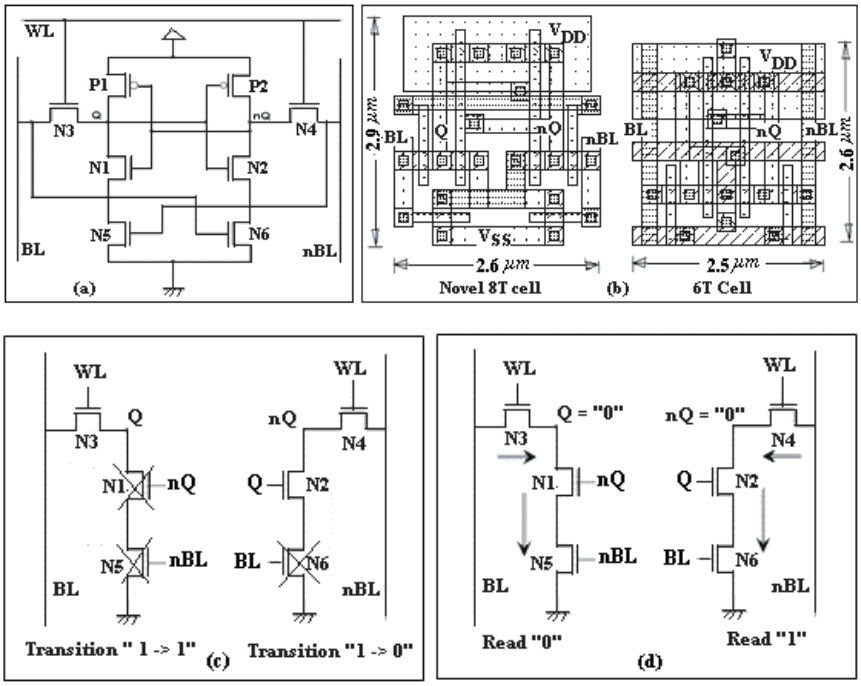


Fig. 1. (a) Novel 8T SRAM cell, (b) Cell Layout, (c) Write mode and (d) Read path

The write operation starts by disconnecting the pull-down of one of the two inverters. The data to be written is determined by the bitline voltage. To write "1" at node Q the bitline has to be set at BL = "1". Now assert WL to high. Here, we will consider two cases. Case I: writing the cell state Q from 1 to 1, i.e. a 1 → 1 transition. Since both Q and BL are at a logic high, such a transition is not possible. Case II: writing the cell state from 0 to 1, i.e. a 0 → 1 transition. Since nBL = "0," transistor N5 turns OFF and disconnects the pull-down path of inv.1 which flips the node Q to high without waiting for the bitline to discharge completely. A write "0" can be performed by setting BL = "0" and asserting WL to high. The first possible case consist of writing cell state from "0" to "0". Since nQ and nBL are at logic high, such transition is not possible. Another write transition, namely 1 → 0 can be easily performed by transistor N6. Since, BL = 0, N6 turns OFF and disconnects the pull-down path of the inv.2 which flips the node nQ to high without waiting for the nBL to discharge completely. A read operation typically involves precharging the bitlines followed by reading the

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010

contents of the cell through the access transistors.

3 Simulation results and discussions

We have performed the simulation of write/read operations with BSIM4 based transistor models in a 0.12 μm logic process technology. The threshold voltage of nMOS (pMOS) is set to 400 mV. The 6T/ZA cell and 8T cell are compared considering various SRAM metrics. In simulation, the widths of all the transistors are adjusted to 240 nm, and $V_{DD} = 1.2$ V. Since, the access transistor size in the 8T cell and ZA cell [7] is the same as the conventional 6T cell, the bit line diffusion capacitance and wordline gate capacitance remain the same in both cells. The write simulations are performed considering power consumption, access delay and current through each transistor. The simulated results are given in Table I (a) and Table I (b). In the proposed cell, the overall power consumption is small compared to the 6T cell and ZA cell for $1 \rightarrow 1/0 \rightarrow 0$ write patterns. This is due to the absence of state transition and the reduced sub-threshold current. Subthreshold leakage current is small (Table I (b)) due to two OFF nMOS transistors (Fig. 1 (c)). This is known as stack effect. Stacking of transistors is an effective way to reduce the subthreshold leakage current [5]. In $1 \rightarrow 0/0 \rightarrow 1$ write patterns, power consumption is reduced due to absence of discharging activity at bitline (Table I (b)). The power dissipated in bitlines (due to increase in height of the proposed cell) is only a part of the total cache power consumption. The tag bitlines only contribute for about 3% to the total cache power consumption during a write operation [7]. The increased power consumption in the wordline of the proposed cell during write mode can be compensated by equalizing the width of 8T cell and the 6T cell layouts. Due to absence of state transition in $0 \rightarrow 0$ and $1 \rightarrow 1$, we only compare the write delay in case of $0 \rightarrow 1/1 \rightarrow 0$. The $1 \rightarrow 0/0 \rightarrow 1$ write transition delays of the new cell is lower than the conventional 6T cell and ZA cell (Table I (a)), due to one OFF transistor in the pull down path of the inverter which lowers the discharging/charging time of bitlines. To measure the write ability, we have varied the word-line voltage (V_{WL}) from high to low. It is observed (Table I (c)) that V_{WL} reduces the strength of access transistors (N3/N4) reduces thereby reducing the write ability. In the proposed cell, a write operation can be performed for a minimum V_{WL} value of equal to 0.62 instead of 0.81 V as in the conventional cell. A lower value of V_{WL} indicates a better write ability.

The read power consumption in the 8T SRAM cell is increased by 10% compared to the conventional cell due to an increase in the cell size which leads to larger wordline interconnect capacitance. The parasitic capacitance also increases due to wires used to connect the gates of tail transistors to BL/nBL, respectively. The additional capacitance due to increased bitline length slightly affects the bitline power during a read operation because only a small voltage difference is developed on the bitline [8]. The two ON nMOS transistors in the read critical path (Fig. 1 (d)) degrade the read access delay of the 8T SRAM cell due to an increase BL/nBL discharge time. This loss

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010

Table I. (a) Summary of power consumption for different input, (b) Summary of current for different input patterns, (c) Access transistor (I_{N3}) current

(a)

		WRITE OPERATION				READ OPERATION	
		0 ⟶ 0	0 ⟶ 1	1 ⟶ 0	1 ⟶ 1	Read "0"	Read "1"
Power (μW)	Conv. 6T	0.002	30.699	30.695	0.002	28.497	28.495
	ZA cell [7]	0.0025	31.498	6.646	0.0015	29.118	31.641
	Novel 8T	0.0005	18.195	18.191	0.0005	31.584	31.587
Delay (ps)	Conv. 6T	-	111	111	-	80	80
	ZA cell [7]	-	116	110	-	81	90
	Novel 8T	-	60	60	-	90	90

(b)

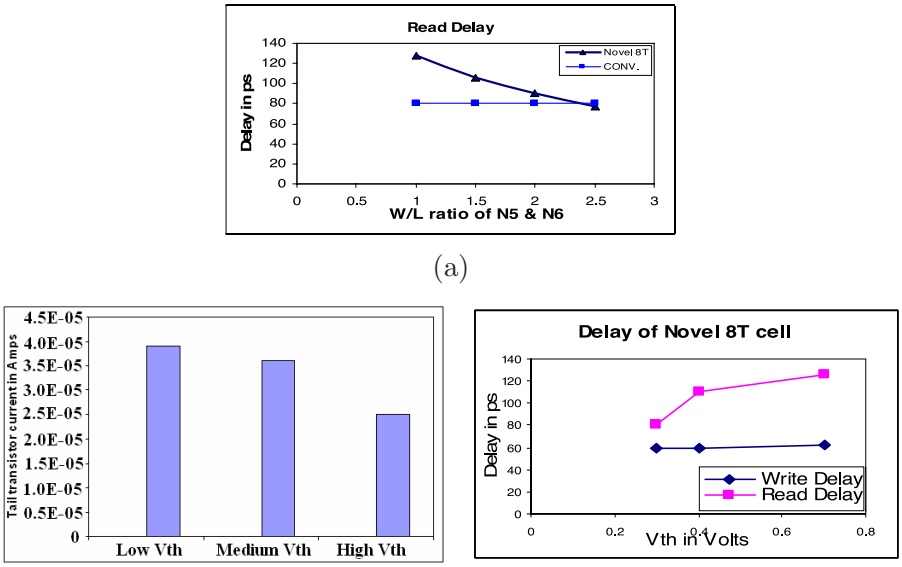
		WRITE OPERATION			
		0 ⟶ 0	0 ⟶ 1	1 ⟶ 0	1 ⟶ 1
Conv. 6T	I_{N3}	0.623nA	0.051mA	0.100mA	0.623nA
	I_{N4}	0.623nA	0.100mA	0.051mA	0.623nA
	I_{N1}	1.623nA	0.050mA	0.039mA	24.61nA
	I_{N2}	24.61nA	0.039mA	0.050mA	1.623nA
Novel 8T	I_{N3}	0.312nA	0.001mA	0.075mA	0.312nA
	I_{N4}	0.312nA	0.075mA	0.001mA	0.312nA
	I_{N5}	0.312nA	0.312nA	0.034mA	3.425nA
	I_{N6}	3.425nA	0.034mA	0.312nA	0.312nA
	I_{N1}	0.312nA	0.312nA	0.034mA	3.425nA
	I_{N2}	0.312nA	0.034mA	0.312nA	0.312nA

(c)

V_{WL} (volts)	I_{N3} in mA	
	Conv. 6T	Novel 8T
1.2	0.098	0.075
1.0	0.098	0.073
0.81	0.096	0.071
0.63	-	0.060
0.62	-	0.058

in delay can be compensated by enlarging the width of the tail transistors to 2.4xL (length of the channel) as seen in Fig. 2 (a). Due to an increase in the width of tail transistors, the write power consumption increases by less than 0.1%. In order to reduce the leakage current in the cell, the tail transistors must have a high threshold voltage (Fig. 2 (b)) because the performance degradation associated with high V_{th} tail transistor(s) is not very significant as seen in Fig. 2 (c). Fig. 2 (c) also shows that the write sensitivity of the proposed cell weakly depends on the threshold voltage variation of tail transistors. All the simulations are performed at T = 27°. The read ability is severely affected due to the variation in threshold voltage of the tail transistors. As threshold voltage varies from 0.3 V to 0.7 V, the read delay

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010



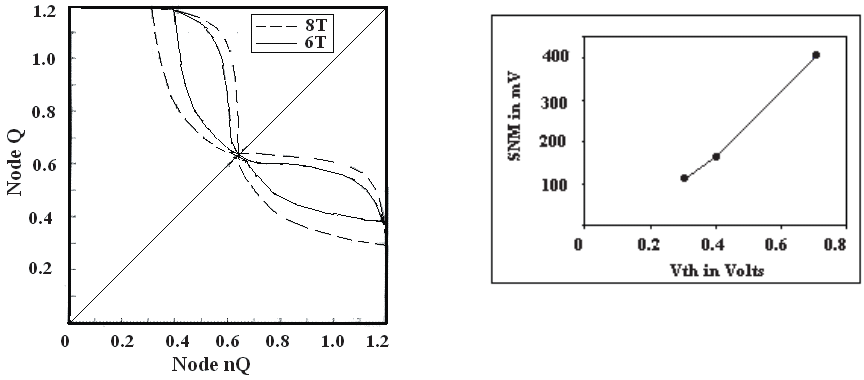
(a)

(b) (c)

Fig. 2. (a) Read delay, (b) Tail Transistor current, (c) Write/Read Time for different Vth

is degraded to 58.4% (Fig. 2 (c)) because the pre-charged bitline discharges through transistors N1/N2 and the tail transistors N5/N6 although the read power consumption drastically reduces due to the reduction in leakage current at higher threshold voltage.

There are two measurement metrics for cell stability: the read stability and the static noise margin (SNM). The SNM is defined as the maximum dc noise required to flip the cell data [11, 12]. In the proposed novel 8T SRAM cell, we have to enlarge the transistors N1, N5, N2 and N6 to compensate the stability loss due to the tail transistors. Figure 3 (a) shows the butterfly curves for proposed cell and the 6T cell. The proposed cell has the SNM of 325 mV (after choosing ratio of W/L of two tail transistors equal to 2.4) which is approximately 1.7 times higher than that of the 6T SRAM cell (195 mV). The Read SNM of the proposed cell improves by approximately 73% as the



(a) (b)

Fig. 3. (a) Graphical representation of SNM, (b) SNM for different V_{th}

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010

threshold voltage of the tail transistor increases form 0.3 V to 0.7 V as shown in Fig. 3 (b). To avoid any instability on the storage nodes Q/nQ in the unselected cells of the proposed 8T SRAM array, write operations must be performed by very short write pulse in the selected cell.

4 Conclusion

In the proposed cell, the write circuit does not discharge for any write operation and hence the write activity factor of the discharging BL is less than "1" which makes the proposed cell more power efficient during write operations compared with the conventional cell. The average column write power (ACWP) reduces in the novel 8T cell. The novel 8T cell does not compromise either stability or read access delay if width of the tail transistors is enlarged to 2.4xL. Due to an increase in the bitlines interconnect capacitance and wordline capacitance, the read power consumption increases in the novel 8T cell.

DOI: 10.1587/elex.7.1175
Received April 08, 2010
Accepted June 18, 2010
Published August 25, 2010