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An optically clocked transistor array (OCTA) for 40-Gb/s, bidirectional serial-to-parallel conversion of asynchronous burst optical packets

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Abstract: We have fabricated an optically clocked transistor array (OCTA) in an optoelectronic integrated circuit (OEIC) technology incorporating 0.18-μm gate length high-electron-mobility transistors (HEMTs). As a result of its dual serial-to-parallel (SP) and parallel-to-serial (PS) conversion (time demux/mux) capability, the OCTA realizes a single-chip, low-power interface between input/output high-speed asynchronous burst optical packets and CMOS electronics, thus enabling a compact, low-power solution for label swapping of optical packets. Single channel measurements indicate an input bandwidth greater than 65 Gb/s. An eight-channel array demonstrates SP and PS conversion at 40 Gb/s.

Keywords: optical packet switching, label swapping, OEIC

Classification: Photonics devices, circuits, and systems

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1 Introduction

The field of optical packet switching has recently experienced considerable growth, with the goal of achieving a high-performance network with the flexibility, scalability, and throughput to support the large amount of Internet Protocol (IP) traffic and demand for new services predicted for the future [1, 2]. One of the key requirements for realizing an optical packet-switched (OPS) network is implementation of the label swapping algorithm at each network node, where the label of an incoming optical packet must be recognized and erased, and a new label determined and attached to the outgoing optical packet.

In previous work, we proposed a label swapping scheme based on an optically clocked transistor array (OCTA) with the ability to perform both serial-to-parallel (SP) and parallel-to-serial (PS) conversion (time-to-space and space-to-time mapping, respectively) of asynchronous burst optical packets [3]. Realization of the OCTA in an optoelectronic integrated circuit (OEIC) technology creates with a single chip, an interface between the input/output asynchronous optical labels and CMOS circuits, which execute the signal processing tasks required for label swapping (label recognition, rewriting of label fields, generation of control signal for switching). The OCTA combined with CMOS thus enables a compact, low-power asynchronous optical label swapper with extremely high functionality. An OCTA fabricated in a 0.7-μm gate length InP high-electron-mobility transistor (HEMT) OEIC technology was integrated with CMOS electronics to form a prototype label swapper module which demonstrated successful label swapping of 10-Gb/s asynchronous burst optical labels [4].

For this work, we have fabricated an OCTA in a 0.18-μm gate length HEMT OEIC process. The improved transistor technology increases OCTA performance, with single channel measurements indicating a sampling bandwidth greater than 65 Gb/s. An eight-channel OCTA achieves SP and PS conversion at 40 Gb/s.

2 Principle of operation

Figure 1 a) shows a diagram of the label swapping scheme. A fraction of the input optical packet is split and fed into an electrical clock-pulse generator (ECG) [5], whose output drives a 1×2 optical switch (SW) with proper

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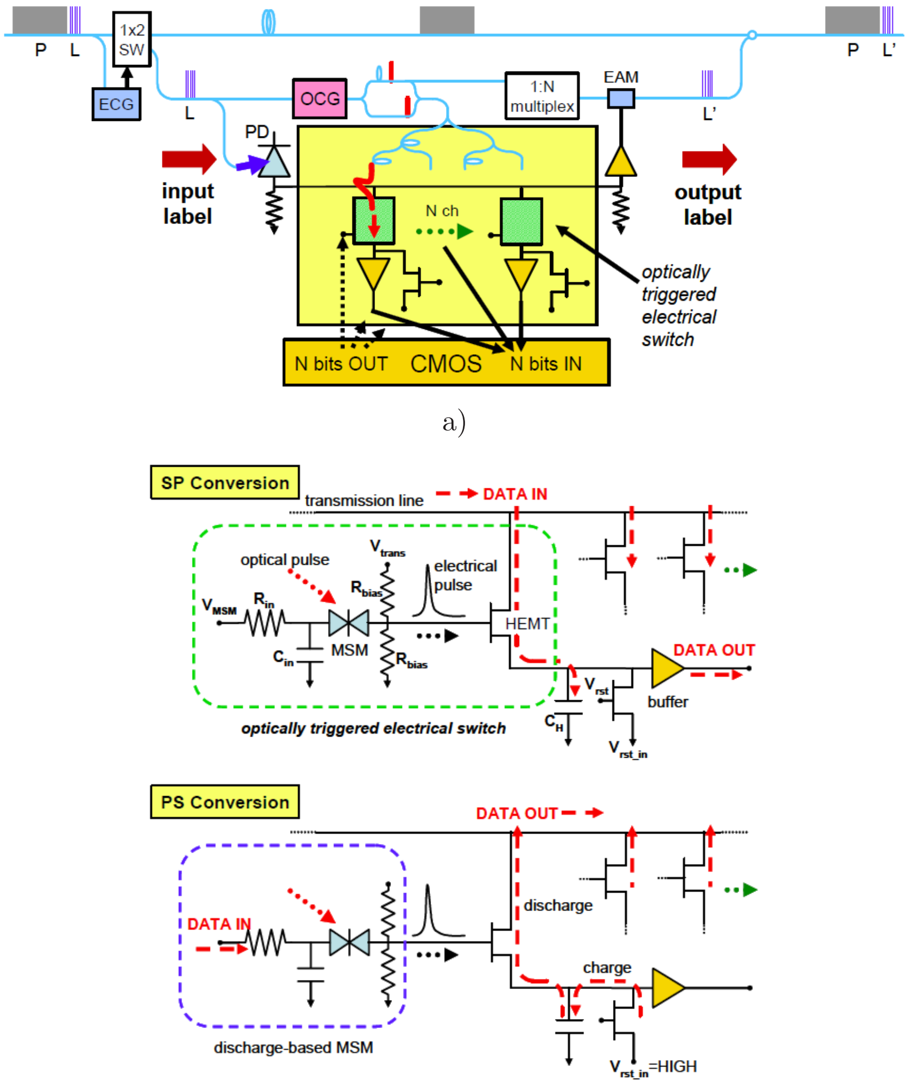

Fig. 1. a) Diagram of label swapping scheme. ECG – electrical clock-pulse generator. SW – optical switch. OCG – optical clock-pulse generator. PD – photodetector. EAM – electroabsorption modulator. b) Circuit diagrams illustrating SP (top) and PS (bottom) conversion operation.

timing to separate the packet into its label and payload. The input label is then split and fed into an optical clock-pulse generator (OCG) and photodetector (PD). The OCG generates a short optical clock-pulse (FWHM $\sim 10\,\text{ps}$) accurately synchronized with the input packet [5]. The PD output electrical signal propagates down a transmission line loaded with an array of optically triggered electrical switches. With one switch for each label bit, triggering the switches with pulses from the OCG samples the entire label in parallel (SP conversion). A high-bandwidth optically triggered electrical switch is realized by combining a discharge-based metal-semiconductor-metal (MSM) PD and a HEMT switch (Fig. 1 b), top). By setting the charge time constant of the input capacitor ($\tau_{in} = R_{in}C_{in}$) to be much longer than the

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discharge time constant ($\tau_{out} = (R_{bias}/2 + R_{MSM}) \times C_{in}$, where R_{MSM} is the MSM on-state resistance), the bias across the MSM approaches zero when triggered with an optical pulse. This eliminates the photoresponse tail due to slow holes to generate an ultrafast electrical pulse output (FWHM $\sim$ 3.3 ps [6]) which modulates the transistor switch gate. With the steady-state gate voltage set below transistor threshold through biasing resistors (R_{bias}), triggering the MSM turns the switch on for a short period of time to perform a high-bandwidth sample-and-hold of the input electrical label signal. One switch/channel samples one label bit, with the trigger appropriately timed for each channel. The held signal is then read through on-chip buffer amplifiers into CMOS electronics where the label is recognized, and a new label determined according to a forwarding table. The new label signal is entered in parallel from CMOS into the switches through the MSM bias node (V_{MSM}), a high voltage for a "1" and zero volts for a "0" (Fig. 1 b), bottom). The hold capacitor (C_H) is simultaneously charged HIGH through reset transistors. Triggering the MSMs with the same timing employed for SP conversion generates the new label as a serial voltage signal onto the transmission line (PS conversion), as only switches of the "1" bit channels turn on to discharge their held charge. The "0" bit channels produce virtually no output, a result of the symmetric device structure of the MSM PD, not possible with a p-i-n PD. An electroabsorption modulator (EAM) encodes the output label voltage signal onto an optical pulse train, created with a $1 : N$ multiplexer which splits, delays, then combines an OCG source pulse. The resulting new optical label is passively coupled to the payload (delayed in optical fiber) to output the label swapped packet.

For a desired SP and PS conversion rate, circuit parameters of the OCTA are adjusted to maximize performance, with a lower τ_{out} value for higher speeds. However, the reduction of τ_{out} (lower C_{in}, R_{bias}) also decreases the HEMT switch turn-on transient which degrades gain/sensitivity of the circuit. As a solution, minimizing the transistor parasitic gate capacitance with the adoption of shorter gate length transistors is an effective means of increasing the switch gate voltage swing and in turn, on-state current flow. For SP conversion, reduced parasitics also lead to a smaller hold capacitance to further increase sensitivity.

3 Experimental results

An OCTA was fabricated in a 0.18-μm HEMT OEIC technology, with transistor gates defined by electron beam lithography. Unity gain frequency (f_t) of the transistors was measured to be $\sim$ 140 GHz. A 0.75-μm finger width and spacing interdigitated pattern covering a $\sim 20 \times 20 \mu m^2$ area was fabricated for the MSMs.

A cross-correlation measurement was initially performed with a single channel to quantify sensitivity and bandwidth of the circuit. A short electrical pulse (FWHM $\sim$ 10.5 ps) generated from a negative output voltage unitraveling-carrier (UTC)-PD was used as the input signal. The buffer out-

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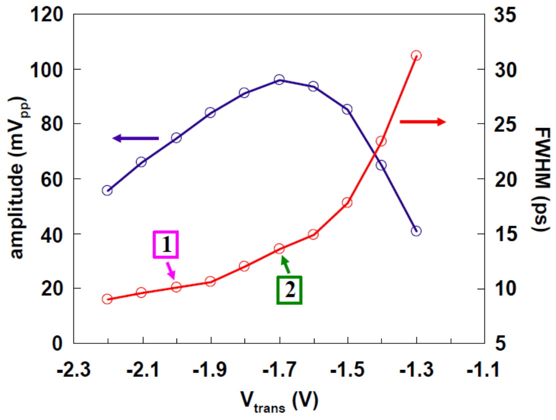
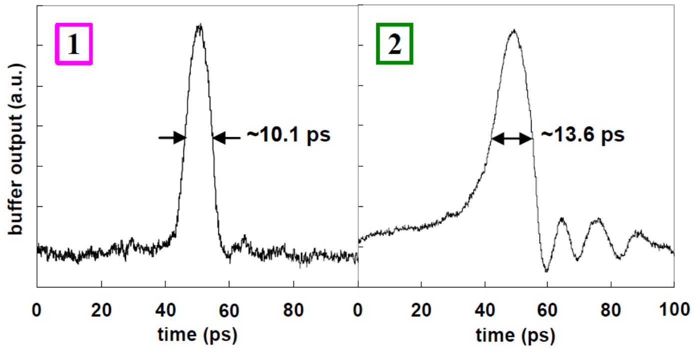


a)



b)

Fig. 2. a) Amplitude and width of cross-correlation measurement output versus V_{trans}. b) Corresponding waveforms for $V_{trans} = -2$ (left) and -1.7 (right).

put was monitored while scanning the relative phase of the MSM optical trigger pulse. For all measurements, input signal amplitude was ~ 300 mV, with a trigger pulse energy of ~ 2 pJ. Figure 2 a) shows the amplitude and width of the resulting cross-correlation output as a function of the switch transistor gate bias voltage (V_{trans}). Tuning V_{trans} leads to a corresponding DC shift of the gate voltage transient with respect to the transistor threshold voltage. Decreasing V_{trans} thus narrows the switch gating function to increase bandwidth, but simultaneously decreases the voltage jump above threshold to decrease sensitivity. This gain-bandwidth tradeoff is reflected in the results of Fig. 2 a), where output amplitude and width decrease with V_{trans}. For V_{trans} greater than -1.7 V, the amplitude decreases as the switch gating function becomes wider than the input pulse signal itself. The cross-correlation waveforms for $V_{trans} = -2$ and -1.7 are shown in Fig. 2 b), exhibiting a FWHM of 10.1 and 13.6 ps, respectively. The minimum output pulse width obtained was ~ 9 ps, shorter than the original input pulse. This result can most likely be attributed to the use of a negative voltage input signal, which sets the input signal node to be the source of the switch transistor. With the gate-source voltage being input signal dependent, the gating function varies as a function of the input signal itself. The switch is effectively off for smaller input voltages, with adjustment of V_{trans} leading to a corresponding change in

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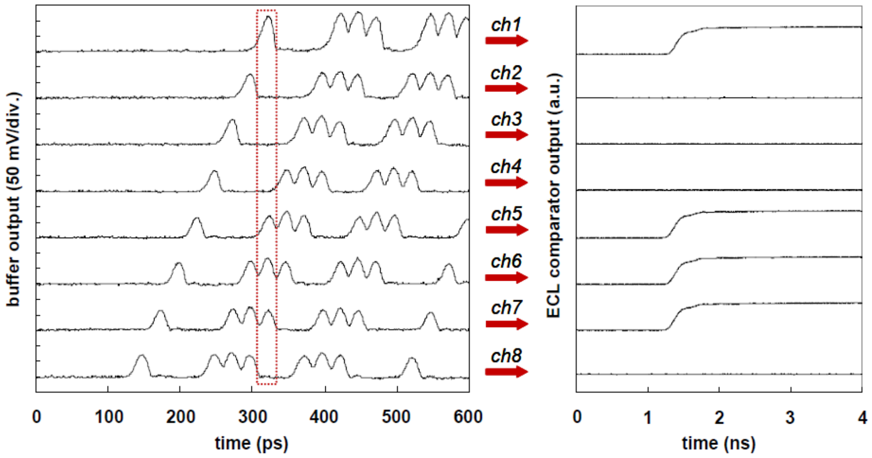

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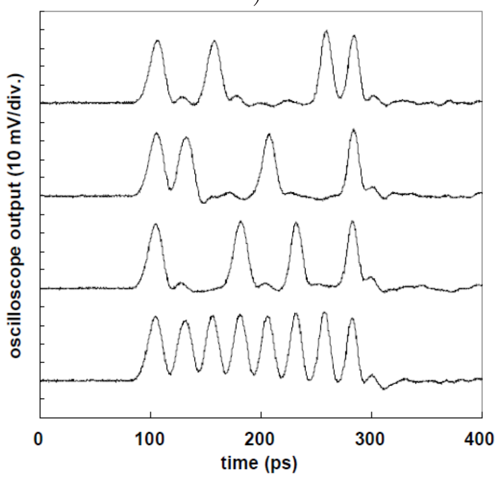

b)

Fig. 3. a) Cross-correlation measurement results with 8-channel OCTA (left). Discrimination of buffer outputs at a fixed trigger pulse phase (right). b) 40-Gb/s PS conversion output for four different 8-bit signals.

this “off” input voltage range. The results of Fig. 2 b) support this analysis, as the right figure includes the post-pulse ringing of the input signal while the left figure eliminates this structure. Functional circuit operation was also confirmed for positive voltage input signals.

Next, an eight-channel OCTA was used to sample a 40-Gb/s, 16-bit input packet/label (1000111001110001). A cross-correlation measurement was performed with each channel of the array, with results shown on the left of Fig. 3 a). Variation of the output amplitude (60–100 mV) from channel to channel is most likely due to process variations and input signal attenuation caused by the transmission line. A comparator circuit performed discrimination of the buffer outputs at a fixed trigger pulse phase (dotted line of Fig. 3 a), left). Results are shown on the right of Fig. 3 a), confirming successful SP conversion of the first eight label bits. PS conversion was demonstrated with the same device, converting four different 8-bit input par-

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allel electrical signals (10100011, 11001001, 10010101, 11111111) to 40-Gb/s output serial packets (Fig. 3 b)). In the final realization, residual features of the output waveform would be eliminated with a comparator circuit. Trigger pulses were butt-coupled to the MSMs with a linear fiber array. Electrical power consumption of the OEIC is only $\sim 8\,\mathrm{mW}$ per channel.

4 Conclusion

We have achieved 40-Gb/s SP and PS conversion with an OCTA fabricated in a 0.18-μm HEMT OEIC technology. The simple, low-power OEIC performs both demux and mux functions, enabling a compact, low-power asynchronous optical label swapper capable of high-speed, polarization insensitive operation.

The OCTA-based label swapping scheme can accommodate longer labels by increasing the number of channels per array or increasing the number of arrays and optically splitting and combining the input and output labels, respectively [3].

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