

A 0.13- μm CMOS 0.1–12 GHz active balun-LNA for multi-standard applications

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Abstract: A 0.1–12 GHz Low Noise Amplifier (LNA) with an active balun is proposed for multi-standard applications. In order to realize wideband matching and single-to-differential (S2D) conversion simultaneously, a single-end resistive negative feedback amplifier is adopted as the first stage for input impedance matching, and a novel active balun consisting of common source amplifier and source follower is designed as latter stage for S2D conversion. This LNA is fabricated in a 0.13- μm CMOS process with an active area of 0.33 mm². The measurement results show that over the full band of interest, the LNA achieves a minimum noise figure (NF) of 3.2 dB, input reflection coefficient S11 less than -9.3 dB, a power gain (S21) of 14.1 dB and -3.6 dBm IIP3 with a power consumption of 10.8 mW from 1.2-V supply.

Keywords: low noise amplifier (LNA), active balun, wideband, single-end

Classification: Integrated circuits

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1 Introduction

Recently, more and more wireless communication standards have sprung up, such as WCDMA, LTE, 802.11a/b/g/n, and UWB (ultra-wideband), etc. There has been a trend for receivers to integrate two or more standards into one chip. Some multi-standard receivers have been reported towards software-defined radio (SDR) applications [1, 2]. As a critical module, broadband low noise amplifier (LNA) is very challenged to work for multi-standard applications. Because of the single-end requirements of antenna and RF pre-filter, LNA has to face the issue of single-to-differential (S2D) conversion to work with the cascading differential building blocks in the receiver. Compared with off-chip balun and on-chip transformer, on-chip active balun has advantages of higher area efficiency, less insertion loss and being easier for monolithic integration. Traditionally, active balun, consisting of a pair of common source (CS) and common gate (CG) amplifiers, is adopted at the input of LNA to complete the S2D conversion [3]. However, the parasitic capacitor at the gate of the CS stage degrades the performance at high frequency, such as S11. In this letter, a broadband balun-LNA is proposed, as shown in Fig. 1. In order to overcome the constraints from active balun to wideband performance, a modified single-ended resistive feedback topology is designed for wideband input matching and a novel wideband active balun is proposed at latter stage for the S2D conversion, respectively. Therefore, comparing to traditional balun-LNA, a much wider bandwidth is achieved. Current reuse technique is used to achieve low power and high gain. To enhance the stability of single-end circuit, a common source amplifier is inserted as compensation stage. The measurement results show that the LNA achieves a minimum NF of 3.2 dB, S11 less than -9.3 dB, maximum gain of 14.1 dB and maximum IIP3 of -3.6 dBm at the power consumption of 10.8 mW. The measured gain and phase imbalance of the balun-LNA are within 1.1 dB and 2.6 degrees.

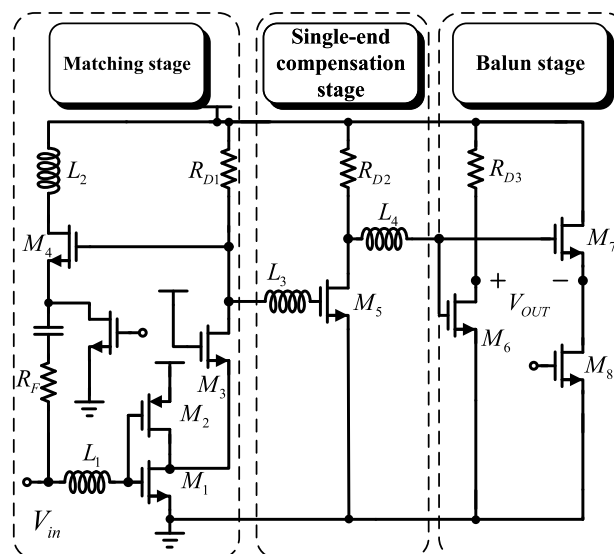


Fig. 1. The proposed broadband balun-LNA

2 Architecture and circuit design

2.1 Input matching stage

As shown in Fig. 1, the proposed input matching stage is designed based on a resistive feedback amplifier which has been widely used as wideband LNA. The schematic and the equivalent small signal model of the traditional resistive feedback amplifier are shown in Fig. 2 (a) and (b).

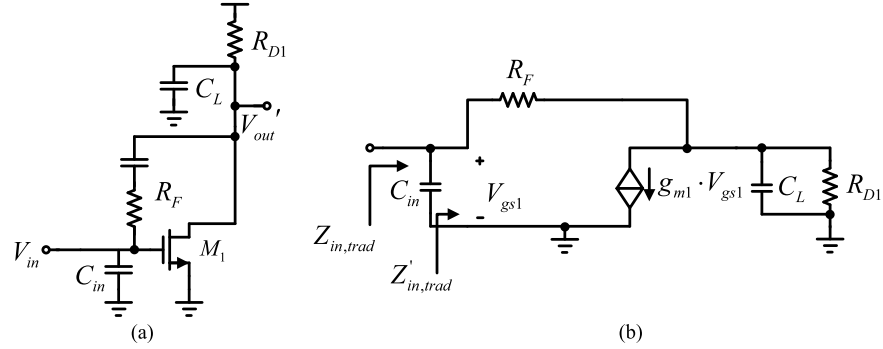


Fig. 2. (a) The schematic of traditional resistive feedback LNA. (b) The small signal equivalent model of traditional resistive feedback LNA

The well-known input impedance $Z_{in,trad}$ can be derived as

$$Z_{in,trad} = Z_{C_{in}} // Z'_{in,trad} = (R_F + Z_{Load}) / (1 + g_{m1} \cdot Z_{Load}) \approx (1 + R_F / Z_{Load}) / g_{m1} \Big|_{Z_{Load} = R_{D1} // C_L} \quad (1)$$

Where R_F and g_{m1} are the feedback resistance and the transconductance of M_1 , respectively, and Z_{Load} is the load impedance, which is equal to load resistor R_{D1} paralleled with load capacitor C_L . According to equation (1), $Z_{in,trad}$ will be affected by Z_{Load} because of the feedback. And the Z_{Load} varies with frequency, which will deteriorate S11 especially at high frequency.

To fix this problem and achieve wideband input matching, the inductor L_2 is introduced. The simplified schematic of matching stage with only L_2 considered is shown in Fig. 3 (a) and its small signal model is shown in Fig. 3 (b). And the input impedance is given by

$$Z_{in} = Z'_{in} // Z_{C_{in}} = \left[R_F + \frac{(Z_{Load} + Z_{L2} + Z_{C_{gd4}}) Z_{C_{gs4}} + (Z_{L2} + Z_{C_{gd4}} + g_{m4} \cdot Z_{C_{gs4}} \cdot Z_{L2}) Z_{Load}}{(Z_{Load} + Z_{L2} + Z_{C_{gd4}})(1 + g_{m4} \cdot Z_{C_{gs4}})} \right] \cdot \left[1 + g_{m1} \cdot Z_{Load} \left(1 - \frac{Z_{Load}}{Z_{Load} + Z_{L2} + Z_{C_{gd4}}} \right) \right]^{-1} // Z_{C_{in}}, Z_{Load} = R_{D1} // C_L \quad (2)$$

According to equation (2), through feedback path, L_2 can reduce the effect of Z_{Load} to some extent and thus improve S11. The simulation results of S11 under different L_2 are shown in Fig. 3 (c). After trial and error, the wideband

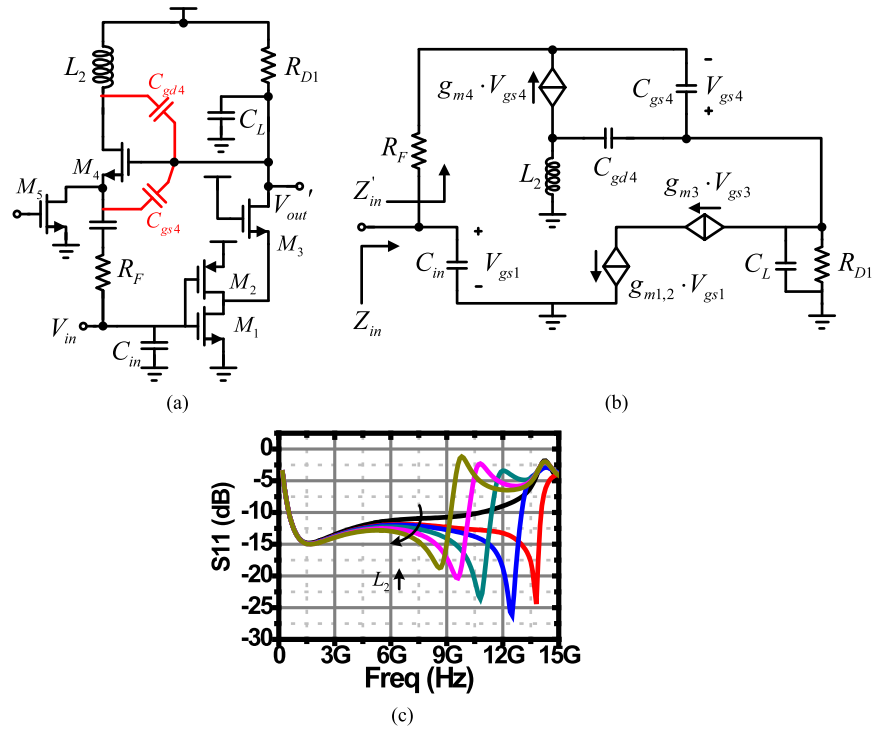


Fig. 3. (a) The schematic of the proposed matching stage. (b) The small signal equivalent model of the proposed matching stage (c) The S11 simulation results with different L_2

input matching can be realized by choosing a suitable value of L_2 . Furthermore, transistors of M_1 and M_2 are employed to fulfill the current reuse function, and the gate peaking inductor L_1 is used to expand the bandwidth, which is shown in Fig. 1.

2.2 Single-end compensation stage

The structure of differential pairs is usually used in conventional LNA design. The simplified schematic of differential pairs is shown in Fig. 4(a). The symmetrical structure of differential pairs forms a virtual ground node X (AC ground) and prevents the small signal current flowing outside the chip. Therefore, the differential topology is insensitive to the non-ideal factors, such as parasitic capacitance C_P , which is from pad and large decoupling

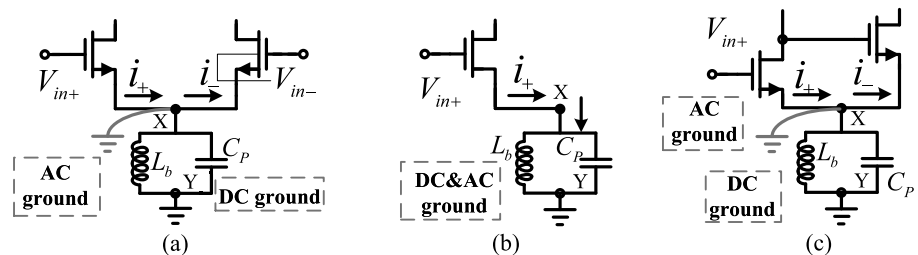


Fig. 4. AC signal analysis of (a) differential pair (b) single-end circuit (c) the proposed circuit (d) effect of compensation stage on Z_{in}

capacitance, bond wire inductor L_b , and even parasitic inductor on probe station.

In single-end circuits, however, AC and DC ground are merged at node Y. As shown in Fig. 4 (b), the AC signal current i_+ flows to Y through L_b and C_p . This LC resonant tank is located in the signal path, and because of the large parasitic capacitance from decouple capacitor, the resonant frequency will fall in the desired band, thus it will effect Z_{in} and S11 significantly. In order to resolve this problem, another common-source amplifier is introduced as a single-end compensation stage. After trial-and-error, the phases of the AC signal currents i_+ and i_- are nearly opposite and then, node X works as virtual ground for the AC signals, which is illustrated in Fig. 4 (c). Therefore, as well as differential topology, little of the small signal current flows off the chip and the core circuit is not easily affected by off-chip non-ideal factors. And in order to expand the bandwidth, L_3 and L_4 are introduced to resonate with the parasitic capacitors at the gate of M_5 - M_7 , as shown in Fig. 1.

2.3 Active balun stage

The co-design of active balun and LNA has been studied in recent years [3].

As shown in Fig. 5 (a), the CG-CS active balun is usually adopted as input stage of LNAs to fulfill input matching and S2D simultaneously in traditional balun-LNA. However, because of the existence of $C_{gs,cs}$ (the gate-source parasitic capacitor of M_{cs}), the S11 will degrade significantly at high frequency, and thus it is hard to design a broadband LNA from DC to over 10 GHz based on the CG-CS balun. In order to eliminate the conflict between broadband input matching and S2D functionality, the balun is arranged at latter stage and the input matching is realized by the input matching stage as discussed in section 2.1. However, the small input impedance of CG-CS, which is equal to $1/g_{m,CG}$ [3], leads to a load effect to pre-stage and thus, the gain of LNA is lowered. In order to overcome this issue, a novel active balun is proposed in Fig. 5 (b). A source follower, which can also provide a positive phase at the output, is exploited to replace the CG amplifier in traditional active balun. Therefore, because of the gate input of both source follower and CS amplifier, the input impedance of the modified balun increases, and

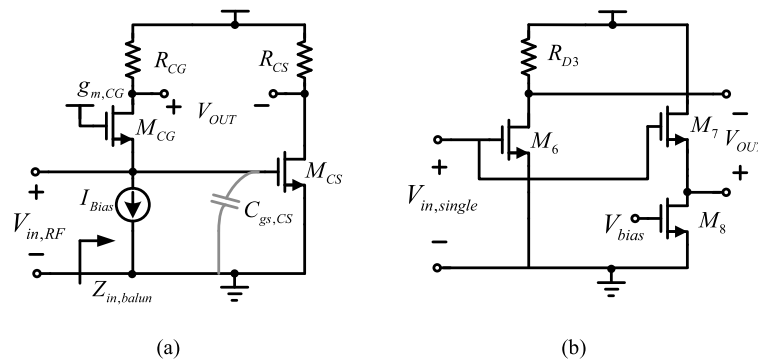


Fig. 5. (a) Traditional active balun. (b). Proposed active balun

the problem of load effect is resolved.

3 Measurement results

The proposed LNA was fabricated in a 0.13- μm , 1P8M RF CMOS process. The die photo of the LNA is shown in Fig. 6 (a). The core size of the LNA is 0.57 mm \times 0.58 mm. The source followers are employed as test buffer to realize 50- Ω output impedance matching. The DC current from the output buffer is 7.6 mA. The power consumption of the core circuit is 10.8 mW (the power consumption of output buffer has been de-embedded) from a 1.2-V supply. Fig. 6 presents the simulation and measurement results. On-wafer testing is completed on RF probe station. It is shown that the LNA achieves a minimum NF of 3.2 dB and a maximum gain of 14.1 dB. The -3 dB bandwidth is 0.1–12 GHz. The output test buffer leads to a 6-dB gain attenuation, which is de-embedded from the measurement result. The real power gain of the LNA is shown in Fig. 6 (b). As shown in Fig. 6 (c), a maximum value of measured IIP3 is -3.6 dBm. The gain and phase imbalance are within 1.1 dB and 2.6 degrees (phase difference - 180) respectively, over the 0.1–12 GHz frequency band.

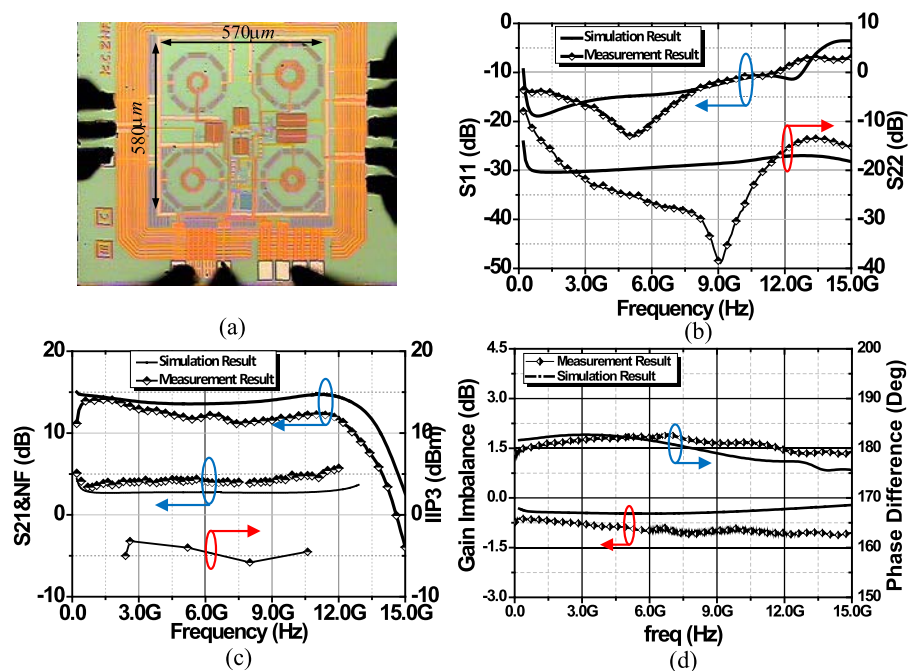


Fig. 6. (a) Die photo of the proposed broadband balun-LNA (b) S11 & S22. (c) S21, NF & IIP3. (d) Gain Imbalance and Phase Difference

The performance comparison among the proposed broadband balun-LNA and recently published LNAs is summarized in TABLE I. Considering the bandwidth and the broadband S2D function, the proposed LNA achieves an excellent comprehensive performance.

Table I. Performance Summary and Comparison

| REFERENCE | [1] | [2] | [3] | [5] | [6] | THIS WORK |
|---------------------------|-------------|----------------------|---------------------------|--------------------|--------------------|----------------------|
| Frequency(GHz) | 0.05-10 | 2-11 | 0.1-2 | 2.6-10.2 | 0.5-11 | 0.1-12 |
| Gain _{max} (dB) | 20 | 16.1 | 16.6 | 12.5 | 10.2 | 14.1 |
| S11(dB) | <-10 | <-10 | <-10 | <-9 | <-9 | <-9.3 |
| NF (dB) | 2.9-5.9 | 1.7-5.3 [†] | >3.8 | 3.0-7.0 | 3.9-4.5 | 3.2-5.5 |
| IIP3 _{max} (dBm) | -7 | -1.2 ^{††} | >0.5 | -2 | -9.1 | -3.6 |
| Architecture | Balun | Single | Balun | Single | Single | Balun |
| Power(mW)* | 22 (N/A) | 29 (20) | 3.6 (N/A) [‡] | N/A (14.4) | N/A (28.8) | 20 (10.8) |
| Area(mm ²) | 0.02 | 0.44 | 0.075 | 0.64 ^{**} | 0.54 ^{**} | 0.33 |
| CMOS | 65-nm | 130-nm | 130-nm | 90-nm | 180-nm | 130-nm |

*Power consumption with test buffer (without buffer) **Including Pads

[†] Measured up to 8GHz ^{††} Measured up to 6GHz

[‡]The power consumption of 3mW in [3] is revised to 3.6mW (3mA*1.2V)

4 Conclusions

In this letter, a 0.1–12 GHz broadband balun-LNA using a 0.13- μm CMOS process is presented. More wireless communication standards are covered, such as WCDMA, LTE, 802.11a/b/g/n and UWB. The proposed resistive feedback topology and active balun are designed for broadband input impedance matching and S2D conversion, respectively. The single-end compensation stage is designed to enhance the stability of the LNA. Current reuse technique is introduced to increase the transconductance and reduce power consumption. Compared with recently published works, the proposed LNA achieves excellent wideband performance, while achieving S2D function simultaneously.

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