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Investigation of bilayer HfN_x gate insulator utilizing ECR plasma sputtering

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Abstract: In this paper, we have investigated bilayer HfN_x gate insulator utilizing ECR plasma sputtering especially for the electrical properties with metallic-phase $HfN_{0.5}$ gate electrode which was formed by *in-situ* process. After PMA of 500°C/10 min in N_2/4.9%H_2 ambient, the bilayer of $HfN_{1.3}$ (1.7 nm)/$HfN_{1.1}$ (0.9 nm) gate insulator formed on Si(100) showed the EOT of 0.61 nm, leakage current density (@V_{FB} −1 V) of 5.5×10^{-3} A/cm^2 and density of interface states (D_{it}) of 5.5×10^{11} cm^{-2} eV^{-1}. The n-MISFET with bilayer HfN_x gate insulator exhibited saturation mobility (μ_{sat}) of 47 cm^2/(V s), which higher than the device with directly deposited $HfN_{1.3}$ gate insulator. HfN_x interfacial layer (IL) with low nitrogen concentration was found to significantly improve the interface properties of HfN_x gate stacks.

Keywords: bilayer, ECR plasma sputtering, hafnium nitride, nitrogen concentration, high-κ gate insulator, interfacial layer

Classification: Electronic materials, semiconductor materials

References

[1] J. Robertson and R. M. Wallace: Mater. Sci. Eng. Rep. **88** (2015) 1. DOI: 10.1016/j.mser.2014.11.001

[2] Q. Zeng, A. R. Oganov, A. O. Lyakhov, C. Xie, X. Zhang, J. Zhang, Q. Zhu, B. Wei and L. Grigorenko: Acta Crystallogr. C **70** (2014) 76. DOI:10.1107/S2053229613027861

[3] S. Ohmi, S. Kudoh and N. Atthi: IEEE Trans. Semicond. Manuf. **28** (2015) 266. DOI:10.1109/TSM.2015.2431375

[4] S. Ohmi: IEICE Electron. Express **11** (2014) 20142006. DOI:10.1587/elex.11.20142006

[5] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. V. Benthem, S. J. Pennycook, P. M. Lenahan and J. T. Ryan: J. Appl. Phys. **100** (2006) 094108. DOI:10.1063/1.2362905

[6] H. S. Han and S. Ohmi: IEICE Electron. Express **9** (2012) 1329. DOI:10.1587/elex.9.1329

[7] H. S. Han, D. H. Han and S. Ohmi: Electron. Lett. **49** (2013) 500. DOI: 10.1049/el.2013.0319

[8] N. Atthi, D. H. Han and S. Ohmi: MRS Proc. **1588** (2014) 1. DOI:10.1557/opl.2014.223

[9] T. Sano and S. Ohmi: Jpn. J. Appl. Phys. **50** (2011) 04DA09. DOI:10.7567/

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JJAP.50.04DA09
[10] N. Atthi and S. Ohmi: The 62nd JSAP Spring Meeting (2015) 13a-A24-12. 12.
[11] N. Atthi and S. Ohmi: IEICE Technical Report (SDM) **115** [280] (2015) 57.
[12] Y.-L. Li, K. C. Liao, C. C. Li, L. T. Chen, T.-H. Su, Y.-W. Chang, T.-C. Chen, C.-C. Tsai, C.-H. Kao, H.-T. Feng and Y. J. Lee: Microelectron. Eng. **147** (2015) 67. DOI:10.1016/j.mee.2015.04.026
[13] J. H. Jang, S. H. Hong, T. J. Park, J. H. Heo, S. R. Yang, M. Y. Kim and C. S. Hwang: ECS Trans. **1** (2006) 393.
[14] S. Ohmi and Y. Nakano: 2007 IEEE Int. Symp. on Semicond. Manuf., Conf. Proc. (2007) 514. DOI:10.1109/ISSM.2007.4446875
[15] S. Saito, K. Torii, M. Hiratani and T. Onai: IEEE Electron. Dev. Lett. **23** (2002) 348. DOI:10.1109/LED.2002.1004231
[16] Z. Gu, C. Hu, H. Huang, S. Zhang, X. Fan, X. Wang and W. Zheng: Acta Mater. **90** (2015) 59. DOI:10.1016/j.actamat.2015.02.026

1 Introduction

Metal gate/high-κ gate dielectric (MG/HK) stacks are promising candidates to replace the conventional poly-Si/SiON gate stack structures to overcome the limitations of scaling in complementary metal-oxide-semiconductor field-effect transistors (CMOS) technology [1]. Among the high-κ materials, Hf-based high-κ gate insulator such as HfO_2, HfON and HfSiON has emerged as one of the promising candidates [2, 3, 4]. However, scaling down an equivalent oxide thickness (EOT) beyond 0.5 nm is a great challenge for CMOS technology. This is because the interfacial layer (IL) with relatively low-dielectric constant between high-κ/Si interfaces is formed easily when the oxide-based high-κ gate insulator is used [5]. Therefore, nitride dielectrics are the candidate materials as a gate dielectric to overcome the problems of oxide-based high-κ materials to suppress IL formation [6, 7]. We have reported that 0.5 nm EOTs were obtained by using hafnium nitride (HfN) gate insulator (I) formed by electron-cyclotron-resonance (ECR) plasma sputtering with *ex-situ* Al gate electrode (G) [8]. However, the contamination and the oxidation during *ex-situ* Al deposition severely degraded the electrical properties such as mobility. Therefore, *in-situ* deposition of thermally stable gate electrode is used instead of Al for gate-first process [9].

We have reported that *in-situ* deposition of HfN_x ($x < 1.0$) gate electrode improves the electrical properties of HfN_x gate stacks [10]. The high nitrogen (N) concentration, such as Hf_3N_4 or higher, would be required for EOT scaling below 0.5 nm since the increase of the N concentration would lead to higher dielectric constant [11]. However, direct contact of HfN_x gate insulator with high N concentration ($x \geq 1.2$) on Si substrate severely degrades the electrical properties of HfN_x gate stacks due to the degradation of interface properties at HfN_x/Si interfaces [10, 11]. Various oxide-based IL such as chemical oxide and thermally grown SiO_2 have been reported to improve the quality of high-κ/Si interface [12]. However, bilayer gate insulator with oxide-based IL limits the scaling down of an EOT. Therefore, nitride-based IL insulator with low nitrogen concentration is required to prevent the IL formation [13].

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In this paper, bilayer of $HfN_{1.3}/HfN_x$ (x = 1.0–1.2) gate insulator utilizing ECR plasma sputtering on the electrical properties of HfN_x gate stack structures is proposed. The effects of nitrogen concentration in high-κ HfN_x IL with low nitrogen concentration on the electrical properties of HfN_x gate stack structures were studied. The influence of post-metallization annealing (PMA) in $N_2/4.9\%H_2$ forming-gas (FG) ambient was investigated. Furthermore, characteristics of an n-MISFET with bilayer HfN_x gate insulator were demonstrated.

2 Experimental procedure

The metal-insulator-semiconductor (MIS) diodes and n-MISFET device with $HfN_{0.5}$ (10 nm)/$HfN_{1.3}$ (1.7 nm)/HfN_x IL (0.9 nm)/p-Si(100) gate stack structures were *in-situ* fabricated in accordance with schematic structures shown in Fig. 1(a) and Fig. 1(b), respectively. To fabricate the MIS-diode with bilayer HfN_x gate insulator, p-Si(100) substrates (N_A: 1×10^{15} cm^{-3}) were cleaned by sulfuric peroxide mixture (SPM) and diluted hydrofluoric acid (DHF). Then, 0.9 nm-thick HfN_x IL with different Ar/N_2 gas flow ratio of 20/8 sccm (N_2: 28.8%, 0.20 Pa), 16/12 sccm (N_2: 44%, 0.20 Pa) and 12/16 sccm (N_2: 57%, 0.20 Pa) were deposited on p-Si(100) by using ECR plasma sputtering (JSW AFTY: AFTEX-3400) [9]. The μ-wave/RF power was 500/400 W. The 1.7 nm-thick $HfN_{1.3}$ (I) layer was *in-situ* deposited on IL utilizing ECR plasma sputtering with Ar/N_2 gas flow ratio of 8/20 sccm (N_2: 71%, 0.20 Pa). The μ-wave/RF power was 500/500 W.

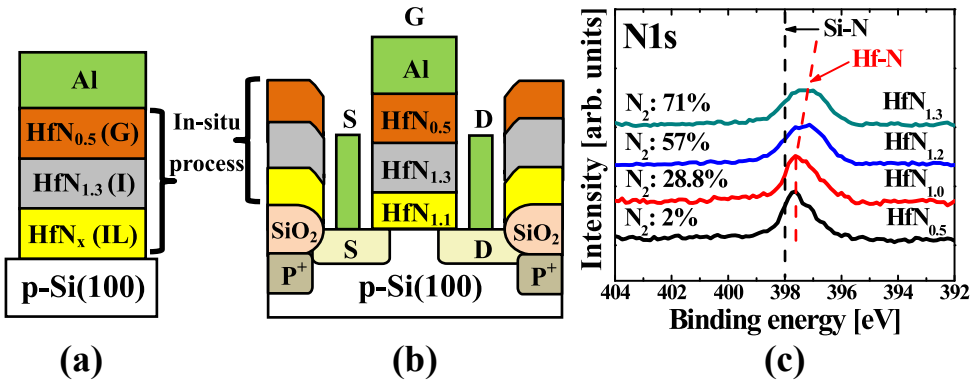

Fig. 1. Schematic cross-sectional structures and composition of HfN_x gate stacks with bilayer HfN_x gate insulator. (a) MIS-diode, (b) n-MISFET and (c) $N_2/(Ar+N_2)$ gas flow ratio dependence of N1s spectra on HfN_x films.

Then, 10 nm-thick metallic-phase $HfN_{0.5}$ gate electrode (ϕ_{HfN}: 4.8 eV) was *in-situ* deposited on $HfN_{1.3}$ (I) using Ar/N_2 gas flow ratio of 10/0.2 sccm (N_2: 2%, 0.09 Pa). The μ-wave/RF power was 500/400 W. The PMA was carried out at 500°C/10 min in $N_2/4.9\%H_2$ FG ambient (1 SLM) by silicon-wafer-covering (SWC) process utilizing rapid thermal annealing (RTA) system [14].

The 40 nm-thick Al contact layer was *ex-situ* evaporated on HfN_x gate stacks. Al contact layer was patterned by H_3PO_4:HNO_3 mixed solution (50:3) for 60 s. Then, HfN_x gate stacks were patterned by DHF (1%) for 90 s. The size of gate electrode was 90×90 μm^2. The backside Al contact was deposited by evaporation.

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Direct contact of HfN_x gate insulator with high N concentration such as 2.5 nm-thick $HfN_{1.3}$ (I) layer on p-Si(100) was fabricated for comparison by using ECR plasma sputtering with Ar/N_2 gas flow ratio of 8/20 sccm (N_2: 71%, 0.20 Pa). The μ-wave/RF power was 500/500 W. The Al contact/$HfN_{0.5}$ (G) stack layers were deposited on $HfN_{1.3}$ (I) layer by using the same process condition as bilayer HfN_x gate insulator MIS-diode.

The n-MISFET was fabricated using conventional gate-last process [7]. After local oxidation of Si (LOCOS) isolation and channel stop formation, source/drain (S/D) was formed by ion implantation of PH_3 at 20 keV with a dose of 5×10^{15} cm^{-2}. The activation annealing was carried out in N_2 ambient at 1000°C/2 min. The HfN_x gate stacks with $HfN_{1.1}$ IL was deposited by using the same process condition as MIS-diode. After contact holes formation, Al pads were patterned for source, drain and gate electrodes. The gate width (W) was 90 μm and gate length (L) was 10 μm.

The capacitance-voltage (C-V) and current-voltage (J-V) characteristics of bilayer HfN_x gate insulator MIS-diode were measured utilizing Agilent 4284A and Agilent 4156C, respectively. A dual-frequency method was used to evaluate the C-V characteristics. The EOTs were extracted from C-V with quantum mechanical correction [15], and the density of interface states (D_{it}) was evaluated by Terman method. The film thickness was measured by ellipsometer, and the x-ray photoelectron spectroscopy (XPS) was carried out to evaluate the film composition. The I_D-V_D and I_D-V_G of n-MISFETs were also characterized.

3 Results and discussion

Fig. 1(c) shows the $N_2/(Ar+N_2)$ gas flow ratio dependence of N1s spectra on HfN_x films. The nitrogen concentration in HfN_x film was determined by N/Hf fraction, which calculated by the products of peak area of Hf4f and N1s spectra and atomic sensitivity factor (ASF) [16]. The nitrogen concentrations were evaluated as $HfN_{0.5}$, $HfN_{1.0}$, $HfN_{1.2}$ and $HfN_{1.3}$ when the N_2 gas flow ratio was changed as 2%, 28.8%, 57% and 71%, respectively. The peak of Hf4f spectra for insulating-phase $HfN_{1.3}$ film was chemically shifted to higher binding energy than metallic-phase $HfN_{0.5}$ film, which attributed to the higher concentration of nitrogen in $HfN_{1.3}$ film [16].

Fig. 2(a) shows the effects of nitrogen concentration of HfN_x IL ($x = 1.0$–1.2) on the C-V characteristics (100 kHz) of as-deposited HfN_x gate stack structures. The $HfN_{1.1}$ IL (N_2: 44%) shows the smallest EOT, although as-deposited films show large frequency dispersion in C-V characteristics (not shown). When the N_2 gas flow ratio increased, the flat-band voltage (V_{FB}) shifted toward positive voltage direction due to decrease of positive fixed charges.

Moreover, the HfN_x gate stacks without IL has higher leakage current density such as $J_g(@V_{FB} - 1\,V)$ of 5.2 A/cm^2 compared to the HfN_x gate stacks with $HfN_{1.1}$ IL (3.8 A/cm^2). Whether the HfN_x film with higher nitrogen concentration is required for EOT scaling below 0.5 nm due to its higher dielectric constant, excess nitrogen concentration in HfN_x IL such as $HfN_{1.2}$ IL (N_2: 57%) generates high D_{it}, which degrades the interface qualities and leads to high leakage paths.

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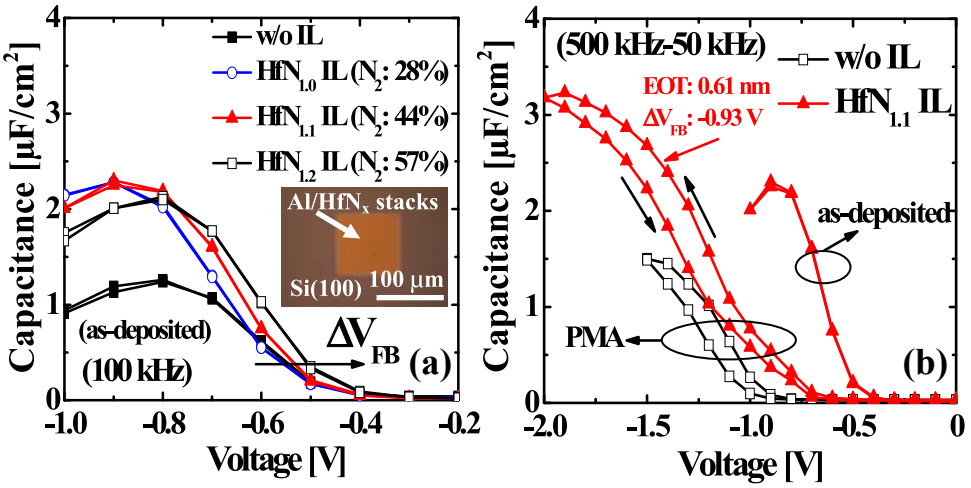

Fig. 2. C-V characteristics of bilayer HfN_x gate insulator MIS-diode. (a) Effects of nitrogen concentration of as-deposited HfN_x IL (100 kHz), and (b) effects of PMA process of different IL materials in $N_2/4.9\%H_2$ FG ambient at 500°C/10 min (500 kHz–50 kHz).

Therefore, HfN_x IL with N_2 gas flow ratio of 44%, which corresponds to $HfN_{1.1}$ IL, is suitable to improve the interface qualities for bilayer HfN_x gate insulator.

Fig. 2(b) shows that by using PMA in $N_2/4.9\%H_2$ FG ambient with SWC process at 500°C/10 min, the frequency dispersion in C-V characteristics and leakage current density of bilayer HfN_x gate insulator MIS-diode was well suppressed compared to as-deposited HfN_x gate stacks (not shown). However, large hysteresis was observed in C-V characteristics so that the PMA process condition should be further optimized.

The dual-frequency method was used to compensate the frequency dispersion and calculate the exact value of EOT. By using PMA in $N_2/4.9\%H_2$ FG ambient at 500°C/10 min, the EOT of 0.61 nm with ΔV_{FB} of −0.93 V and $J_g(@V_{FB} - 1\,V)$ of 5.5×10^{-3} A/cm^2 were obtained for HfN_x gate stacks with $HfN_{1.1}$ IL. The D_{it} of annealed HfN_x gate stacks with $HfN_{1.1}$ IL is able to be reduced to 5.5×10^{11} cm^{-2} eV^{-1}.

Fig. 3 shows the I_D-V_D and I_D-V_G characteristics of n-MISFETs device (L/W: 10/90 μm) with bilayer HfN_x gate insulator. The saturation mobility (μ_{sat}) extracted from the results was 47 cm^2/(V s), which is higher than our previous reported data [7]. At V_D of 0.05 V, the n-MISFET exhibits excellent performance in terms of near ideal subthreshold swing (SS) of 77 mV/dec. When the V_D increased from 0.05 to 1.0 V, the V_{th} was slightly shifted from −0.04 to −0.03 V. Furthermore, the SS degraded from 77 to 90 mV/dec, and off leakage current increased two orders of magnitude. This is because the effects of drain-induced barrier lowering (DIBL). Therefore, the superior electrical properties, especially the saturation mobility, are probably attributed to the lower nitrogen concentration of HfN_x IL improved the interface properties of MISFETs.

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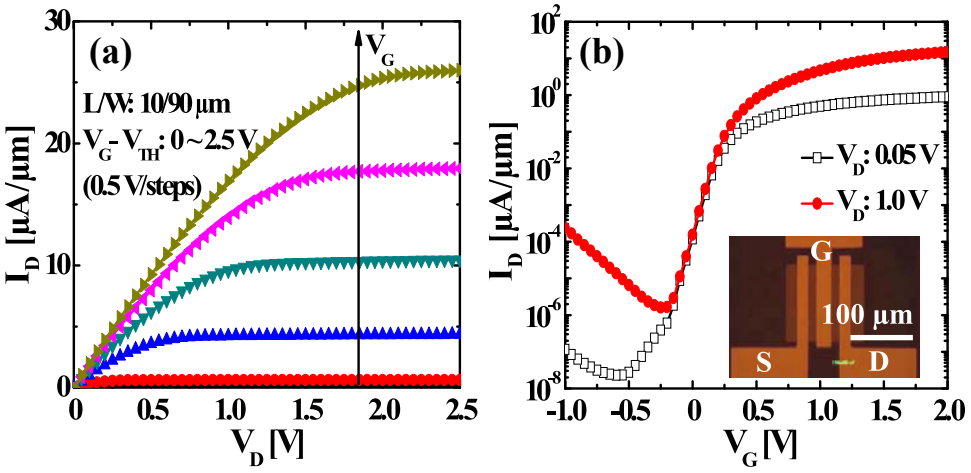

Fig. 3. Electrical characteristics of n-MISFET (L/W: 10/90 μm) using bilayer HfN_x gate insulator with $HfN_{1.1}$ IL fabricated by conventional gate-last process after PMA in N_2/4.9%H_2 FG ambient at 500°C/10 min. (a) I_D-V_D and (b) I_D-V_G.

4 Conclusions

We investigated the bilayer HfN_x gate insulator formation utilizing ECR plasma sputtering for the first time. The EOT of 0.61 nm with low J_g was achieved by using $HfN_{1.1}$ IL. The n-MISFET device exhibits μ_{sat} of 47 $cm^2/(V\,s)$. It was confirmed that bilayer HfN_x gate insulator with low nitrogen concentration of $HfN_{1.1}$ IL shows significantly improved the interface qualities, which leads to the superior electrical properties of HfN_x gate stacks.

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