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Green phase difference coding with low switching activity for Network-on-Chip

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Abstract: A low-power bus coding called Green Phase Difference Coding (GPD) is proposed to reduce the power consumption of long interconnects between multi-cores. In GPD, the Green-Modified coding (GM) is a novel low switching activity coding on the basis of Self-Corrected Green Coding (SGC). The mapping of GM coding between original set and converted set is modified to reduce bit transition. And the phase difference technology that uses the phase difference between the clock and data is introduced to replace decision bit. Based on SMIC 130 nm CMOS technology, the simulation results show that the GPD coding scheme achieves 37.51% and 4.13%~8.29% energy reduction compared with the parallel bus by applying random data source and SPEC95/2000 CINT reference source, respectively.

Keywords: low-power, bus coding, low switching activity, phase difference

Classification: Integrated circuits

References

[1] M. B. Taylor, J. Kim, J. Miller, D. Wentzlaff, F. Ghodrat, B. Greenwald, H. Hoffman, P. Johnson, J.-W. Lee, W. Lee, A. Ma, A. Saraf, M. Seneski, N. Shnidman, V. Strumpen, M. Frank, S. Amarasinghe and A. Agarwal: IEEE Micro **22** [2] (2002) 25. DOI:10.1109/MM.2002.997877

[2] P. Gratz, C. Kim, K. Sankaralingam, H. Hanson, P. Shivakumar, S. W. Keckler and D. Burger: IEEE Micro **27** [5] (2007) 41. DOI:10.1109/MM.2007.4378782

[3] K. Lee, S.-J. Lee, S.-E. Kim, H.-M. Choi, D. Kim, S. Kim, M.-W. Lee and H.-J. Yoo: ISSCC Dig. Tech. Papers (2004) 152. DOI:10.1109/ISSCC.2004.1332639

[4] Y. Shin, S. I. Chae and K. Choi: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **9** (2001) 377. DOI:10.1109/92.924059

[5] R. B. Lin and C. M. Tsai: VLSI Dig. Tech. Papers (2002) 121. DOI:10.1109/ASPDAC.2002.994897

[6] M. Shafaei, A. Patooghy and S. G. Miremadi: DSD Dig. Tech. Papers (2011) 55. DOI:10.1109/DSD.2011.12

[7] P. T. Huang, W. L. Fang, Y. L. Wang and W. Hwang: NoCS Dig. Tech. Papers (2008) 77. DOI:10.1109/NOCS.2008.4492727

[8] C. T. Chiu, W. C. Huang, C. H. Lin, W. C. Lai and Y. F. Tsao: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **21** (2013) 1797. DOI:10.1109/TVLSI.2012.2219888

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Copyedited July 25, 2015

[9] Z. Zhang and Y. Chang: Electronics&Packaging **7** [10] (2007) 33.
[10] S. R. Sridhara and N. R. Shanbhag: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **13** (2005) 655. DOI:10.1109/TVLSI.2005.848816
[11] J. Sun and A. Jiang: ICCRD Dig. Tech. Papers (2011) 452. DOI:10.1109/ICCRD.2011.5764172
[12] Y. Liu, S. Ma, Y. Yang and Z. Zhu: IEICE Electron. Express **11** (2014) 20140038. DOI:10.1587/elex.11.20140038

1 Introduction

With the continuous development of integrated circuit, the delay and power consumption of interconnects are one of the main bottlenecks for network-on-chip (NoC). In recent years, the power consumption in interconnects between processors has ascended to 31% of the total system power consumption [1, 2, 3]. Reducing the power consumption in interconnects becomes a hot topic. Many low-power coding methods have been proposed in the literature including the Partial Bus-Invert Coding [4], Weight-Based Bus-Invert Coding [5], Numeral-Based Crosstalk Avoidance Coding [6], Self-Corrected Green coding [7], and etc. Among those coding methods, Self-Corrected Green coding (SGC) [7] can realizes a higher energy efficiency among these approaches. And based on UMC 90 nm COMS technology, the simulation results show that SGC coding can achieve 34.4% energy reduction with small codec overhead [7]. However, an extra indication bit is added in every data word to represent inversion occurrence and the indication bit increases the transmission overhead and the bit transitions.

In this work, a low-power bus coding called Green Phase difference coding (GPD) is proposed to reduce the power consumption by reducing the switching activity. GPD coding has the lower switching activity than SGC coding. Moreover, GPD coding scheme that uses the phase difference between the clock and data in the transmitted serial data can tackle the problem of the extra indication bit [8]. The simulation results show that the transition and energy consumption is reduced by 21.6% and 37.51%, respectively, compared with those of the SGC.

The remainder of this paper is organized as follows. The second section presents the GPD coding scheme and the design of encoder and decoder. The third section provides simulation results of the coding system. Finally, the paper is concluded in Section 4.

2 Green Phase difference coding (GPD)

The overall architecture of the GPD consisting of an encoder and a decoder in Network-on-chip is shown in Fig. 1. As depicted in the figure, the 32-bit data is firstly encoded by the Green-modified encoder and then transformed into 8-bit data via the serializer. The decision bit is used to control the phase encoder block to embed the inversion information in the phase difference between the clock and the encoded data. In the GPD decoder part, the 8-bit data is transformed to 32-bit data by the deserializer. And then the data is decoded by the phase detector and the decoder.

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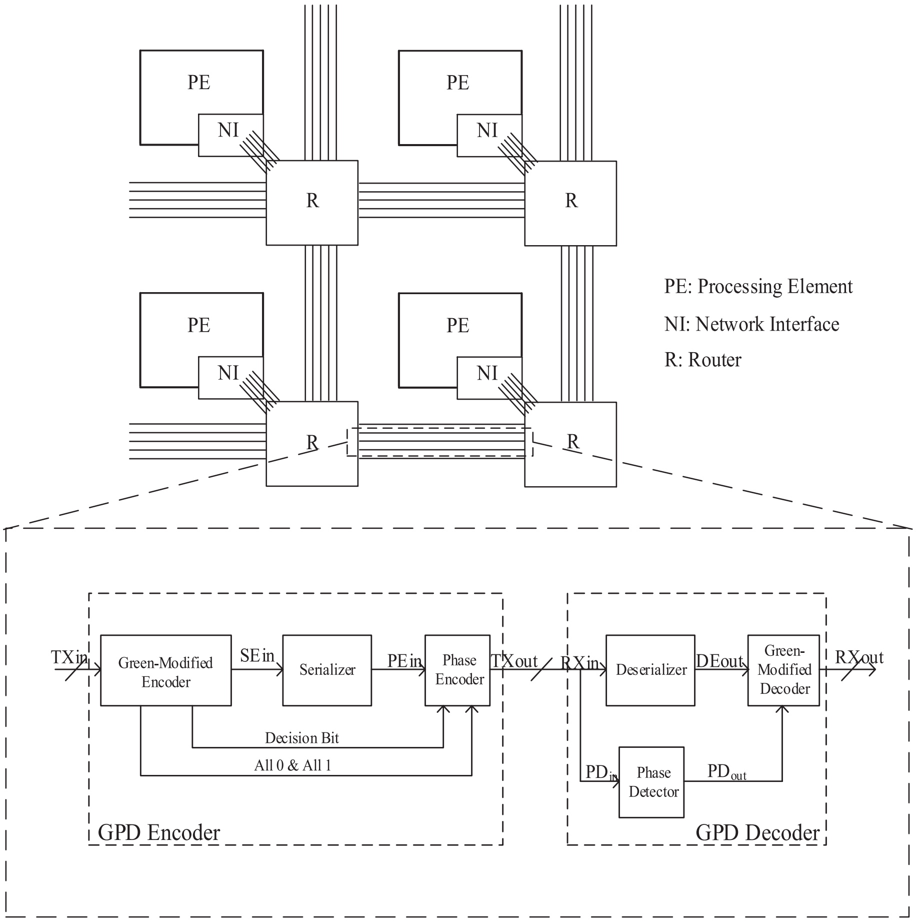

Fig. 1. Overall architecture of the GPD scheme in Network-on-chip.

2.1 Green-Modified coding

In this work, GM (Green-Modified) coding is proposed based on SGC coding [7]. The mechanism of GM coding is shown in Fig. 2. According to the correspondences, the data-word can be grouped into two sets, the original set and converted set. When the transmitted data is in the converted set, GM coding will convert the data to the original set by one-on-one mapping. Meanwhile, the decision bit will be set as "1". When the transmitted data is in the original set, the data is not modified and the decision bit will be set as "0". The ALL0&ALL1 is the decision bit to indicate whether the dataword is "0101" or "1010". The circuit implementation of Green-Modified encoder is shown in Fig. 3.

2.2 Phase encoder

The phase encoder is used to generate phase difference between the encoded data and the clock at each data-word. The circuit implementation of phase encoder is shown in Fig. 4, including a D flip-flop, an inverter, and three multiplexers.

Figs. 5(a) and 5(b) show the example of waveforms of a normal data word "0111" and a special data word "0010". Same $TX_{out}(PE_{out})$ "0111" in Fig. 4(a) and 5(b) is obtained from TX_{in} "0111" and "0010" without and with inversion. A half-clock cycle difference between PE_{out} and clk is observed in Fig. 5(b), indicating that PE_{in} has been encoded. The PE_{out} and clk are aligned in Fig. 5(a), indicating that PE_{in} has not been changed.

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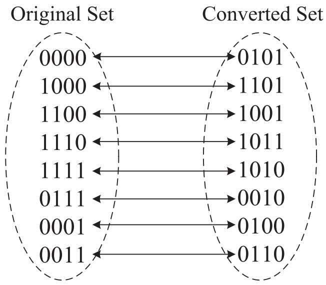
Dataword x3~x0	Codeword y3~y0	Decision Bit	ALL0 &ALL1
0000	0000	0	0
0001	0001	0	0
0010	0111	1	0
0011	0011	0	0
0100	0001	1	0
0101	0000	1	1
0110	0011	1	0
0111	0111	0	0
1000	1000	0	0
1001	1100	1	0
1010	1111	1	1
1011	1110	1	0
1100	1100	0	0
1101	1000	1	0
1110	1110	0	0
1111	1111	0	0



decision_bit
$=\overline{x3}x2\overline{x1}+x3\overline{x1}x0$
$+x3\overline{x2}x0+\overline{x3}x1\overline{x0}$
if(decision_bit==1)
then
$y0=\overline{x0},y2=\overline{x2}$
else
y0=x0,y2=x2
all 0&all 1$=\overline{x3}x2\overline{x1}x0+x3\overline{x2}x1\overline{x0}$

Fig. 2. Codeword, signal mapping and Boolean expression for GM coding scheme

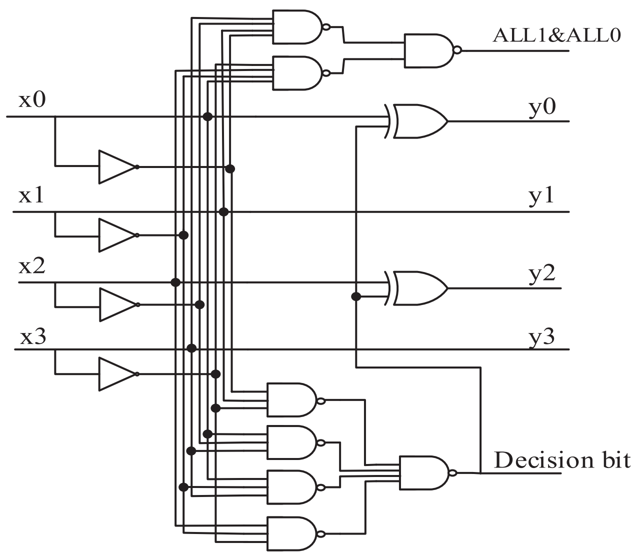


Fig. 3. Architecture of Green-Modified encoder

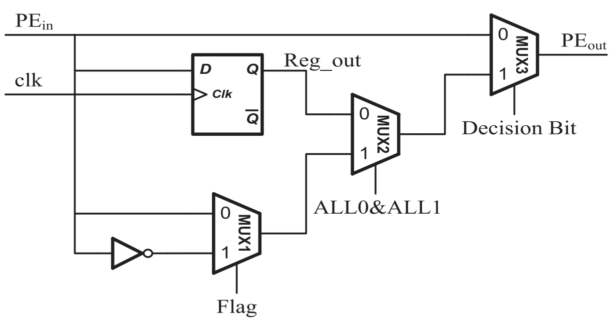


Fig. 4. Architecture of the phase encoder

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Fig. 5(c) and (d) shows the waveforms of special data words ("0101" and "1010"). When the *Flag* is "1", the codeword "0000" and "1111" change to "1000" and "0111". The first bit of PE_{out} in the "1000" and "0111" is aligned with *clk* and the duration of the bit is only half of the *clk* cycle. *Flag* is obtained according to Eq. (1) as follow:

$$Flag = \overline{clk} \cdot \overline{clk/2} \cdot clk/4 \tag{1}$$

In the equation, $clk/2$ is defined as a half of the *clk* and $clk/4$ is defined as the quarter of *clk*.

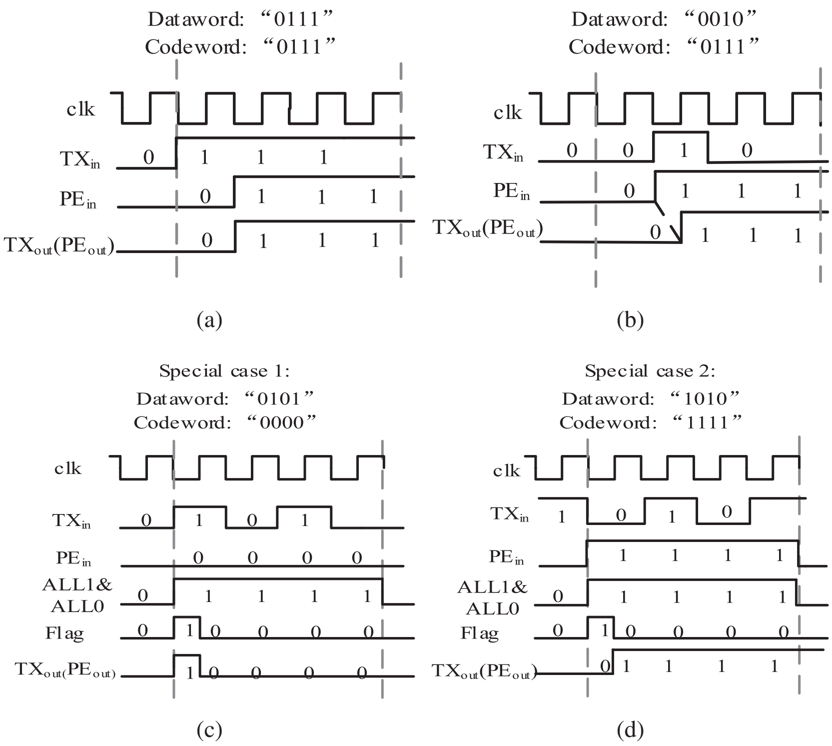

Fig. 5. (a) Waveform for normal data words ("0111") (b) Waveform for normal data words ("0010") (c) Waveform for special data words ("0101") (d) Waveform for special data words ("1010")

2.3 Phase detector

A phase detector is employed to check the phase difference between the encoded data and the clock at each data word. The scheme of the phase detector is depicted in Fig. 6(a). Fig. 6(b) shows the waveform of the phase detector in the normal case ("1000"). The reg1 differs from reg2 when there is a phase difference in PD_{in}. In this case, *xor_out* is "1" in T2, T3 or T4 at least. The *xor_out* is stored in *reg4* and *reg5*, so that *reg6* which is equal to *xor_out|reg4|reg5* can indicate whether there is a phase difference in the PD_{in}.

However, Fig. 6(c) shows that *reg6* is "0" in T1~T4 which means *reg6* fails to detect the phase difference in the special case ("0001"). This is due to the fact that there is no transition in the first three bits. In this case, *reg6* cannot indicate whether there is phase difference in PD_{in}. In order to detect the phase difference, second part of phase detector is added. Fig. 6(d) shows the waveform of the second part of

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phase detector in the special case (“0001”). In this case, *reg4* becomes “1” in T6 and *reg7* becomes “1” in T7. It shows that *reg7* can detect the phase difference in the special case. So PD_{out} which is equal to $reg6|reg7$ can indicate whether there is a phase difference. $clk/4$ is used to synchronize the outputs in this circuit.

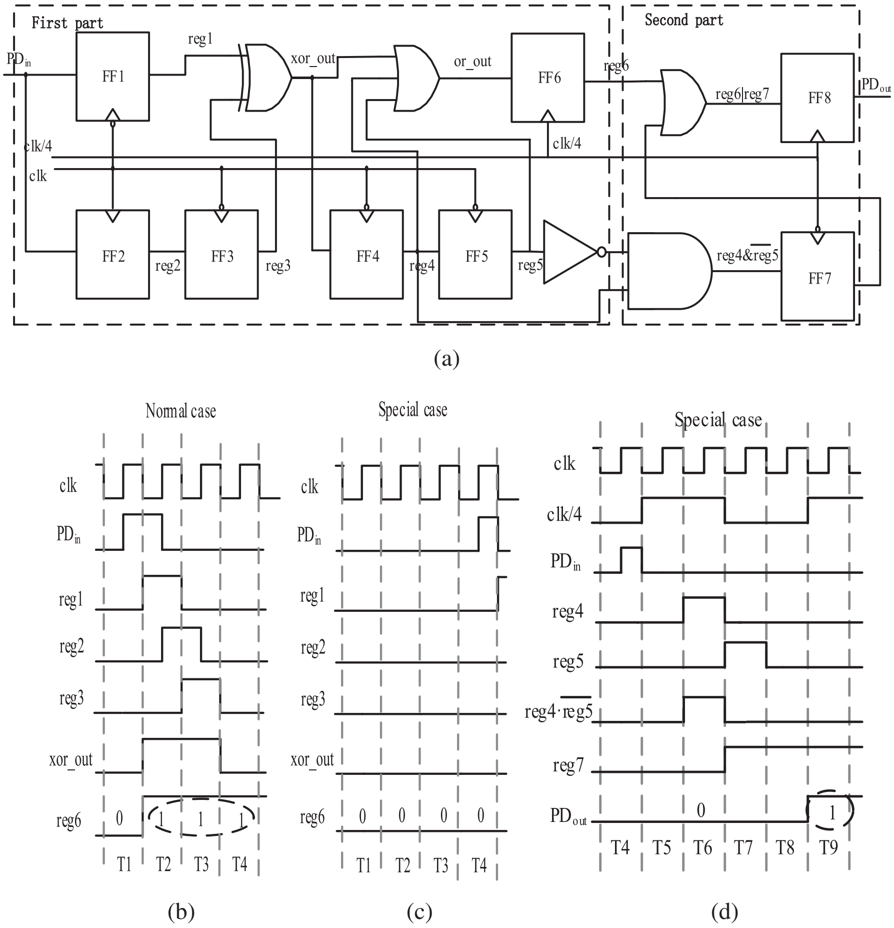

Fig. 6. (a) Phase detector scheme (b) Waveform of phase detector in normal case (“1000”) (c) Waveform of the first part of phase detector in special case (“0001”) (d) Waveform of the second part of phase detector in special case (“0001”)

2.4 Serializer and deserializer for GPD coding

The results of the researches about serializer and deserializer show that serializer can reduce the power consumption of transmitters and transceivers [7]. But the serializer can increase the extra power consumption. The simulation results in [7] show that 4:1 serializer is an optimized ratio to achieve energy saving. A 4:1 tree serdes is introduced in [9] to reduce power consumption and routing resources. In the serdes, multiplexing distribute structure is adopted to form a tree configuration. And samples are taken at the rise and down edges of the clock to achieve a higher converting speed. Fig. 7(a) and (b) shows the scheme of the serializer and deserializer.

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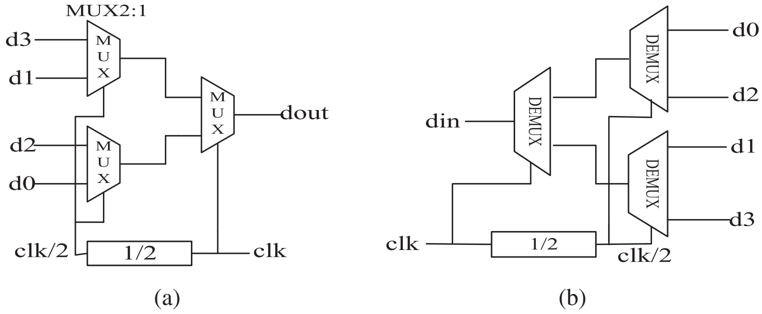

Fig. 7. (a) Serializer scheme. (b) Deserializer scheme

3 Simulation results

Table I shows the area and power consumption ratio of GPD coding circuit under 130 nm CMOS technology in different clock. The GPD coding circuit is composed of GM encoder, phase encoder, GM decoder, and phase checker. As illustrated in Table I, the phase encoder and checker increase the extra power and area. But the area and power of the phase encoder and checker in the overall circuit decrease as the clock frequency increases.

Table I. Area and power of GPD coding circuit under 130 nm CMOS technology

GPD Coding	Area				Power			
	0.5 GHz		1 GHz		0.5 GHz		1 GHz	
	μm²	%	μm²	%	μW	%	μW	%
GM_Encoder	191.8	17%	410.67	29%	65.13	7%	167.7	9%
Phase_Encoder	257.69	23%	210.63	15%	401.39	44%	696.4	38%
GM_Decoder	268.29	24%	377.72	26%	57.5	6%	178.3	10%
Phase_Detector	395.37	36%	431.85	30%	380.4	42%	770	42%
Total	1113.15	100%	1430.87	100%	904.42	100%	1812.4	100%

Table II shows the reduction of the transition for various encoding schemes in the literature by applying the random data source and SPEC95/2000 CINT reference source. Compared with uncoded data, Hamming coding increases the switching activity because of the parity bits and BI coding can only reduce the switching activity by applying the random data source. However, SGC coding and GPD coding can reduce the switching activity by applying the random data source and SPEC95/2000 CINT reference source. According to the simulation results, the GPD coding can make a greater transition reduction than SGC coding. And the transition reduction of the GPD coding is up to 21.16% compared with that of the SGC coding for random data source.

Table III shows the Energy saving of interconnects by applying different coding for the 130 nm CMOS technology at 1.2 V. In the simulation, the frequency of the system clock is set as 1 GHz [8] and the length of interconnects is set as 2 mm of metal-4 with the width of 0.4 um and the spacing of 0.6 um [12]. We have taken many types of the data source into considerations, including the random data source

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Table II. Transition reduction compared with uncoded data by applying different coding

Reference Source	random	compress95	perl	parser	vortex	vpr	mcf
Hamming [10]	−49.81%	−65.08%	−75.68%	−67.33%	−64.69%	−65.26%	−65.64%
BI [11]	7.33%	−2.63%	−1.40%	−2.64%	−2.46%	−2.52%	−2.59%
SGC [7]	16.40%	1.77%	4.45%	2.46%	2.08%	1.81%	1.79%
GPD	37.56%	5.31%	12.09%	6.66%	5.73%	5.37%	5.55%

and SPEC95/2000 CINT reference sources, such as compress95, perl, parser, vortex, vpr and mcf. According to Table III, GPD coding can achieve more energy reduction compared with other coding methods. The final results show that the energy reduction is up to 37.51% for random data source and that the energy reduction is up to 4.13%–8.29% for SPEC95/2000 CINT reference source.

Table III. Energy saving of interconnects by applying different coding.

Reference Source	random	compress95	perl	parser	vortex	vpr	mcf
uncode	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Hamming	−51.39%	−88.11%	−85.90%	−86.26%	−82.96%	−86.21%	−84.73%
BI	7.43%	−3.48%	−0.99%	−1.11%	−1.60%	−1.59%	−1.93%
SGC	17.23%	2.45%	1.86%	4.65%	5.17%	4.22%	1.99%
GPD	37.51%	5.61%	5.66%	6.85%	8.29%	7.46%	4.13%

4 Conclusion

In this paper, a new low-power bus coding called GPD is presented. It is able to reduce the power consumption by reducing the switching activity. The working mechanism of the coding method is elaborated. Simulations results demonstrate that GPD coding achieves 5.37%–37.56% transition reduction and 4.13%–37.51% energy reduction. Compared with other available coding method mentioned in this paper, the proposed GPD provides a further reduced power consumption of the long interconnects in NoC.

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