IEICE Electronics Express, Vol.6, No.22, 1582–1586

Memory cell using Modified Field Effect Diode

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Abstract: Using spice 9.3, we have modeled (I-V) characteristics of a Modified Field Effect Diode (M-FED) with gate length of 75 nm and oxide thickness of 10 nm. An SRAM cell (Register) has been designed with the simulated M-FED and has been compared to an SOI-MOSFET based circuit. Simulation results demonstrate that clock frequency applied to a memory cell which is designed with M-FED is more than 2 orders of magnitude larger than that of a comparable SOI-MOSFET, while the access time of the M-FED based memory cell is three orders of magnitude less than the comparable SOI-MOSFET.

Keywords: Modified Field Effect Diode (M-FED), SOI-MOSFET, SRAM cell

Classification: Electron devices, circuits, and systems

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1 Introduction

The physical structure of the Modified Field Effect Diode (M-FED) is provided in Fig. 1. It has two gates over its channel and the source and drain doping profiles are different from that of a MOSFET. This structure provides orders of magnitude larger current and I_{on}/I_{off} ratio, compared to a regular MOSFET and also does not suffer from short channel effects [1, 2, 3] both of which are attributed to the fact that pinch-off does not occur in M-FED.

In this paper, we have modeled (I-V) characteristics of an M-FED and

DOI: 10.1587/elex.6.1582
Received September 19, 2009
Accepted October 15, 2009
Published November 25, 2009

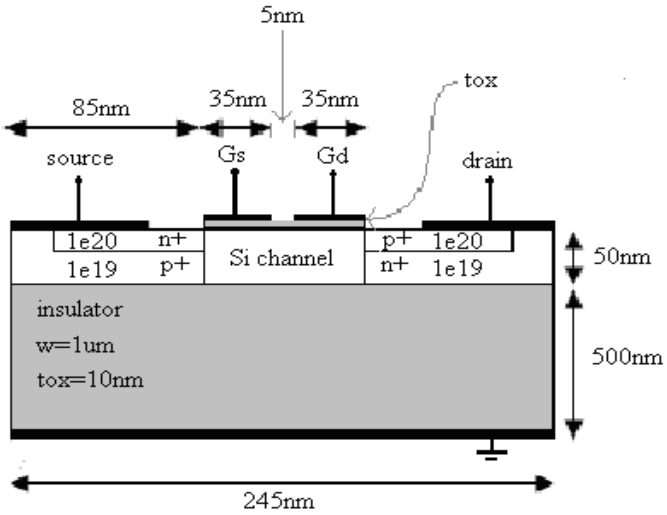

Fig. 1. M-FED structure.

a comparable SOI-MOSFET with channel length of 75 nm and gate oxide thickness of 10 nm. A memory cell has been simulated based on this modeling which demonstrates that the operation speed of M-FED based structures is faster than SOI-MOSFET. The on and off (I-V) curves corresponding to the structure of Fig. 1 which are used in modeling have been presented in [1]. In general, the (I-V) curve of M-FED is similar to that of a regular p-n junction diode with the added feature that the carrier density can be modulated by the two gates. M-FED can be modeled with a diode, a resistor and a voltage source as presented in Fig. 2.

Two parallel paths account for the ON and OFF states which are obtained by the voltages applied to the gates, represented by two switches. The (I-V) curves of the M-FED and that of the MOSFET were obtained by PISCESS-IIB simulation program and then fed to SPICE 9.3 for circuit simulation.

2 SRAM cell simulation

A simple register is composed of a D-Flip-Flop (DFF) and an output controller buffer, Fig. 3.a. It is possible to design D-FF with NAND gates [5], while the NAND gates can be designed based on MOSFET [4] or M-FED [2]. The loading capacitors have been chosen as 20 pf, which are chosen to be much larger than the M-FED parasitic capacitors.

Figs. 3.a and 3.b show the input, output and "clk" signals for SOI-MOSFET-DFF and M-FED-DFF, respectively. When "clk" = "1", the input voltage is transmitted to the output and when "clk" = "0", the output logic of D-FF doesn't change. Figs. 3.a and 3.b demonstrate that M-FED-DFF works about 2 orders of magnitude faster than a comparable SOI-MOSFET-DFF.

The output stage of the register that is shown in Fig. 3.a is composed of a push-pull FED buffer and a switch (swr). The push-pull buffer and swr switch are also based on M-FED. The "ctrl" signal that is applied to swr switch, works as "Read" signal in register. Figs. 3.d and 3.e demonstrate

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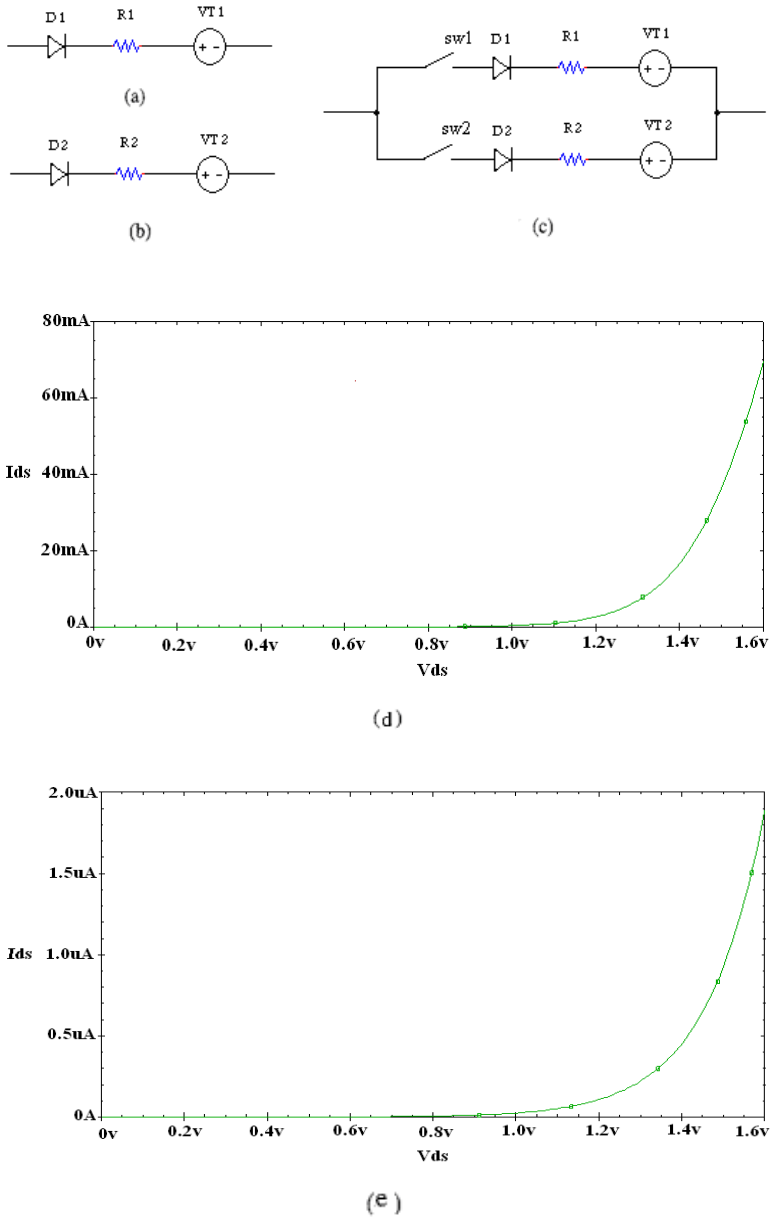

Fig. 2. (a) On-state model of M-FED, (b) Off-state model of M-FED, (c) Complete model of M-FED, (d) On-state (I-V) curve of M-FED model ($V_{GS} = -V_{GD} = 1.5\,v$), (e) Off-state (I-V) curve of M-FED model ($V_{GS} = -V_{GD} = -1.5\,v$).

the "Read" and the "output" signals for SOI-MOSFET register and M-FED register. In addition to frequency of "clk" signal, access time is a factor to evaluate the speed of memories.

It is obvious from Figs. 3.d and 3.e, that t_{ac} in SOI-MOSFET register is about 0.56 usec whereas for a comparable M-FED is about 0.61 nsec, resulting in about three orders of magnitude larger speed with comparable size and power consumption.

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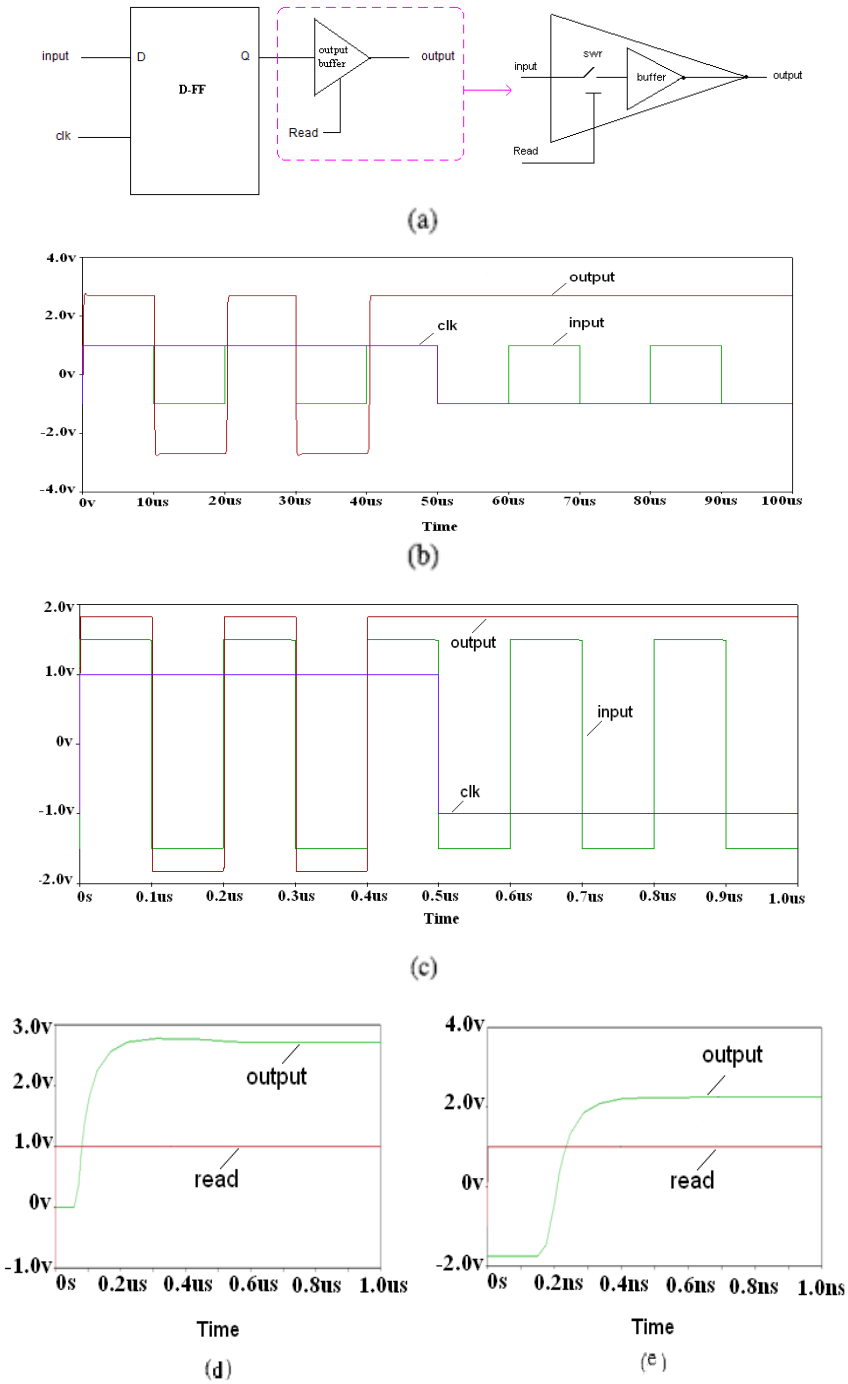

Fig. 3. (a) Structure of a register with output controller buffer, (b) The input, output and "clk" signals for SOI-MOSFET-DFF, (c) The input, output and "clk" signals for M-FED-DFF, It is clear that M-FED-DFF can work 2 orders of magnitude faster than SOI-MOSFET-DFF, (d) The "Read" and the "output" signals for SOI-MOSFET register, (e) The "Read" and the "output" signals for M-FED register, the access time of the M-FED based memory cell is about three orders of magnitude less than the comparable SOI-MOSFET.

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3 Conclusion

The large current handling property of M-FED and its large Ion/Ioff ratio can be used to design SRAM cells (register) which are orders of magnitude faster than comparable MOSFET structures. Since the fabrication steps of M-FED are similar to that of MOSFET, they can easily be incorporated into conventional nanoscale circuits to add speed, functionality or to provide large currents.

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