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A high CMRR low power fully differential Current Buffer

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Abstract: In this paper a low power fully differential current buffer is introduced which performs high CMRR exploiting a novel method to alleviate common mode gain. The proposed current buffer is designed and simulated with HSPICE in 0.18 μm CMOS process and supply voltage of $\pm$0.75 V. The simulation results show an 8.48 Ω input resistance, 98 dB CMRR, 369 MHz bandwidth and power dissipation of 135 μW. The corner case simulation has been done which shows an acceptable performance for the proposed buffer in all situations. The proposed circuit tends to be the fundamental block of a new family of electronic differential topologies greatly capable to be much further improved and utilized.

Keywords: current mode, low input impedance stage, fully differential Current Buffer, high CMRR Current Buffer, low power Current Buffer

Classification: Integrated circuits

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1 Introduction

Excellent performance features of current mode signal processing are the main reasons of current mode design popularity [1, 2, 3, 4]. Unlike the voltage mode circuits, low input resistance is the key feature of current mode circuits. As a result low input impedance current buffer (Current Follower) has gained a great importance and wide application in current mode signal processing, either independently or as an input part of other current processors. For example CF-based active filters and oscillators have been proposed in [5, 6, 7].

The most popular types of current buffers are the common gate (CG) in CMOS technology and common base (CB) in BJT technology [8] which are employed in current mode circuits [9, 10]. These simple current buffers have two main problems. First, their input resistance is in the order of 1/gm, which is not low enough for most current mode processing circuits. One usual method to reduce the input resistance is increasing transistors gm which results in increasing power consumption. Some other techniques have been used in literatures to reduce their input impedance. For example negative feedback method and compensation method [11] each has its own drawbacks. Secondly and more importantly, they are in single-input single-output arrangement as is seen from [10]. By increasing the mixed-mode circuit applications, fully differential structures become more demanded in analog part of the design due to ability to provide more immunity to power supply noises, clock feed through, interferences and other types of common mode disturbances [12]. Because of single-input single–output structure of CG (CB) stage the conventional fully differential current buffer is used employing two CG (CB) stages at the input [9] which have to be matched. In this fully differential current buffer, both common mode and differential mode inputs are transferred to output without any attenuation. So the resulted fully differential current buffer will have a 0 dB CMRR. Low CMRR in fully differential structures is not acceptable, because one of the main reasons of using differential structures is its ability to cancel common mode inputs effect on the output.

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Due to the increasing importance of fully differential structures, in this work a new high CMRR fully differential current buffer based on CG stage is introduced which uses a novel common mode alleviation technique to increase current buffer's CMRR while conserving the low power consumption. Low input impedance for proposed current buffer is provided by a simple positive feedback method. The arrangement of the paper is as follows: In section 2 the proposed buffer is presented. Simulation results are presented in section 3 and finally section 4 concludes the paper.

2 Proposed fully differential current buffer

The proposed current buffer is illustrated in fig.1 in which the sources of M_{r1}-M_{r2} transistors are grounded making zero voltage of the input nodes of the structure due to equality of the currents of the input transistors and M_{r1}-M_{r2} transistors. This arrangement thus results in zero value for input impedance of the proposed current buffer. In practice, the input resistance of this current buffer can be found from:

$$R_{in} = (g_m)^{-1} - (g_{mr})^{-1} \tag{1}$$

Where g_m and gm_r denote the transconductances of the input transistors (M_1-M_2) and the positive feedback network transistors (M_{r1}-M_{r2}) respectively. Ideally by making gm_1 equal to gm_{r1} (and gm_2 equal to gm_{r2}) the input resistance will become zero. But due to the process tolerances we should keep a safe margin to avoid creating negative resistance which may result instability.

The high CMRR for the proposed fully differential current buffer is provided by the circuit enclosed in dashed line which operates as follows:

A portion of the input currents is transferred to M_{B1}-M_{B2} via M_{P3}-M'_{P3}. M_{B1} and M_{B2} are diode connected transistors which have two main rules in the proposed circuit: 1) Providing proper biasing for source coupled pair M_{S1}-M_{S2}, 2) Producing voltages proportional to input currents for the differential pair M_{S1}-M_{S2} inputs.

In the case of common mode inputs, the inputs of differential pair M_{S1}-M_{S2} are proportional to common mode input currents. So voltage at the source of differential pair is proportional to input common mode current. On the other hand, voltage at node A will be approximately equal to the source voltage of differential pair M_{S1}-M_{S2} via the diode connected transistor M_{S3} which is used just for level shifting purpose. As is shown in fig.1, the gate of M_{N1}-M_{N2} in the output branch is connected to node A so their output currents are proportional to input common mode currents. By proper choosing the aspect ratios of M_{N1}-M_{N2}, their output currents in common mode can be made very close to input common mode currents. On the other hand, the input common mode currents are transferred to the output branches by M_{P0}-M'_{P0} where are subtracted from M_{N1}-M_{N2} output currents and hence a much attenuated common mode current is transferred to the loads resulting a high CMRR. The common mode gain of the proposed current buffer

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can be found from (2) assuming a high output impedance current source for differential pair.

$$A_c = (\lambda_2 - \lambda_1.gm_{N1,2}.(gm_{B1,2})^{-1}) \quad (2)$$

In (2) λ_2 and λ_1 are the current transfer gain of M_{P0}-M_{P1} (or M'_{P0}-M'_{P1}) and M_{P1}-M_{P3} (or M'_{P1}-M'_{P3}) current mirrors respectively and gm_N and gm_B are transconductances of M_{N1}-M_{N2} and M_{B1}-M_{B2} transistors respectively. As (2) implies, by proper choosing M_{N1}-M_{N2} and M_{B1}-M_{B2} transistors transconductances, the common mode gain of current buffer can be made near zero resulting a high CMRR.

In the case of differential mode input currents, voltage at node A is at virtual ground so the differential mode current of M_{N1}-M_{N2} is zero and hence the input current is transferred to the output by M_{P0}-M'_{P0} resulting the differential mode gain of current buffer to be found from:

$$A_d = \lambda_2 \quad (3)$$

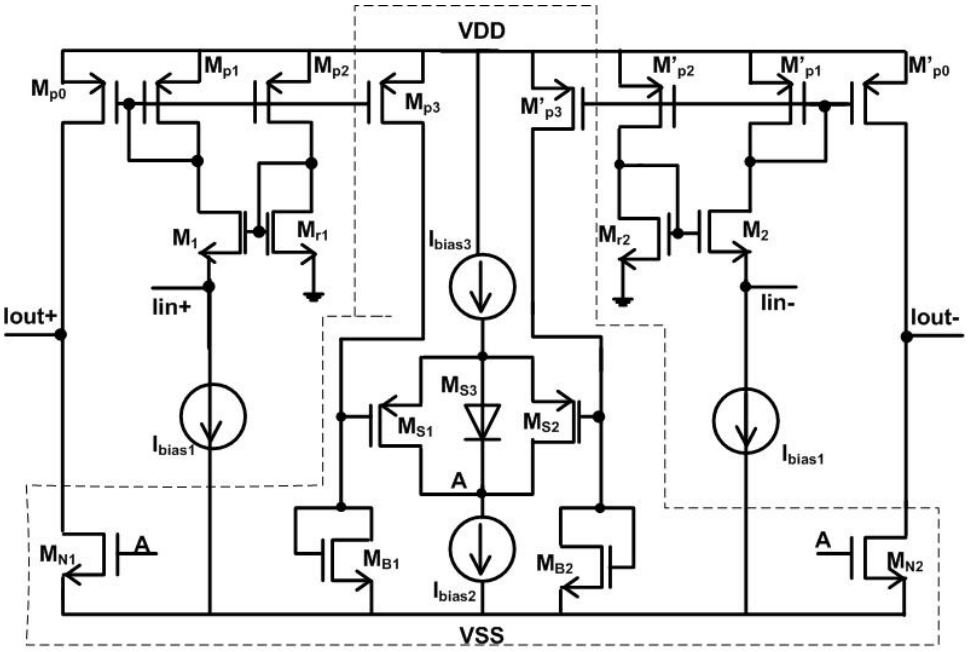

Fig. 1. The proposed current buffer

Due to the low input impedance of current buffer, the produced pole by input capacitors is negligible and the $-3\,\mathrm{dB}$ frequency of the proposed current buffer is determined by current mirrors M_{P0}-M_{P1} (and M'_{P0}-M'_{P1}). Using (2) and (3), the CMRR of proposed current buffer becomes:

$$CMRR = \lambda_2 \times (\lambda_2 - \lambda_1 \frac{g_{mN1,2}}{g_{mB1,2}})^{-1} \quad (4)$$

The proposed buffer needs at least a supply voltage of $V_{Th}+ 3V_{DS}$ which is the same for conventional CG based fully differential current buffer too. By choosing a low bias current for the proposed circuit in dashed line in fig.1, the total power consumption can be further lowered.

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The proposed circuit is actually the innovative combination of many deliberate powerful ideas so effective that grant a wide range of merits like high CMRR, low input impedance, low power, moderately low voltage and wide bandwidth to a single compact differential structure. The proposed structure thus can be considered as a fundamental block well qualified to be much further improved presenting a new differential topology to both societies of designers and consumers of electronic processors.

3 Simulation results

The proposed circuit is simulated with HSPICE using the model parameters of 0.18 μm CMOS process. The supply voltage is $\pm$0.75 V and bias current for all transistors is 10 μA. Eachoutput terminal is connected to a grounded 1 KΩ resistor. The frequency performance of the main parameters of proposed buffer is shown in fig.2. Figure 2-a shows the frequency response of the input resistance. The proposed fully differential current buffer has an input resistance of 8.48 Ω and stays under 20 Ω up to 1 MHz. The gain frequency response of the proposed current buffer, Ai, is not shown here due to space limitation. However, it is equal to 1.05, rolling off at -3 dB frequency of 364 MHz without any peak. CMRR frequency performance is shown in fig.2-b which shows 98 dB for DC magnitude and -3 dB bandwidth of 3.7 KHz. To study the stability of the block, fig.2-c shows its output response to an input step of $\pm$5 μA both in typical case and all standard corner cases simulations validating its secure stability. The simulation results of the standard corner cases are compared with the typical case ones in Table I which evident a high performance current buffer in typical case (TT) and an acceptable one in all standard corners. In worst case, the proposed current buffer has CMRR of 29 dB which is still 29 dB higher than the CMRR of conventional fully differential current buffer. The power consumption of proposed buffer is 135 μW.

Table I. Comparative results of the performance of the proposed current buffer in different cases

specifications	Typical case (TT)	Corner cases			
		FF	FS	SS	SF
BW(MHz)	364	427	336	337	188
Rin(Ω)	8.48	140	73.8	500	417
CMRR(dB)	98	58	29	45	29
Power Dissipation(μW)	135	139.3	132.88	125.29	130.38

4 Conclusions

This paper proposes a novel fully differential current buffer employing a novel common mode alleviation method. In the proposed method, common mode currents are simply canceled at the output branch before injecting to the loads. Unlike the conventional common mode feedback method, the proposed method is very simple and no frequency compensation is needed. The

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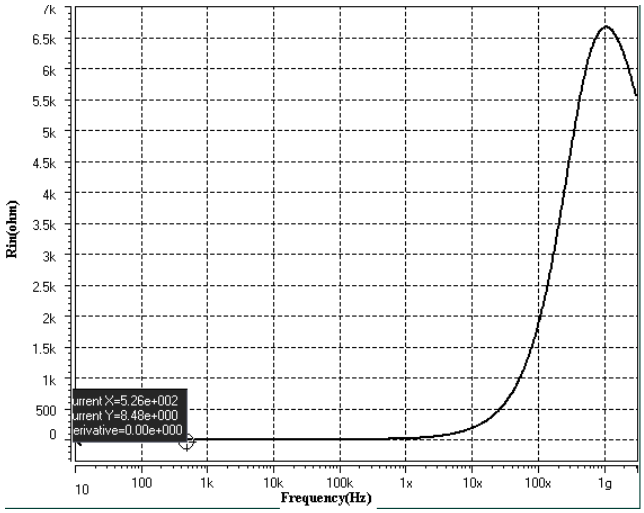
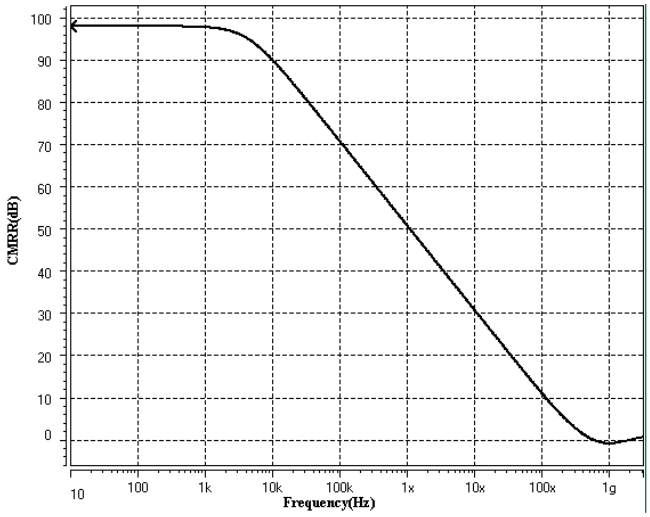
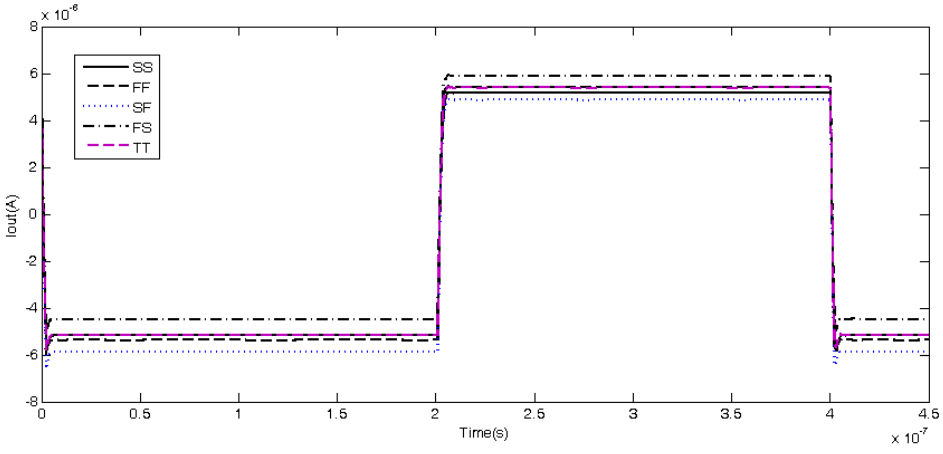


(a)



(b)



(c)

Fig. 2. The proposed buffer simulation results (a) Input resistance (b) CMRR (c) Step response of all cases

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proposed method can be simply combined with other methods to reduce input impedance as in this paper the positive feedback is used. The CMRR of the buffer is very high. Low input impedance of current mirror and its high CMRR makes it suitable for accurate applications.

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