

Variable resolution SAR ADC architecture with 99.6% reduction in switching energy over conventional scheme

Jiaojiao Yao, Zhangming Zhu^{a)}, Yutao Wang, and Yintang Yang

School of Microelectronics, Xidian University, Xi'an 710071, P. R. China

a) zmyh@263.net

Abstract: A novel energy-efficient switching method for variable resolution successive approximation register (SAR) analogue-to-digital converters (ADCs) is presented. The proposed switching scheme achieves switching energy inspired by the early reset merged capacitor switching algorithm (EMCS) and monotonic capacitor switching procedure. Besides, the dummy capacitors are used to further reduce power consumption and area. When sized for the same static linearity as the conventional SAR ADC, the proposed method enhances the efficiency of switching energy by 99.6% and reduces the total area by 93.75%. Furthermore, the proposed scheme can achieve a variable resolution for SAR ADCs.

Keywords: SAR ADC, switching scheme, EMCS, monotonic, energy efficiency

Classification: Integrated circuits

References

- [1] C. Yuan and Y. Lam: *Electron. Lett.* **48** (2012) 482. DOI:10.1049/el.2011.4001
- [2] A. Sanyal and N. Sun: *Electron. Lett.* **49** (2013) 248. DOI:10.1049/el.2012.3900
- [3] H. Song and M. Lee: *IEICE Electron. Express* **11** (2014) 20140345. DOI:10.1587/elex.11.20140345
- [4] L. Xie, G. Wen, J. Liu and Y. Wang: *Electron. Lett.* **50** (2014) 22. DOI:10.1049/el.2013.2794
- [5] J. S. Lee and I. C. Park: *Int. Symp. Circuits and Systems* (2008) 236. DOI:10.1109/ISCAS.2008.4541398
- [6] S. R. Srinivasan and P. T. Balsara: *Electron. Lett.* **50** (2014) 1421. DOI:10.1049/el.2014.1760

1 Introduction

SAR ADC is one of the most popular topologies for medium to high resolution application. With the supply voltage scaling, new methods for reducing the power of capacitor arrays become popular. Recent state-of-the-art has introduced several techniques to reduce the switching energy. Compared to the conventional architecture, the new tri-level [1], Sanyal and Sun [2], asymmetric monotonic [3] and

hybrid capacitor [4] reduce the switching energy by 96.89%, 98.4%, 98.5% and 98.83%, respectively. The switching architecture in [5] employing the previous bits to control the splitting capacitors of the sub-DAC has significant energy consumption from the first two comparison cycles, and wastes the same large capacitor area as the conventional scheme. In this paper, a novel switching scheme is presented that achieves a reduction of 99.6% and 93.75% in the switching energy and area when sized for the same static linearity as the conventional SAR ADC. Similar to [6], the new scheme is favorable to reconfigurable application.

2 Proposed switching scheme

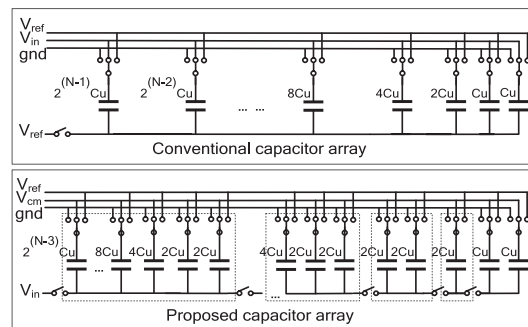


Fig. 1. Capacitor arrays of conventional and proposed switching schemes

The proposed switching scheme divides the $2^i C_u$ ($i > 1$) in the conventional capacitor arrays into binary-weighted capacitors, with the unit capacitor of $2C_u$ (as shown in Fig. 1). Fig. 2 shows the DAC switching scheme for a 4-bit SAR ADC. The proposed scheme is a factor of 4 less than the conventional architecture in the total number of unit capacitor. The switching scheme is realized in four phases: most significant bit (MSB), 2nd-MSB, 3rd-MSB to 2nd-LSB (second least significant bit) and LSB. In the first phase, the differential input signal is sampled on the top-plates of both capacitor arrays, and the bottom-plates of capacitors are initially connected to the common-mode voltage V_{cm} which is $0.5V_{ref}$. After turning off all the switches splitting the capacitors, the MSB is obtained. In the second phase, the SAR logic will switch the bottom-plates of the main-DAC capacitors which sample the higher input voltage to gnd and the other main-DAC capacitors remain unchanged. Then the 2nd-MSB is obtained. In the third phase, the sub-DAC utilizes all the previous bits to generate the next reference voltage. The positive and negative reference voltages on the V_{XP} and V_{XN} side are shown in Table I. Then this sub-DAC merges with the main-DAC and becomes a part of it. This procedure continues until the 2nd-LSB is determined. In the LSB phase, the dummy capacitors are used. Table II shows the conversion mode of two dummy capacitors.

As shown in Fig. 2, this novel switching architecture wastes no energy in the first two steps. Only one dummy capacitor is switched to determine the LSB, resulting in less switching activity and lower energy consumption. Besides, the proposed scheme requires $2(N-9)$ more switches than the conventional structure. In

other words, the increased number of switches is only 2 for 10 bit ADC, which is not significant, as the process technology improves. The increasing number of the switches leads to more interconnection lines which produce excessive power dissipation; however, placing the capacitors controlled by the same switches compactly and nearly to the controlling switches is a way to reduce the power consumption and area.

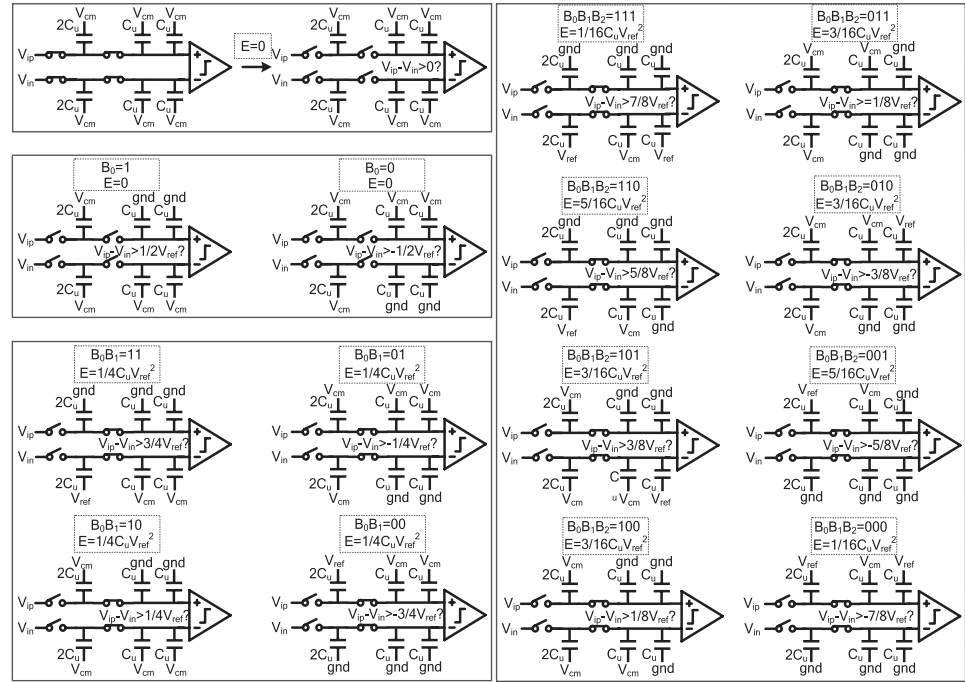


Fig. 2. Switching sequence and energy consumption of a 4-bit ADC with proposed switching scheme

Table I. Different reference voltages based on first comparison result

	MSB = 1		MSB = 0	
Differential input	V _{XP} side	V _{XN} side	V _{XP} side	V _{XN} side
Positive reference	V _{cm}	V _{ref}	V _{ref}	V _{cm}
Negative reference	gnd	V _{cm}	V _{cm}	gnd

Table II. Conversion mode of two dummy capacitors

	MSB = 1		MSB = 0	
(N – 1)th bit	1	0	1	0
Positive reference	gnd	gnd	gnd	V _{ref}
Negative reference	V _{ref}	gnd	gnd	gnd

Figs. 3a and b provide an illustration of the waveforms of the hybrid capacitor switching scheme [4] and the proposed technique. As it is shown, the common-mode voltage of the proposed switching scheme will monotonically approach V_{cm}.

3 DAC control logic analysis

DAC control logics of the proposed circuit are shown in Fig. 4. As we can see, control logics of the unit capacitor (C), the dummy capacitor (C_{dummy}), and the (i – 1)th capacitor in the sub-DAC (C_{sub,i-1}) are different. These logics are accept-

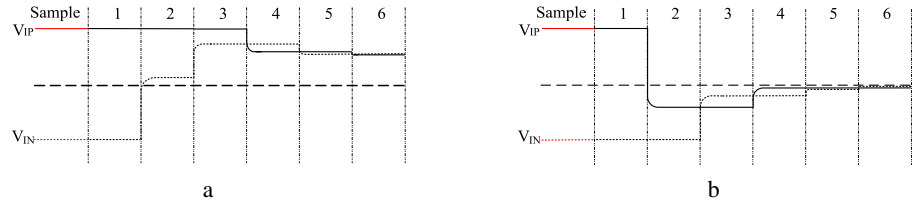


Fig. 3. Waveforms of hybrid switching scheme and proposed switching scheme
a Hybrid switching scheme
b Proposed switching scheme

able in complexity. As the process technology improves, the total area and energy consumption in the SAR logic are small enough compared to the switching capacitor array.

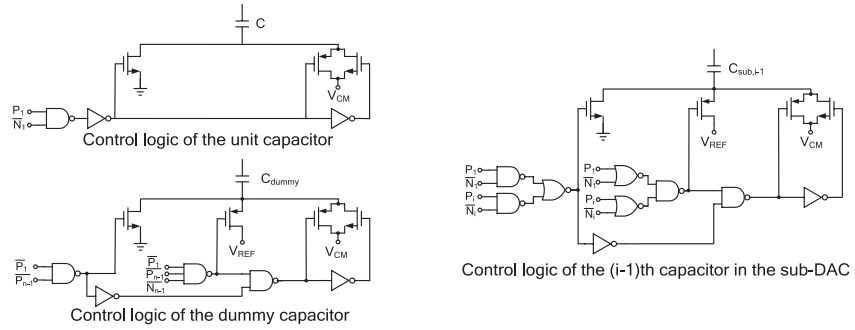


Fig. 4. Control logics of the proposed switching scheme

4 Switching energy analysis

For the proposed method, the switching energy required to generate the M th (b_{M-1}) can be written as

$$E_M = \begin{cases} 0, & M = 1, 2 \\ \frac{1}{2^{M-1}} \cdot C_u \cdot V_{ref}^2, & M = 3 \\ \frac{1}{2^{M-1}} \cdot C_u \cdot V_{ref}^2 + \frac{1}{2} \left(1 - \frac{C_{Vref}}{C_{Total}^{sub-DAC}} \right) \cdot C_{Vref} \cdot V_{ref}^2, & M \in [4, N-1] \\ \frac{1}{2^M} \cdot C_u \cdot V_{ref}^2 + A \cdot \left(\frac{1}{2} - \frac{1}{2^{M-2}} \right) \cdot C_u \cdot V_{ref}^2 + \frac{(-1)^A \cdot B}{2^M} \cdot C_u \cdot V_{ref}^2, & M = N \end{cases}$$

where C_{Vref} , $C_{Total}^{sub-DAC}$, A and B are given by

$$C_{Vref} = \sum_{i=1}^{M-2} C_i \cdot (b_i \odot b_0)$$

$$C_i = \begin{cases} 2^{M-2-i} C_u, & i \neq M-2 \\ 2C_u, & i = M-2 \end{cases}$$

$$C_{Total}^{sub-DAC} = 2^{M-2} C_u$$

$$A = b_{M-2} \oplus b_0$$

$$B = \sum_{i=1}^{M-3} 2^{M-2-i} (b_i \oplus b_0)$$

Table III summarizes the features of different switching schemes for a 10 bit SAR ADC. It can be seen that the proposed method is competitive with the current state-of-the-art. The average switching energies for the sub-DAC merging switch [6] and the proposed switch are $10.67C_u V_{\text{ref}}^2$ and $5.4C_u V_{\text{ref}}^2$ respectively when sized for the same static linearity.

Table III. Comparison of switching schemes for 10-bit SAR ADC

Switching scheme	Average switching energy ($C_u V_{\text{ref}}^2$)	Energy saving	Area reduction
Conventional	1363.3	Reference	Reference
New tri-level [1]	42.41	96.89%	75%
Sanyal and Sun [2]	21.3	98.4%	75%
Asymmetric monotonic [3]	19.84	98.5%	50%
Hybrid capacitor [4]	15.88	98.83%	75%
Sub-DAC merging [6]	42.67 (noise-matched)	96.9%	50%
	10.67 (linearity-matched)	99.21%	87.5%
Proposed	21.58 (noise-matched)	98.4%	75%
	5.4 (linearity-matched)	99.6%	93.75%

5 Linearity analysis

The worst case transitions are from $[1, V_{\text{cm}}, 1, 1, 1 \dots]$ to $[1, 1, V_{\text{cm}}, V_{\text{cm}}, V_{\text{cm}} \dots]$ and $[0, 0, V_{\text{cm}}, V_{\text{cm}}, V_{\text{cm}} \dots]$ to $[0, V_{\text{cm}}, 0, 0, 0 \dots]$. Assuming that the unit capacitor is modelled with nominal value of C_u and a standard deviation of σ_u , the maximum standard deviation of integral and differential nonlinearities (INL and DNL) for the proposed scheme can be calculated as $0.5 \times 2^{(n/2-1)}\sigma_u$ and $2^{(n/2-1)}\sigma_u$ LBSs, respectively. Reduced INL and DNL by a factor of 2 halves the capacitor matching requirement compared to the conventional switching scheme. In addition, process mismatches can be reduced by arranging unit-sized capacitors to make up of a large splitting capacitor.

6 Conclusion

A novel switching scheme for a variable resolution SAR ADC is proposed. Compared with the sub-DAC merging scheme, the proposed scheme is more energy-efficient in the first two and the last comparison cycles. The presented scheme is reduced by 12.5% in common-mode voltage variation compared to the hybrid capacitor scheme. The improved static linearity by a factor of 2 also relaxes the capacitor matching requirements of the DAC array.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (61234002, 61322405, 61306044, 61376033), the National High-tech Program of China (2013AA014103).