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An improved timing monitor for deep dynamic voltage scaling system

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Abstract: In the current Dynamic voltage scaling (DVS) integrated circuits, sufficient timing and voltage margins are typically wasted, because it is difficult to anticipate the exact amount by which the voltage or frequency should be scaled. The on-chip timing monitoring method is effective for this problem. In this paper, an improved timing monitor circuit with a fast error comparator is designed to detect and correct timing errors, and then it is used in a DVS system on 65 nm CMOS technology for deep DVS. Post-layout simulation results show that the monitor performs well in different process corners with a wide voltage range and wide temperature range. Compared with the non-DVS circuit supplied by a fixed 1.2 V voltage, our timing monitor based DVS system can save, on average, 33.4% dynamic power in different corners at the expense of 22.9% increased area.

Keywords: low power, Dynamic voltage scaling, integrated circuit

Classification: Integrated circuits

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1 Introduction

The dynamic voltage scaling (DVS) method is very effective at decreasing a chip's power consumption, in that the supply voltage and frequency can be dynamically adjusted according to application demands. However, the currently used DVS methods cannot decrease the supply voltage to the best, because sufficient timing and voltage margins are reserved to resist the impact of environmental variations, transistor model inaccuracy, and EDA tool limitation, etc. [1, 2, 3, 4, 5, 6].

Razor [2, 3] is a kind of error detection flip-flop used to eliminate excess timing margins through real-time detection of chip operations. Microprocessors with several pipeline stages can be redesigned for low power by combining error detection and micro-architectural recovery mechanisms [2, 4, 5, 6]. However, these methods are usually closely dependent on the chip architecture.

In this paper, an improved timing monitor circuit is designed and applied within a pipeline stage DVS system. Its advantages are: 1) a custom designed monitor circuit with an optimized error signal generator to improve its performance; 2) a simplified error recovery mechanism not dependent on the chip architecture; 3) a closed-loop feedback control voltage adjustment method with open-loop support for the initial control value.

2 Timing monitor circuit design, layout and simulation

The timing monitor circuits are inserted at the endpoints of the critical paths instead of the usual D flip-flops (DFFs) to monitor its working status and further correct the timing error. It is mainly composed of a DFF, a parallel shadow latch, a metastability detector, a 2-to-1 Multiplexer (MUX2), an OR2

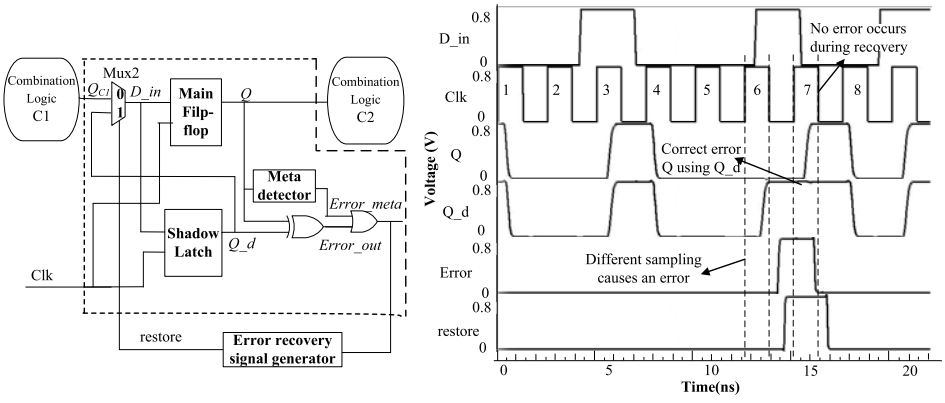

Fig. 1. (a) Block diagram of the timing monitor (b) Simulation timing results

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gate and a XOR2 gate [3], as shown in Fig. 1 (a). It relies on the shadow latch with an additional half-cycle setup time, since it samples the input data D_in on the negative clock edge. Therefore, it will maintain a correct timing when the main flip-flop begins to fail the timing requirements. At this time, a timing error "error_out" is generated once the output of the main flip-flop differs from that of the shadow latch.

Our transistor level timing monitor circuit is shown in Fig. 2, with its simulated timing results shown in Fig. 1 (b). The output of main flip-flop ① Q3 is compared with output Q5 of and the shadow latch ② through error signal generator ③. This error status is also used to generate a restore signal to recover the output from the incorrect state Q3 with Q5 by error recovery unit ④, since Q5 remains correct at this time. The error recovery unit ④ is a tri-state gate as a multiplexor MUX2 controlled by "restore" signal, which is generated by error recovery signal generator ⑥ for data recovery after errant status occurs. The metastability detector ⑤ is composed of one standard and two skewed inverters to detect metastable state. The final Error signal is the XOR of error_out and error_meta.

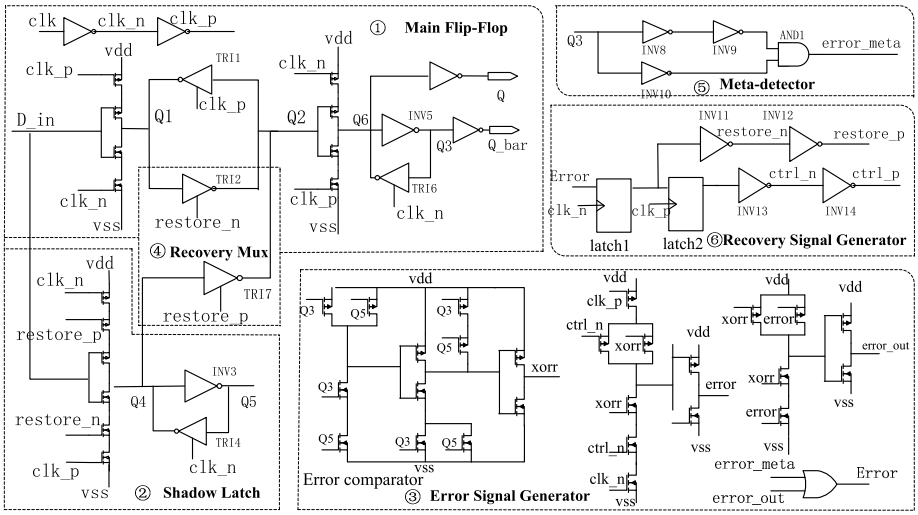

Fig. 2. Transistor Level Schematic of the Timing Monitor Circuit

Here a new error signal generator, under the control of the "restore" signal is designed instead of the original dynamic logic structure with several stacks of three transistors in [3], which improves the frequency of the whole timing monitor circuit. "ctrl_n" is the negative signal of the half cycle delayed "restore" signal, which is used to reset the "Error" signal after restoring the errant system. In this error signal generator, first the output of the main flip-flop and that of the shadow latch is XORed to generator "xorr" signal, then "xorr" is controlled by "Clk" and "ctrl_n" to generate an "error_out" signal which lasts a half cycle at only negative clock cycle. Finally, the "error_out" is XORed with the metastability detecting result "error_meta" to generate the final timing "Error" signal.

Its working principle can be illustrated according to the simulation results

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of Fig. 1 (b) at f = 400 MHz, V = 0.8 V, T = 100°C, and TT corner. During the first five clock cycles, no timing violation occurs. While in the sixth cycle, D_in arrives late after the positive edge of "clk", so that the error comparator detects a discrepancy between the data sampled by the main flip-flop and the shadow latch, which causes an error. Then, under the control of the restore signal, Q_d is used to recover the timing error to guarantee that the eventual output Q is correct. It should be noted that during the error recovery process, new timing errors will be ignored and an additional clock cycle is sacrificed for error correction.

Under identical operation and measurement conditions, the average power of the designed timing monitor circuit is 2.4/2.1 times larger than that of the DFF cell (DRNQHSV2 in TSMC 65 nm standard cell library) at 1.2 V/0.8 V supply voltage.

Further simulations under different process corners, voltages, and temperature ranges show that the timing monitor circuit performs well in different process corners at a frequency of 400 MHz and in the voltage range of 0.8 V–1.2 V as well as the temperature range of −50°C–100°C. Its operation frequency could also be decreased which will further enlarge the working voltage range.

3 Timing monitor based DVS system and voltage control

To use the error detection and correction FF for deep DVS, a pipeline system as shown in Fig. 3 is built with error recovery. Its main body is a three-pipeline stage multiplication circuit with the critical paths monitored. Furthermore, an error recovery signal generator and a DVS module are added for voltage adjustment.

The inputs of the DVS system are two 4-bit Mul_a[3:0] and Mul_b[3:0] of the multipliers, while its output is an 8-bit result Mul_out[7:0]. After RTL (Register Transfer Level) design, the timing is analyzed via Design Compiler. According to the timing analysis, the critical paths are found

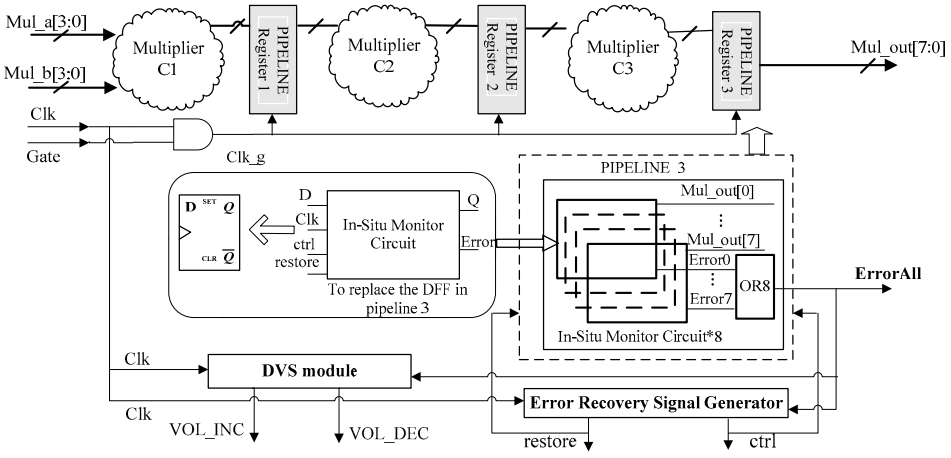

Fig. 3. Construction of the Timing Monitor Based DVS System

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in pipeline 3, and accordingly the eight standard DFFs at the endpoints of pipeline3 are replaced by timing monitors. By combining all the eight individual error signals, the composite ErrorAll is generated as the alarm signal for the DVS module to generate a voltage increase signal VOL_INC or a voltage decrease signal VOL_DEC. Here an additional clock cycle is needed for error correction, so the clock is gated when a timing error appears to guarantee that the whole pipeline works correctly.

4 Simulated power reduction results

The layout of the expanded DVS system is designed under SMIC 65 nm process with an area of 40.60 μm $\times$ 40.40 μm, which occupies 22.9% more area. However, in a large system, this area penalty will be decreased dramatically.

The DVS control process is as follows. If any timing error occurs, the DVS module generates a VOL_INC signal and the whole system corrects timing errors with one clock gated to prevent error transmission. Otherwise, the current voltage is maintained until there are no timing errors in the continuous M clock cycles, and then VOL_DEC is generated to decrease the supply voltage for further voltage margin reduction. Here M is a parameter determined by the specific application and the voltage settling time of the DC/DC converter.

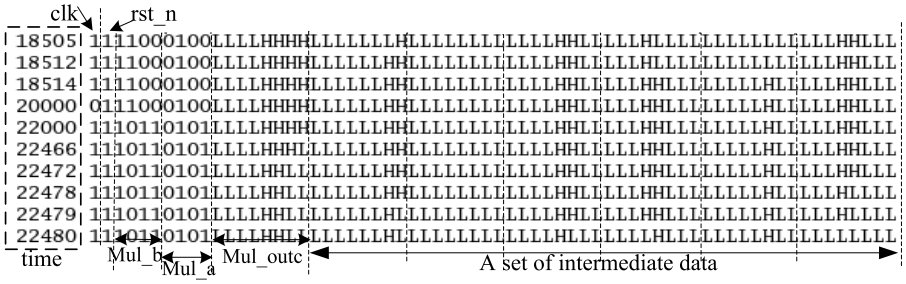

Fig. 4. Part of the input vector of the DVS system for HSIM post-layout simulations

The first step of simulation is functional verification by VCS tool, which could not reveal timing characteristics. Then the verified input and output data are mapped into a long vector to be used in HSIM post-layout simulations. Part of the vector is shown in Fig. 4, covering clock, reset, input Mul_a[3:0], Mul_b[3:0] and the theoretical output Mul_outc[7:0], as well as intermediate data. During post-layout simulation, HSIM compares the theoretical output and intermediate data with the circuit generated data, to verify the correctness of the monitoring system. By applying more than 10,000 input patterns, the outputs of the multiplier as well as the monitored error signal are all correct as assumed.

A simplified DVS control flow is used here for demonstration as shown in Fig. 5 with T = 25°C and f = 300 MHz in FF corner. (1) At the very beginning, the voltage generator determines a suitable initial open loop supply voltage (0.9 V here) from a built-in look-up table. (2) At this relatively con-

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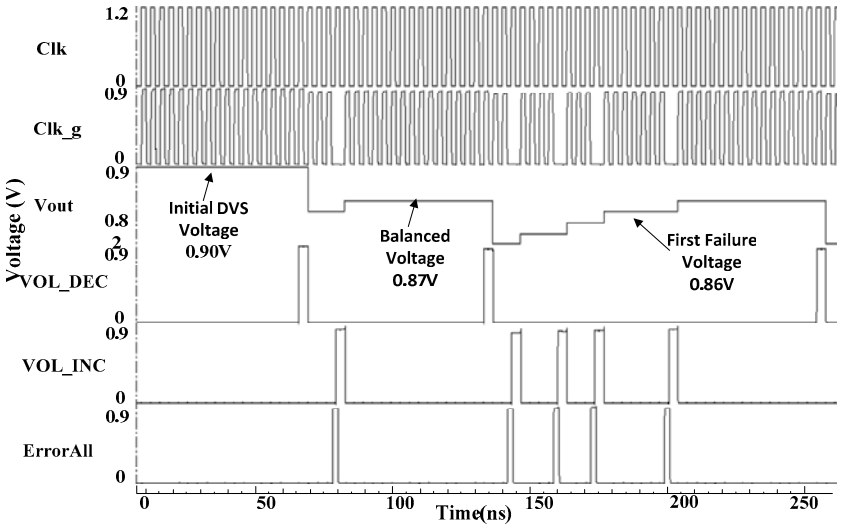

Fig. 5. DVS voltage control system simulation results

servative supply voltage, VOL_DEC is generated after M clock cycles without any timing errors (M = 16 here for example), which reduces supply voltage by 0.04 V. (3) The decreased supply voltage of 0.86 V results in a timing error as detected by the eight timing monitor circuits in the critical paths, and this triggers a corresponding VOL_INC. (4) Then the supply voltage is increased by a 0.01 V step, and one clock cycle is gated to correct timing and to prevent error transmission. The whole DVS system finally adapts itself to a balanced voltage of 0.87 V. Its performances in different corners are also simulated. Compared with the original non-DVS average power under the same operation conditions (f = 300 MHz and T = 25°C), the power savings under five different process corners are: 47.94% under FF corner, 22.75% under SS corner, 32.61% under TT corner, 31.64% under SNFP corner and 32.20% for the FNSP corner.

5 Operating voltage range analysis

There are two kinds of circumstances to discuss the operating voltage range of the error detection systems. First, for a fixed frequency, since the static timing analysis at design time guarantees at least ±10% voltage range for the chip (the lower frequency, the lower allowable voltage), thus, the main contribution of the in-situ monitoring is to find the lowest applicable voltage to eliminate the timing margin [3]. Second, if the frequency is also scalable, the operating voltage could be further scaled while guaranteeing the timing in different PVT corners at design time. Since it is unable to cover every frequency and voltage combinations, usually several typical frequencies are optimized for timing [5]. In our design, the working frequency of 300 MHz for the DVS system is not the highest frequency, therefore, it could be a relatively wide 0.87 V∼1.2 V range.

It should be noted that no matter for what kinds of the situation, during the design time, at each combination of PVT (process, voltage, temperature) and frequency, the correct timing should be designed to guarantee that the

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shadow latch can fetch the correct value even for the worst activated critical path. Otherwise, the chip will not work correctly, not to mention to correct errors.

6 Conclusion

This paper designed an improved timing monitor circuit as well as a DVS control system based on timing error detection and correction. The timing monitor is used in a DVS system of a three-stage-pipeline multiplication unit with error recovery and voltage control modules. Post-layout HSIM simulations showed that 22.75% to 47.94% dynamic power could be saved in different corners at 300 MHz and 25°C compared with the non-DVS design with 22.9% extra area, thus providing a good low power solution for high performance circuits.

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