ELectronics EXpress

IEICE Electronics Express, Vol.8, No.1, 20–25

All-digital ramp waveform generator for two-step single-slope ADC

Tetsuya Iizuka[a)] **and Kunihiro Asada**

VLSI Design and Education Center (VDEC), University of Tokyo

2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-0032, Japan

a) *iizuka@vdec.u-tokyo.ac.jp*

Abstract: This paper presents an all-digital on-chip ramp waveform generator for an 8-bit single-slope ADC. The proposed ramp waveform generator consists of static CMOS digital circuits and is designed using standard cells aiming for the process portability. The proposed circuit realizes digitally-controlled ramp output and also realizes two step coarse-fine ramp waveform to speed up the single-slope analog-to-digital conversion. The experimental results of the circuit simulation with random variation on 0.18 μm CMOS process demonstrate the feasibility of our ramp waveform generator and 8-bit two-step single-slope ADC with DNL within ±0.2LSB and INL within ±0.8LSB.

Keywords: analog-to-digital converter, single-slope ADC, ramp waveform generator, all-digital

Classification: Integrated circuits

References

[1] M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2968–2977, Dec. 2007.

[2] S. Lim, J. Lee, D. Kim, and G. Han, "A High-Speed CMOS Image Sensor With Column-Parallel Two-Step Single-Slope ADCs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 393–398, March 2009.

[3] W. F. Lin and H. P. Chou, "A Fast Single Slope ADC with Vernier Delay Line Technique," *IEEE Nuclear Science Symp. Conf. Record*, pp. 313–317, Nov. 2009.

[4] M. Park and M. H. Perrott, "A Single-Slope 80 MS/s ADC using Two-Step Time-to-Digital Conversion," *Proc. IEEE Int. Symp. Circuits Syst.*, pp. 373–376, May 2009.

[5] S. B. Kobenge and H. Yang, "A 250 KS/s, 0.8 V Ultra-Low Power Successive Approximation Register ADC using a Dynamic Rail-to-Rail Comparator," *IEICE Electron. Express*, vol. 7, no. 4, pp. 261–267, Feb. 2010.

1 Introduction

Integrating type analog-to-digital converter (ADC), such as single or dual

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011

slope ADC is one of the most traditional and simplest implementation of the analog-to-digital conversion. This type of ADC is commonly used in the areas of CMOS image sensors, radiation sensors, and so on [1, 2, 3, 4]. A single-slope ADC has an advantage of its simplest implementation with minimal analog contents and can provide higher ADC resolution and linearity with the cost of the conversion time. Thus, this type of ADC is often used for the applications which requires high precision with relatively slow conversion frequency. One of the key components of the single-slope ADC is a ramp waveform generator. A lot of types of ramp waveform generators such as analog integrator, current DAC, capacitance DAC, etc. have been used. Recently, new types of integrating ADC based on Time-to-Digital Converter (TDC) is also proposed to improve the conversion time which is limited by a clock period of a digital counter [3, 4].

In this paper, we present an all-digital ramp waveform generator based on a shift register and a capacitance DAC for an on-chip single-slope ADC. This ramp generator consists of static CMOS digital circuits and is designed using standard-cells aiming for higher process portability. The proposed ramp generator also realizes two-step coarse-fine ramp waveform to improve the conversion time of the 8-bit single-slope ADC.

2 All-digital two-step ramp waveform generator

A schematic diagram of the proposed all-digital ramp waveform generator is illustrated in Fig. 1 (a). The proposed ramp generator is based on a shift register type capacitance DAC to guarantee a monotonicity of the ramp output. All the capacitors connected to the DFF outputs have unit capacitance value C and all the circuit block except capacitors are static CMOS logic circuits. The shift register block has 2^x columns and 2^y rows. To generate the ramp waveform for N-bit steps, 2^N unit capacitors are required. Thus the following equations are derived.

$$2^N = 2^x \times 2^y, \quad N = x + y. \tag{1}$$

Before starting the ramp output, all the output of 2^N DFFs are reset to 0 V and V_{RAMP} output is also reset to 0 V. During the coarse ramp generation which is followed by the fine ramp generation, the DFFs shift their data vertically using the selector "1" input. Therefore the output of the 2^x DFFs are turned into V_{DD} simultaneously by a single clock. On the other hand of the fine ramp generation, the DFFs shift their data horizontally using the selector "0" input and the output of only a single DFF is turned into V_{DD} by a single clock. This coarse-fine ramp generation process also guarantees a monotonicity of the ramp output. Since the output voltage V_{RAMP} is written as

$$V_{RAMP} = \frac{n \times C}{2^N \times C} V_{DD} = \frac{n}{2^N} V_{DD} \quad (0 \le n \le 2^N) \tag{2}$$

where n is the number of DFFs whose output is V_{DD}, the coarse and fine ramp output step V_{coarse} and V_{fine} is written as follows.

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011

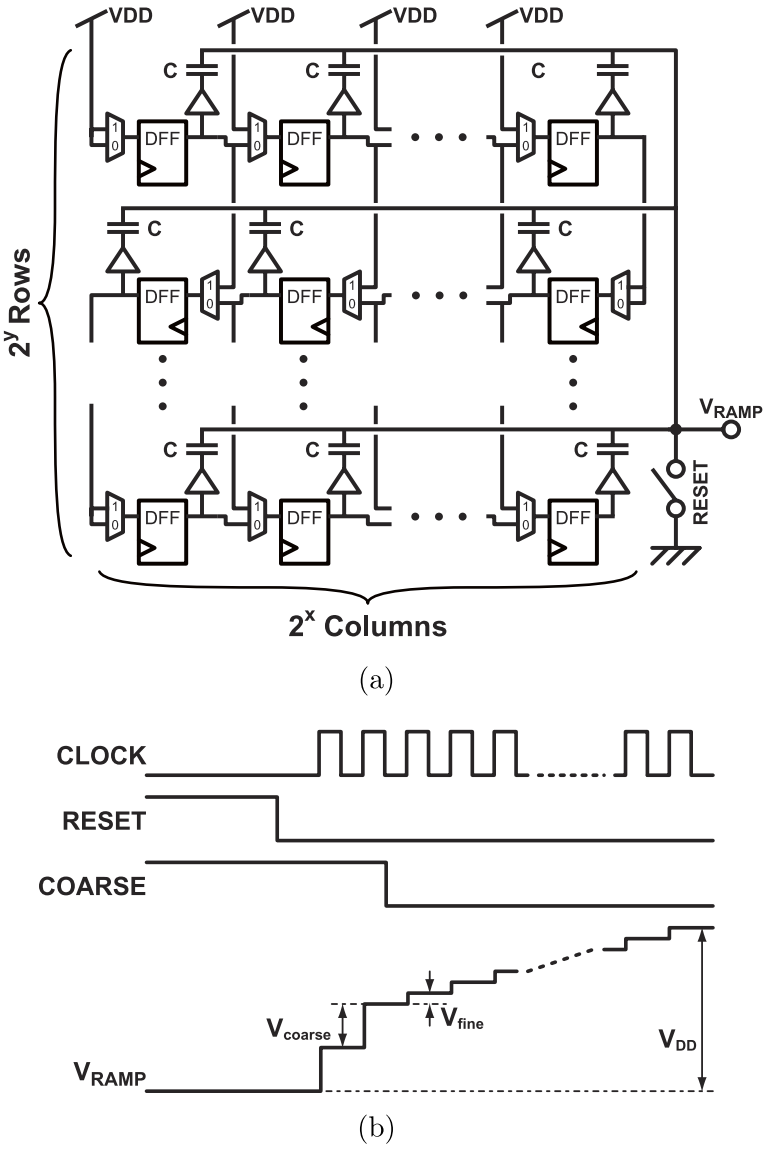


Fig. 1. (a) A schematic diagram and (b) a timing diagram of the proposed all-digital ramp waveform generator.

$$V_{coarse} = \frac{2^x}{2^N} V_{DD} = \frac{1}{2^y} V_{DD}, \tag{3}$$

$$V_{fine} = \frac{1}{2^N} V_{DD}. \tag{4}$$

Figure 1 (b) shows a timing diagram of the ramp waveform generation. During the reset state, the ramp output voltage is fixed to 0 V. Then, the RESET signal falls down to logic level 0 and the reset state is released. After the reset release, if the COARSE signal input is logic level 1, the "1" inputs of the selectors are used and the DFFs in the shift register block vertically shift the data. Thus, the V_{RAMP} voltage increases by V_{coarse} step according to the CLOCK input. After the COARSE signal falls down to logic level 0, the V_{RAMP} voltage increases by V_{fine} step until it reaches to V_{DD}. In the actual implementation, the final V_{RAMP} voltage is lower than V_{DD} due to the parasitic capacitance effects.

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011

3 Two-step single-slope ADC

A block diagram of the two-step single-slope ADC using the proposed all-digital ramp waveform generator is illustrated in Fig. 2 (a). Although the reset signal is abbreviated in this block diagram, all the DFF outputs in this

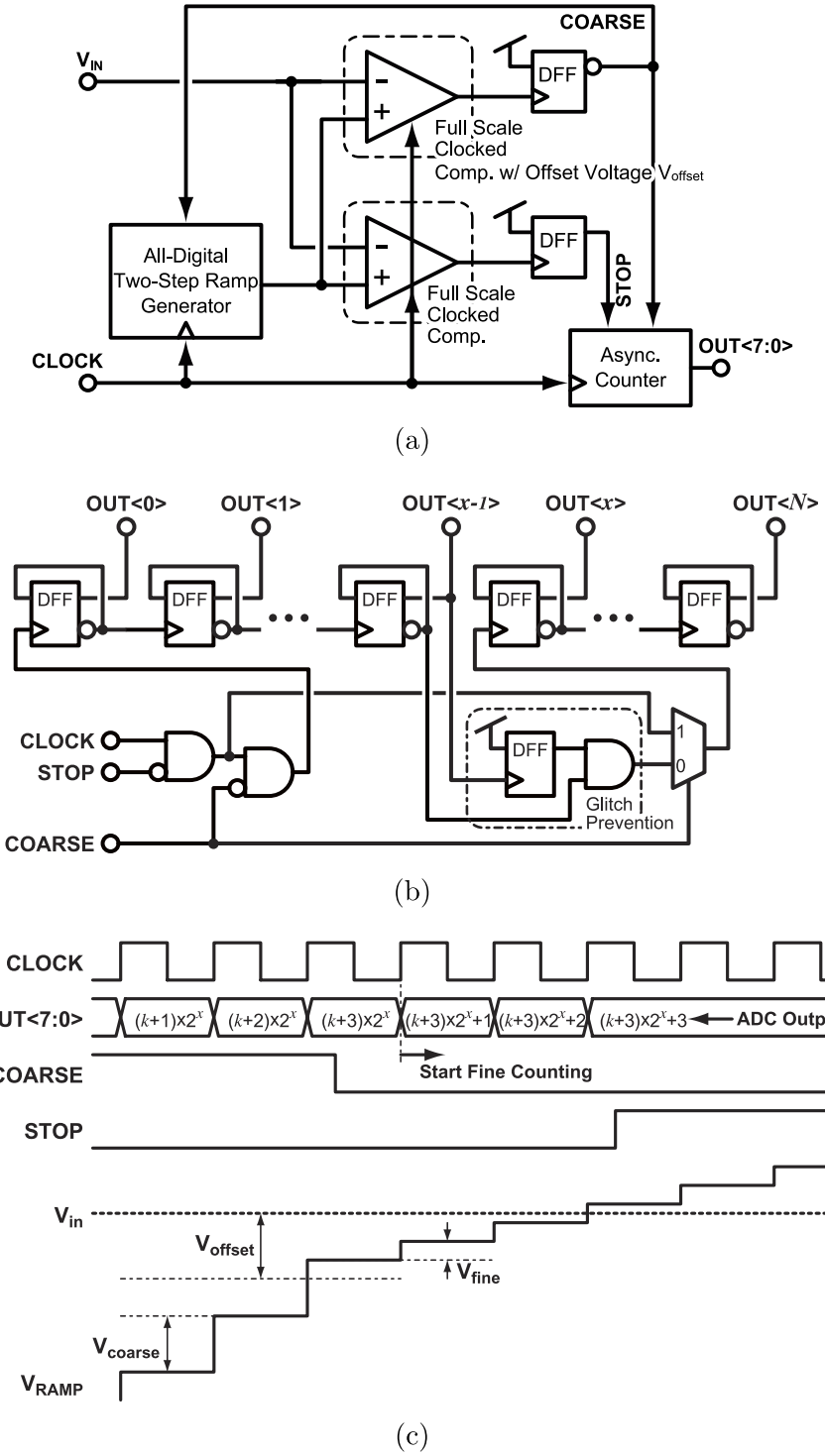


Fig. 2. (a) A block diagram of the 8-bit two-step single-slope ADC, (b) a N-bit asynchronous counter with coarse counting circuit and (c) a timing diagram of the two-step single-slope ADC.

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011

ADC are set to logic level 0 during reset state. Our single-slope ADC uses two full-scale comparators, one is to stop the counter for ADC output and the other is to switch the coarse-fine ramp waveform generation. We used low power and high speed rail-to-rail comparator proposed in [5] for these full-scale comparators. The comparator for coarse-fine switching has input offset voltage V_{offset} to stop the coarse ramp generation before the ramp output voltage reaches to the input voltage V_{in}. Therefore, the input offset voltage V_{offset} must be larger than the coarse step of the ramp waveform V_{coarse}. This input offset voltage is introduced by changing the W/L size of the differential input transistor pair.

During the coarse ramp waveform generation, the asynchronous counter has to count 2^x step by a single clock. Figure 2 (b) shows a block diagram of the N-bit asynchronous counter with coarse counting circuit. The input CLOCK signal is propagated directly to the x bit counting DFF during STOP signal is logic level 0 and COARSE signal is 1. Once COARSE signal falls down to logic level 0, the CLOCK signal is connected to 0 bit counting DFF. To prevent the unnecessary count during the COARSE signal transition, the glitch prevention circuit is inserted between $x-1$ and x bits DFFs. When STOP signal becomes 1, all the CLOCK distribution is disabled and this counter stops counting.

Figure 2 (c) illustrates the simplified timing diagram of the two-step single-slope ADC. As shown in this figure, the ramp waveform generator starts the ramp signal with coarse voltage step V_{coarse}. Once V_{RAMP} reaches to $V_{in} - V_{offset}$, COARSE signal falls down to logic level 0 due to the rise output from the comparator with input offset voltage. After the 0 to 1 transition of COARSE signal, the ramp waveform increases by V_{fine} step until it reaches to V_{in}. Then, STOP signal rises to 1 due to the rise output from the comparator without offset and counter stops.

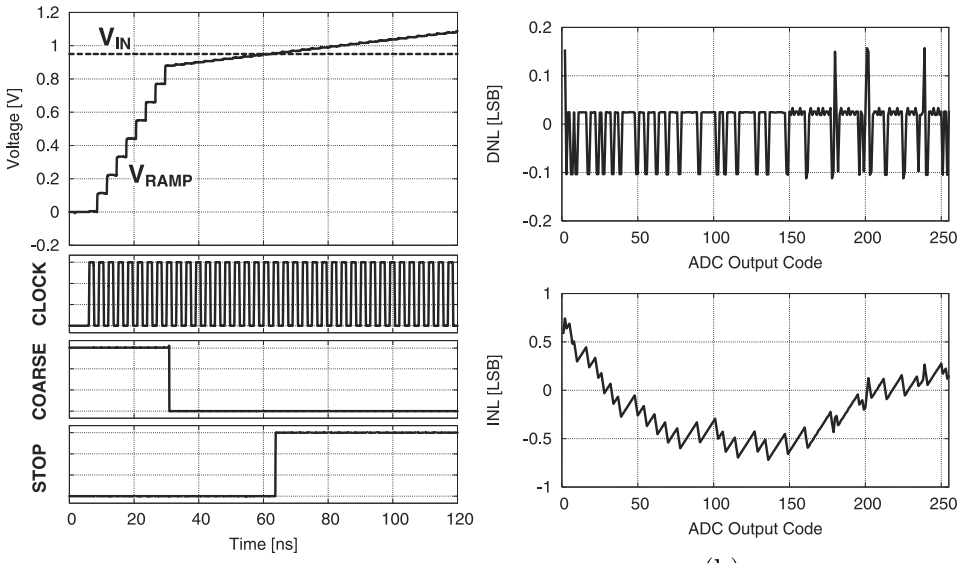
4 Experimental results

The proposed all-digital ramp waveform generator is implemented for an 8-bit two-step single-slope ADC using a 0.18 μm CMOS process. An estimated occupation area of the 8-bit two-step single-slope ADC is about 400 μm $\times$ 400 μm. In this implementation, the unit capacitance C is designed using 64 fF MIM (Metal-Insulator-Metal) capacitor. In the ramp waveform generator, the shift register is designed with 2^4 columns and 2^4 rows to implement the 8-bit ramp generator. Thus the coarse and fine steps of the ramp waveform are $V_{DD}/2^4$ and $V_{DD}/2^8$, respectively.

A simulated waveform of the ADC operation using 300 MHz clock signal is shown in Fig. 3 (a) and these waveforms show the correct operation of the two-step single-slope ADC as explained in Sect. 3. The simulation results show that 6 Msamples/s analog-to-digital conversion is realized by the implemented ADC in the slowest conversion case, whereas the sampling rate in the same case is about 1 Msamples/s without the two-step operation.

Figures 3 (b) shows the non-linearity plots of the 8-bit two-step single-

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011



(a) (b)

Fig. 3. (a) Simulated waveforms and (b) non-linearity plots of the 8-bit two-step single-slope ADC based on the proposed all-digital ramp waveform generator.

slope ADC with random capacitance variation of $3\sigma = 10\%$. As shown in these graphs, the simulated DNL and INL is within $\pm$0.2LSB and $\pm$0.8LSB, respectively. All these results show that the implemented 8-bit ADC guarantees monotonicity with two-step operation using quite simple structure with the cost of large area.

5 Summary

This paper presented an all-digital on-chip ramp waveform generator for an 8-bit two-step single-slope ADC. The proposed circuit realizes two step coarse-fine ramp waveform to speed up the single-slope analog-to-digital conversion. The experimental results of the circuit simulation on 0.18 μm CMOS process demonstrated the feasibility of our ramp waveform generator and 8-bit ADC with DNL within $\pm$0.2LSB and INL within $\pm$0.8LSB. Our future work includes the measurement and evaluation of the fabricated 8-bit two-step single-slope ADC.

Acknowledgments

This research project has been supported by STARC. The VLSI chip in this study has been designed in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

DOI: 10.1587/elex.8.20
Received October 26, 2010
Accepted November 29, 2010
Published January 10, 2011