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ADC jitter estimation using a single frequency test without requiring coherent sampling

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Abstract: An accurate and cost-effective method for ADC jitter estimation is proposed. The new method only requires a single high-frequency test. Eliminating the need for a 2nd low-frequency test in the conventional dual-frequency tests can significantly save both hardware and data acquisition time. Furthermore, the proposed method does not require the condition of coherent sampling and expensive instruments. Theoretical analysis, simulation and experimental results show that the proposed method is cost-effective and can achieve the test accuracy comparable to conventional dual-frequency tests.

Keywords: ADC, jitter, sine wave fitting, least square method

Classification: Integrated circuits

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1 Introduction

The jitter or aperture uncertainty in analog-to-digital converters (ADCs) is a random variation in the sampling instant [1]. This parameter is of special importance as the signal frequency and data rate increasingly get higher. In

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some applications, jitter has becomes the bottleneck of many systems performance. Current many jitter test methods are proposed in the literature [2, 3]. However, there are some problems in existing methods. Most of them require dual-frequency tests: a low frequency signal test and a high frequency signal test. Compared with a single frequency test, dual-frequency tests increase greatly the test time and test cost, consume large die area and hence are not suitable for being built on chip. Furthermore, these methods require coherent-sampling. However, achieving coherent sampling needs expensive frequency synthesizer and is a great challenge, and is impossible for high-performance ADC test and on-chip test [4]. Therefore, to reduce test cost and eliminate the need of coherent-sampling, it is necessary to develop some new jitter test methods.

In this letter, an accurate and cost-effective method for measuring random jitter is proposed, which requires only a single high frequency test and does not require coherent sampling. Compared with the conventional dual-frequency tests, the new method cut the test time by 1/2. Furthermore, the proposed method does not fulfill the condition of coherent sampling, and hence only requires cheaper instruments. In addition, the proposed method offers the potential solution for on-chip jitter test.

2 Conventional dual-frequency jitter tests

Most of the existing methods for ADC jitter estimation require the following dual-frequency tests and two SNR (Signal-to-Noise Ratio) measurements [3]. The SNR_L and SNR_H can be obtained by measuring SNR at a low frequency signal and a high frequency signal, respectively. Based on the degradation in SNR at high frequencies, the root-mean-square (RMS) jitter $\sigma_{\delta t}$ is calculated as follow

$$\sigma_{\delta t} = \frac{1}{2\pi f}\sqrt{\left(\frac{1}{10^{SNR_H/20}}\right)^2 - \left(\frac{1}{10^{SNR_L/20}}\right)^2} \tag{1}$$

where f is the frequency of the high frequency input signal. Furthermore, in the FFT (Fast Fourier Transform) test routine for measuring SNR, coherent sampling is commonly required in order to prevent the spectral leakage.

3 Single-frequency jitter test without requiring coherent sampling

A single-frequency jitter test method without requiring coherent sampling is derived by theoretical analysis, and then realized by a 7-step procedure.

Let $V_{in}(t)$ denote the input signal of an ADC. The output of the ADC is a sequence of samples x_n which has the length of M and is given by

$$x_n = V_{in}(nT_s+\delta t_n)+V_{hd}(nT_s)+V_{noise}(nT_s)+V_q(nT_s), \mathrm{n} = 0, 1, 2, 3, ..., \mathrm{M}-1 \tag{2}$$

where T_s represents the ideal sampling period for the ADC. δt_n is a random time variable which represents the ADC jitter, and is distributed normally with zero mean and variance $\sigma_{\delta t}^2$. $V_{hd}(nT_s)$ represents the harmonic distortion

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components and their magnitudes are small, generally on the order of a LSB (least significant bit). $V_{noise}(nT_s)$ represents the additive measurement noise. $V_q(nT_s)$ represents quantization noise of ADC. The goal of this letter is to find a simple method to estimate the standard deviation of δt_n, viz. the RMS jitter $\sigma_{\delta t}$.

According to Taylor formula, (2) can be easily converted to

$$x_n \approx V_{in}(nT_s) + \frac{dV_{in}}{dt}\delta t_n + V_{hd}(nT_s) + V_w(nT_s) \tag{3}$$

where $V_w(nT_s) = V_{noise}(nT_s) + V_q(nT_s)$. Equation (3) indicates that the jitter δt_n is modulated by the slope of the input signal when it is converted to noise. In this letter, we will take advantage of this result.

For sine wave input,

$$V_{in}(t) = C + A\sin(2\pi ft + \varphi) \tag{4}$$

where C, A, f and φ are offset, amplitude, frequency and initial phase of sine wave, respectively. The slope of the input signal is given by

$$\frac{dV_{in}}{dt} = 2\pi fA\cos(2\pi ft + \varphi) \tag{5}$$

In (3), substituting $V_{in}(t)$ and $\frac{dV_{in}}{dt}$ with (4) and (5) gives

$$x_n \approx C + A\sin(2\pi fnT_s + \varphi) + 2\pi fA\cos(2\pi fnT_s + \varphi)\delta t_n + V_{hd}(nT_s) + V_w(nT_s) \tag{6}$$

Suppose the fundamental component can be identified and removed from the raw data x_n, then we can get the error sequence e_n, as shown in (7), no matter whether the condition of coherent sampling is satisfied.

$$e_n \approx x_n - \hat{C} - \hat{A}\sin(2\pi\hat{f}nT_s + \hat{\varphi}) \tag{7}$$

where $\hat{C}$, $\hat{A}$, $\hat{f}$ and $\hat{\varphi}$ are the estimated values of C, A, f, φ, respectively. In (7), substituting x_n with (6) gives

$$e_n \approx 2\pi\hat{f}\hat{A}\cos(2\pi\hat{f}nT_s + \hat{\varphi})\delta t_n + V_{hd}(nT_s) + V_w(nT_s) \tag{8}$$

Equation (8) indicates that e_n is a function of jitter δt_n. Let θ be the identified fundamental's phase

$$\theta = 2\pi\hat{f}nT_s + \hat{\varphi} \tag{9}$$

In order to realize jitter estimation under a single frequency test, we split θ into two parts: the zero-crossing parts $\{\theta_H\}$ and full-scale parts $\{\theta_L\}$.

$$\{\theta_H\} = \{\theta | -\frac{\pi}{4} + i\pi \le \theta \le \frac{\pi}{4} + i\pi, i = 0, \pm1, \pm2, \pm3, ...\} \tag{10}$$

$$\{\theta_L\} = \{\theta | \frac{\pi}{4} + i\pi < \theta < \frac{3\pi}{4} + i\pi, i = 0, \pm1, \pm2, \pm3, ...\} \tag{11}$$

Note that $\{\theta_H\}$ and $\{\theta_L\}$ are two sets with the same length M/2. Accordingly, $\{e_n\}$ is sorted into two sets $\{e_{Hn}\}$ and $\{e_{Ln}\}$ with the same length M/2 according to the identified fundamental's phase.

$$e_{Hn} \approx 2\pi\hat{f}\hat{A}\cos(\theta_H)\delta t_n + V_{hd}(nT_s) + V_w(nT_s) \tag{12}$$

$$e_{Ln} \approx 2\pi\hat{f}\hat{A}\cos(\theta_L)\delta t_n + V_{hd}(nT_s) + V_w(nT_s) \tag{13}$$

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Note that $|\cos\theta_H| \geq \frac{1}{\sqrt{2}}$ for all e_n in $\{e_{Hn}\}$, and $|\cos\theta_L| < \frac{1}{\sqrt{2}}$ for all e_n in $\{e_{Ln}\}$. This shows that the contribution to noise due to jitter in the zero-crossing parts is larger than that in full-scale parts. Fig. 1 illustrates that $\{e_n\}$ is sorted into $\{e_{Hn}\}$ and $\{e_{Ln}\}$ according to the identified fundamental's phase. Fig. 1 (a) shows a 9-bit ADC output codes in time domain. Fig. 1(b) shows that $\{e_n\}$ is sorted into two distinct sets $\{e_{Hn}\}$ and $\{e_{Ln}\}$. Obviously, e_{Hn} is larger than e_{Ln} in magnitudes. In fact, the power of e_{Hn} and e_{Ln} can be derived as follows.

$$P_{e_H} = \left(2\pi\hat{f}\,\hat{A}\right)^2 \left(\frac{1}{2} + \frac{1}{\pi}\right)\sigma_{\delta t}^2 + \sigma_{hd}^2 + \sigma_w^2 \tag{14}$$

$$P_{e_L} = \left(2\pi\hat{f}\,\hat{A}\right)^2 \left(\frac{1}{2} - \frac{1}{\pi}\right)\sigma_{\delta t}^2 + \sigma_{hd}^2 + \sigma_w^2 \tag{15}$$

where $\sigma_{\delta_t}^2$ is the variance of jitter δt_n, σ_{hd}^2 and σ_w^2 are the power of harmonics noise and quantization noise, respectively. Obviously, P_{e_H} is larger than P_{e_L}. Furthermore, P_{e_H} and P_{e_L} can be easily obtained by computing the variance of $\{e_{Hn}\}$ and $\{e_{Ln}\}$, respectively.

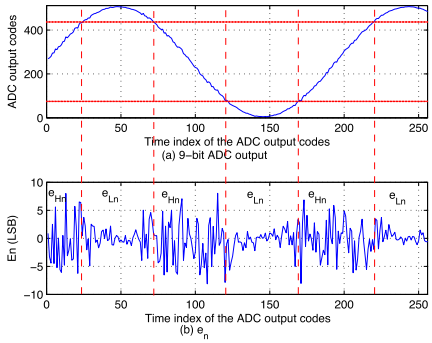

Fig. 1. $\{e_n\}$ sorted into $\{e_{Hn}\}$ and $\{e_{Ln}\}$.

Combining (14) and (15), we can get the RMS jitter

$$\sigma_{\delta t} = \sqrt{\frac{P_{e_H} - P_{e_L}}{8\pi(\hat{f}\hat{A})^2}} \tag{16}$$

Therefore, as long as the fundamental can be identified with reasonable accuracy, then the RMS jitter can be estimated with only a single frequency test. To make the effects of aperture jitter on the noise floor more noticeable, the frequency of sampling clock should be set for the maximum allowable, and the frequency of input signal should be high enough, even it can be greater than Nyquist frequency. Furthermore, in order to make the proposed method have the capability of processing non-coherent data, we use the four-parameter sine wave fitting algorithm [1] to identify the fundamental. The procedures of the proposed method are outlined in the following seven steps.

1. Collect M (even) samples x_n from output for the given input and clock signals (without requiring coherent sampling).

2. Perform FFT, and estimate f by the three-sample interpolated FFT technique [5].

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3. Identify C, A and φ by the least square method.

4. Subtract the identified fundamental from x_n to obtain the error sequence e_n.

5. Sort e_n into two sets (e_{Hn} and e_{Ln}) with the same length M/2 by using the identified fundamental's phase.

6. Compute P_{e_H} and P_{e_L}, respectively.

7. Compute RMS jitter by using (16).

In the proposed method, only a high frequency test is performed and additional instruments are not required. Elimination of the need for a 2nd low-frequency test significantly saves both hardware and data acquisition time. Furthermore, coherent sampling is not required, and hence the test only requires cheaper instruments. Therefore, the proposed method is cost-effective.

4 Simulation results

In order to validate the accuracy of the estimation method, some simulations are performed, in which some known values of jitter are added. In the simulation, the output of ADC is simulated as a set of transition levels. Its nonlinearity error is chosen to be a Gaussian random variable with zero mean and standard deviation σ_{DNL}. The input of ADC is a pure high frequency sine wave whose amplitude is set for 96% of the full scale range (FSR) in ADC. Additive measurement noise (such as thermal noise) is introduced at the input node of ADC. The noise is normally distributed with zero mean and standard deviation σ_{noise}=0.25 LSB. The jitter is a random error added to the ideal sampling time instants, and is distributed normally with zero mean and a known standard deviation $\sigma_{\delta t}$.

Table I summarizes the estimated RMS jitter by the proposed method under different conditions. In Table I, N represents the resolution of ADC, f_{clk} is the frequency of sampling clock, f_{sig} is the frequency of input sine wave. In each case, the collected data record length is 16384. And the data are non-coherent, namely, each data record does not comprise exactly an integer number of input signal periods. As expected, from Table I we can obtain that the estimated values of RMS jitter are close to the ideal values, the maximum relative error is in ±1.7%, and the errors are acceptable.

Table I. Estimated RMS jitter under different conditions

N /bit	σ_{DNL} /LSB	f_{clk} /MHz	f_{sig} /MHz	Ideal $\sigma_{\delta t}$ /ps	Estimated $\sigma_{\delta t}$ /ps	Relative error
9	0.07	1000	494.207764	5	5.085	1.7%
9[a]	0.07[a]	1000[a]	994.946289[a]	2[a]	2.008	0.4%
12	0.02	400	196.809082	2.5	2.497	−0.12%
14	0.008	200	98.404541	1	0.984	−1.6%

[a]*:The test condition of Fig. 1.*

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5 Experimental results

The estimation method is implemented on a commercial 9-bit ADC sampling at 400 MS/s. The frequency of input signal is about 399 MHz. The collected output data are non-coherent and their length is 8190. According to the procedures in section 2, the fundamental is first identified by four-parameter sine wave fitting algorithm. $\{e_n\}$ is then obtained by removing the identified fundamental from raw data. Finally $\{e_n\}$ is sorted into two sets $\{e_{Hn}\}$ and $\{e_{Ln}\}$ with the same length of 4095 according to the fundamental's phase. Fig. 2 (a) and Fig. 2 (b) illustrate the spectra of e_{Hn} and e_{Ln}, respectively. Fig. 2 shows that e_{Hn} is larger than e_{Ln} in magnitudes. In fact, the computed P_{e_H} and P_{e_L} are 6.432824×10^{-6} and 5.612734×10^{-6}, respectively (these values are relative to FSR, here FSR=2). As the amplitude and frequency of the identified fundamental are 0.9442 and 398.974609 MHz, respectively. So, according to (16), the estimated RMS jitter by the proposed method is 0.479 ps.

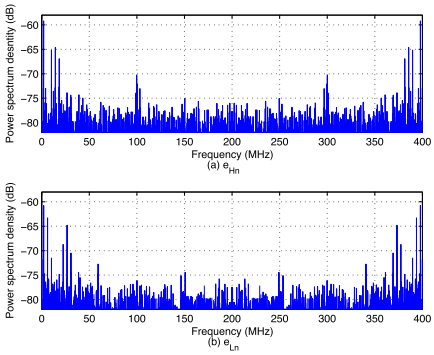

Fig. 2. The spectra of e_{Hn} and e_{Ln}

To compare the results between the proposed method and the dual-frequency test [3], an extra low frequency test is also implemented, in which the frequency of input signal is about 2 MHz. The measured SNR_L is 50.3648 dB. In fact, in previous high-frequency test, the non-coherent data are obtained by discarding the last two samples of a coherent data whose length is 8192. The measured SNR_H is 49.8292 dB by performing FFT spectral analysis on the coherent data. Finally, according to (1), the estimated RMS jitter of the dual-frequency test is 0.480 ps, which has only 0.001 ps difference with the proposed method. This shows that the proposed method can achieve the accuracy comparable to the dual-frequency test.

6 Conclusion

A cost-effective method for random jitter estimation is proposed. The proposed method only requires a high frequency test. Compared with the conventional dual-frequency test, the proposed method cuts the test time by 1/2. Furthermore, coherent sampling is not required, and hence the test only need cheaper instruments. The simulation results show that the relative er-

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rors between the estimated jitter and the ideal jitter are within ±1.7%. The experimental results show that the proposed method can achieve accuracy comparable to conventional dual-frequency test.

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