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Comparative study of the static and switching characteristics of SiC and Si MOSFETs

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Abstract: SiC power devices with low loss and fast switching capability have been developing. This study experimentally characterizes trench gate and planar gate SiC MOSFETs, and discusses the difference to conventional Si MOSFET in terms of static and dynamic performance. First, the static current–voltage (I–V) characteristics are evaluated to assess conduction loss. Next, the bias voltage dependencies of terminal capacitance (C–V) are characterized to clarify differences stemming from device configuration. Turn-off switchings for non-inductive resistive loads are examined, and the result are evaluated by associating measured C–V characteristics.

Keywords: SiC MOSFET, I–V characteristics, C–V characteristics, conduction loss, fast switching

Classification: Electron devices, circuits, and systems

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1 Introduction

Power conversion circuits that are operated at high voltages achieve efficient energy usage, and the high frequency switching improves the functionality and miniaturization of power conversion systems. SiC power semiconductor devices have been developing to meet these requirements. It is known that a SiC Schottky barrier diode substantially reduces switching losses during fast turn-off operations by eliminating the reverse recovery phenomenon, which is unavoidable with conventional high-voltage Si PiN diodes [1, 2, 3]. A controllable switching device is also expected to have fast switching capability with low power loss. This study experimentally evaluates the operating performance of trench gate (TMOS) and planar gate (DMOS) SiC MOSFETs and compares them with a conventional Si power MOSFET (SiMOS) with equivalent rated voltage and current density. To this end, static current-voltage (I–V) characteristics are first measured and the conduction losses are evaluated. Then, the bias voltage dependency of the terminal capacitance (C–V), which governs the switching behavior of a unipolar device, is characterized. The turn-off switching operation is tested and evaluated by associating the measured static characteristics. Finally, the authors discuss suitable usage of SiC MOSFETs in state of the art for power conversion.

2 Static characteristics

SiC MOSFETs (TMOS, DMOS) used in this experiment are developed by the authors; SiC DMOS is a commercial sample (SiC DMOS 1st generation, 600 V, 5 A, ROHM), and the SiC TMOS is a design sample (cell pitch 6 μm, channel length 0.4 μm, drift layer 7 μm with impurity concentration $7.5 \times 10^{15}\mathrm{cm}^{-3}$). Si MOSFET used for comparison is a commercially available device (R6006ANX, 600 V, 6 A, ROHM). The chip sizes for TMOS, DMOS, and SiMOS are 1.2 mm × 2.4 mm, 2.0 mm × 1.85 mm, and 2.56 mm × 2.63 mm, respectively. The characteristics of MOSFETs are evaluated with the values for per unit area in the followings.

2.1 I–V characteristics

Figure 1 shows the measured I–V characteristics. The forward and reverse conduction characteristics are shown in Fig. 1 (a). A 20 V gate voltage (V_{gs}) is applied to conduct the MOSFET. The conduction resistance (R_{on}) at $I_{\mathrm{ds}} = 100\,\mathrm{A/cm}^2$ is 0.00551, 0.0182 and 0.0915 $\Omega\mathrm{cm}^2$ for TMOS, DMOS, and SiMOS, respectively. TMOS has the least R_{on} per unit area, which deserves 1/3 for DMOS and 1/16 for SiMOS.

The reverse current flows through the body diode when V_{gs} is 0 V. The series resistances of body diodes are 0.00272, 0.00625 and 0.00112 $\Omega\mathrm{cm}^2$, respectively for TMOS, DMOS and SiMOS, whose magnitude relations differ to the forward conduction resistance. The knee voltage of body diodes are −1.18, −1.64 and −0.59 V (at $I_{\mathrm{ds}} = -100\,\mathrm{mA/cm}^2$) respectively for TMOS, DMOS and SiMOS. The extracted diode factors are n = 3.03, 5.40 and 1.14, respectively for TMOS, DMOS and SiMOS. The body diode of SiMOS

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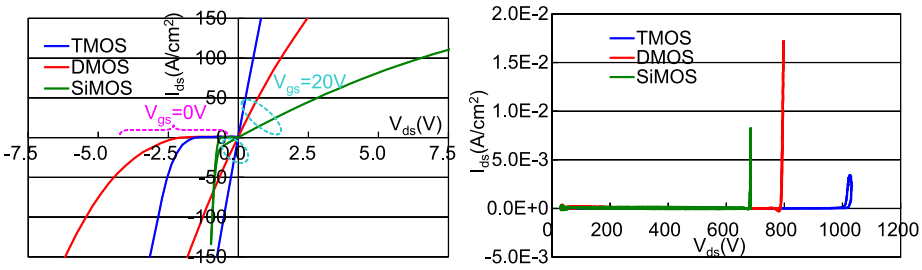
works as a typical diode with $n \approx 1$. However, the characteristics of body diodes for SiC DMOS and TMOS are far from ideal diode as shown in the extracted diode coefficients $n > 2$. The high series resistances of body diode for SiC MOSFETs denote the shortage of conductivity modulation by minority carrier (hole) injection to drift region. These characteristics present the insufficient activation of doped impurities in SiC semiconductor.

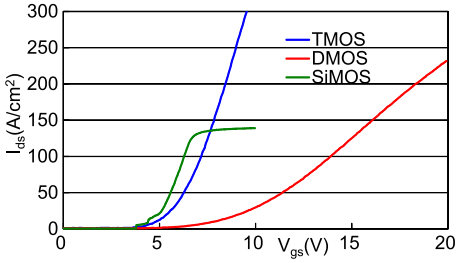
Reverse current also flows through the MOSFET channel for $V_{gs} = 20\,\mathrm{V}$. The series resistance in this condition corresponds to R_{on} in the forward conduction. Though the body diode current of SiMOS dominates the reverse direction current for $I_{ds} < -20\,\mathrm{A/cm^2}$, but SiC TMOS and DMOS give less voltage drop and conduction loss in reverse conduction with conducting the channel by synchronous rectification operation.

The leakage current in forward blocking condition ($V_{gs} = 0\,\mathrm{V}$) is shown in Fig. 1 (b). The breakdown voltages are 1020, 789, and 680 V for TMOS, DMOS, and SiMOS, respectively.

Figure 1 (c) shows the forward transfer admittance (V_{gs}–I_{ds}) characteristics with respect to a constant drain voltage. The extracted threshold gate voltages are 3.89, 5.00, and 3.72 V for TMOS, DMOS, and SiMOS, respectively, and the forward transfer admittances are 65.8, 22.5, and 78.5 $\mathrm{S/cm^2}$ (at $I_{ds} = 100\,\mathrm{A/cm^2}$), respectively. Thus, SiMOS has the highest voltage gain, and TMOS and DMOS respectively provide voltage gains of 84% and 29% to SiMOS. SiC MOSFETs does not show current saturation for V_{gs} up to 20 V, which means gradual generation of inversion layer under the gate. The value of V_{gs} required for conducting TMOS is less than that for DMOS, and the R_{on} drops considerably for $V_{gs} = 10\,\mathrm{V}$.



(a) Forward and reverse conduction. (b) Leakage current in forward blocking.



(c) Forward transfer admittance.

Fig. 1. Static I–V characteristics of trench gate (TMOS), planar gate (DMOS) SiC MOSFETs, and Si MOSFET (SiMOS).

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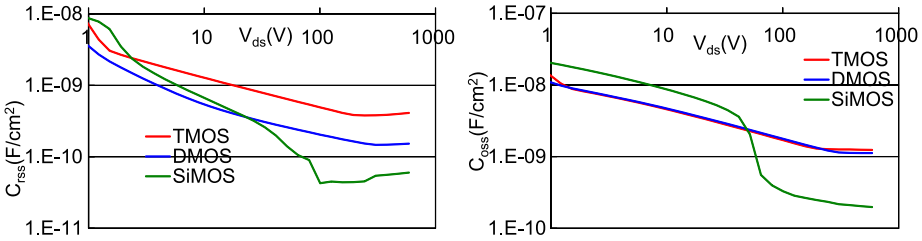
2.2 C–V characteristics

The terminal capacitance of a MOSFET affects the switching behavior. The bias voltage dependency in reverse transfer capacitance ($C_{\rm rss}$), input capacitance ($C_{\rm iss}$), and output capacitance ($C_{\rm oss}$) are measured [4, 5] and evaluated here.

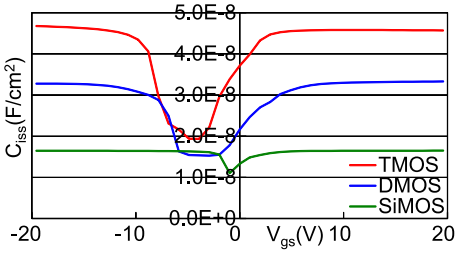
$C_{\rm rss}$ leads to the Miller effect [6] in on-off transitions during the switching operation. Fig. 2 (a) shows the $C_{\rm rss}$–$V_{\rm ds}$ characteristics. The $C_{\rm rss}$ of TMOS, DMOS, and SiMOS is 7.43, 3.64, and 8.76 nF/cm^2, respectively, at $V_{\rm ds} = 1$ V. SiMOS has the largest $C_{\rm rss}$ for a low bias voltage. However, impurity concentration for the drift region of SiMOS is low to attain high breakdown voltage with depleting the long depth at the expense of $R_{\rm on}$. Then, the $C_{\rm rss}$ of SiMOS changes substantially with the applied bias voltage and becomes less than that of TMOS and DMOS. In TMOS, the gate is along the vertical direction, and the distance between the bottom of the gate and drain electrodes is shorter than that in DMOS. Thus, TMOS has larger $C_{\rm rss}$ owing to the structure.

$C_{\rm oss}$ in Fig. 2 (b) affects the switching behavior, especially the turn-off operation, for it must be discharged with a load current to deplete the drift region and block the drain voltage. SiMOS has the largest $C_{\rm oss}$ for low $V_{\rm ds}$, but similar to its $C_{\rm rss}$, its $C_{\rm oss}$ changes significantly with applied $V_{\rm ds}$. The $C_{\rm oss}$ of SiMOS becomes lower than that of TMOS and DMOS for $V_{\rm ds} > 70$ V, resulting in lower sweep-out charge and fast buildup of $V_{\rm ds}$ for high voltages ($V_{\rm ds} > 70$ V). TMOS and DMOS gives approximately the same $C_{\rm oss}$ and analogus turn-off behavior is expected.

Figure 2 (c) shows the gate bias voltage ($V_{\rm gs}$) dependency of $C_{\rm iss}$, which governs the gate driving response. TMOS and DMOS respectively have 3 and 2 times larger $C_{\rm iss}$ than SiMOS, which gives adverse effect in fast gate driving. The formation of accumulation, depletion, and inversion layer in the



(a) $C_{\rm rss}$-$V_{\rm ds}$. (b) $C_{\rm oss}$-$V_{\rm ds}$.



(c) $C_{\rm iss}$-$V_{\rm gs}$.

Fig. 2. C–V characteristics of MOSFETs.

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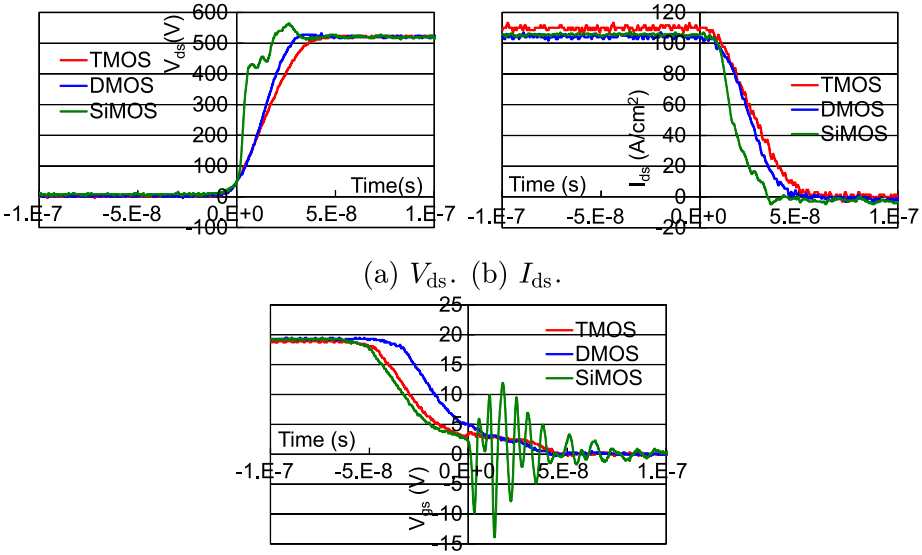
channel in accordance with the applied V_{gs} is clearly observed as capacitance change. The depletion layer is formed in the channel in the region of $-9\,\mathrm{V} < V_{gs} < 6\,\mathrm{V}$, $-13\,\mathrm{V} < V_{gs} < 3\,\mathrm{V}$, and $-2\,\mathrm{V} < V_{gs} < 3\,\mathrm{V}$ for TMOS, DMOS, and SiMOS, respectively. The gradual formation of the inversion layers in the channels of SiC MOSFETs with the applied V_{gs} are observed.

3 Switching characteristics

The turn-off operation of MOSFETs for a non-inductive resistive load for the same conducting current density is evaluated experimentally as switching characteristics. A 500 V power supply voltage provides a drain current $I_{ds} = 100\,\mathrm{A/cm^2}$. The MOSFETs are driven by 20–0 V gate voltages through gate resistance $R_g = 10\,\Omega$.

Figure 3 shows the results. The origin of the time response ($t = 0$) is aligned with the moment the drain voltage increases to 10% of the power supply voltage ($V_{ds} = 50\,\mathrm{V}$). The behavior of V_{ds} for $t < 0$ corresponds to the respective device, where C_{oss} is large with low bias voltage. I_{ds} behaves in approximately the same manner during this period. C_{oss} of SiMOS in Fig. 2 (b) substantially decreases as V_{ds} increases above 50 V; V_{ds} increases steeply for $t > 0$ and I_{ds} decreases rapidly, as shown in Fig. 3 (b). C_{oss} of TMOS and DMOS changes similarly and smoothly with V_{ds} in Fig. 2 (b), and then V_{ds} increases gradually and shows slower build up than that of SiMOS as shown in Fig. 3 (a), which stems from larger C_{oss} than SiMOS in the high voltage region. The rise times for V_{ds} to increase from 10% to 90% of the supply voltage are 29.3, 23.4, and 12.2 ns for TMOS, DMOS, and SiMOS, respectively. The fall time of the drain current shows the similar response.

Figure 3 (c) shows the response of the gate voltage. The delay times between the instant V_{gs} reaches 90% of the supply voltage and $t = 0$ are 49.7,



(a) V_{ds}. (b) I_{ds}.

(c) V_{gs}.

Fig. 3. Time response of MOSFETs in turn-off switching operation.

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34.1, and 50.5 ns for TMOS, DMOS, and SiMOS, respectively. The delay time is governed by C_{iss} and gate voltage of the device, where MOSFET begins to operate in the saturation region.

The turn-off time consists of the delay time and the rise time. The turn-off times are 79.0, 77.5, and 62.7 ns for TMOS, DMOS, and SiMOS, respectively. SiMOS provides the fastest turn off capability for the same current density, though it has largest conduction loss. V_{gs} oscillates for $t > 0$ in SiMOS, which results from interaction between the terminal capacitance and parasitic wiring inductance, high voltage gain, and excitation with large dV_{ds}/dt accompanied by fast turn-off. Thus, SiMOS requires a larger gate resistance to avoid gate-driving malfunction. Miller effect durations of 50 and 25 ns are observed for TMOS and DMOS, respectively, because of the large C_{rss} for high drain voltage ($V_{ds} > 50$ V), which reduces switching speed.

The experimental results elucidated that switching operations of SiC MOSFETs in state of the art are not necessarily faster than conventional Si MOSFET with the same device area. This can be attributed to the larger output capacitances of SiC MOSFETs than Si MOSFET, which stems from higher critical breakdown electric field of SiC semiconductor and higher doping concentration in drift region to achieve low on resistance. Therefore, it is advisable to utilize SiC MOSFETs as a low conduction loss power switch and not to raise the switching frequency higher than conventional Si MOSFET.

4 Conclusion

This paper experimentally evaluated and compared the static I–V, C–V, and dynamic switching characteristics of TMOS, DMOS, and SiMOS.

The I–V characteristics reveal that SiC MOSFETs provide the considerable reduction in conduction loss, and the trench gate structure gives the lowest R_{on} for per unit area of the device. However, synchronous rectifications are required for SiC MOSFETs to reduce the conduction loss in flowing reverse current because of the high voltage drop in body diode.

The C–V characteristics showed that the SiMOS terminal capacitance changes significantly with the applied drain voltage. SiMOS shows larger capacitance than SiC devices at low voltage, but the capacitance becomes small at high voltages, which assists fast turn-off operation. Though, Si MOSFET provides fastest turn-off for same current density operation, but the conduction loss is considerably large. SiC MOSFETs realize low conduction loss, therefore further development in managing terminal capacitance is required to realize superior power conversion system with fast switching operation.

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