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Fully parallel comparator for the moduli set $\{2^n, 2^n-1, 2^n+1\}$

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Abstract: A novel circuit based on sign detection is introduced in this paper which uses the subtraction for comparing two numbers without carrying out a full comparison and conversion. Thus, the proposed schema decreases the delay significantly using only a little redundant hardware in contrast to previous works. Also the time complexity of the new design has the best results comparing to the previous work.

Keywords: residue number system, reverse converter, binary comparator

Classification: Integrated circuits

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1 Introduction

RNS is a collection of positive integers named a module and a set of modules which are called a module set [1]. In this system any integer number X can be represented as the vector of its residue module, such as $X = \{x_1, x_2, \ldots, x_n\}$, while x_i denotes operation X mod m_i.

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The system will have the largest possible dynamic range if all modules are relatively pair wise primes. The dynamic range of a module set is called M and is expressed as Eq. (1).

$$M = \Pi^{n}_{i=1}(m_i) \tag{1}$$

Each binary operation between two integers (X, Y) in range M is defined as Eq. (2).

$$X \circ Y = (x_1 \circ y_1 \bmod m_1, x_2 \circ y_2 \bmod m_2, \ldots, x_n \circ y_n \bmod m_n) \tag{2}$$

It is evident that such operations are performed in "residue-parallel" in modulo m_i.

In non-weighted number systems such as RNS, all operations are performed independently on each residue [1]. It is the result of non-weighted system; however the comparison is more difficult because of this nature, so it cannot use widely in some applications.

To compare the numbers in $\{2^n, 2^n - 1, 2^n + 1\}$ module set some works have been done previous some of which uses mixed radix. Thus they force to use the CRT [2], but CRT requires complex calculations that are not efficient [3]. It is known that one of the simplest ways to compare two numbers in a weighted system is subtraction. In this paper a novel circuit is introduced using sign detection instead of comparing two numbers. So that it decreases the delay using a little hardware by leading less time complexity in comparison with the previous work [3].

2 Comparing by subtracting

The most common way to compare two numbers is by subtraction. But because subtraction uses a borrowed digit, it is sometimes difficult to implement in a hardware circuit. Thus in this paper we commute the subtraction to the addition as Eq. (3)

$$A - B = A + (B)^{/} + 1 \tag{3}$$

3 Reverse convertor

As discussed before, RNS is a non-weighted number system therefore the comparison is more difficult in this system. Thus, in the novel method, only some stages of a convertor are used to convert remainders to a binary representation which is introduced in [4].

Let the three residues be denoted as (X_1, X_2, X_3) and the module set as ($2^n - 1$, 2^n, $2^n + 1$). The binary value of X can be computed according to Eq. (4).

$$X = |A + B + C + |-X_3||_{2^{2n}-1} \times 2^n + x_2 \tag{4}$$

Where the variables are defined as below:

$$A = (x_{10}x_{1n-1}\ldots x_{11}x_{10}x_{1n-1}\ldots x_{11}) \tag{5}$$

$$B = (\overline{X}_{2n-1}\overline{X}_{2n-2}\ldots\overline{X}_{21}\overline{X}_{20}\underbrace{11\ldots1}_{n}) \tag{6}$$

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$$C = (b_0 x_{3n-1} \dots x_{31} b_0 x_{3n-1} \dots x_{31}), b_0 = x_{3n} \oplus x_{30} \quad (7)$$

Where $\oplus$ denotes XOR.

$$|-X_3|_{2^{2n}-1} = (\underbrace{11\dots1}_{n-1} \overline{X}_{3n} \overline{X}_{3n-1} \dots \overline{X}_{31} \overline{X}_{30}) \quad (8)$$

4 Novel RNS comparison schema

One of the fundamental operations in numeric systems is comparison but it is hardly implemented in non-weighted number systems such as RNS. A novel

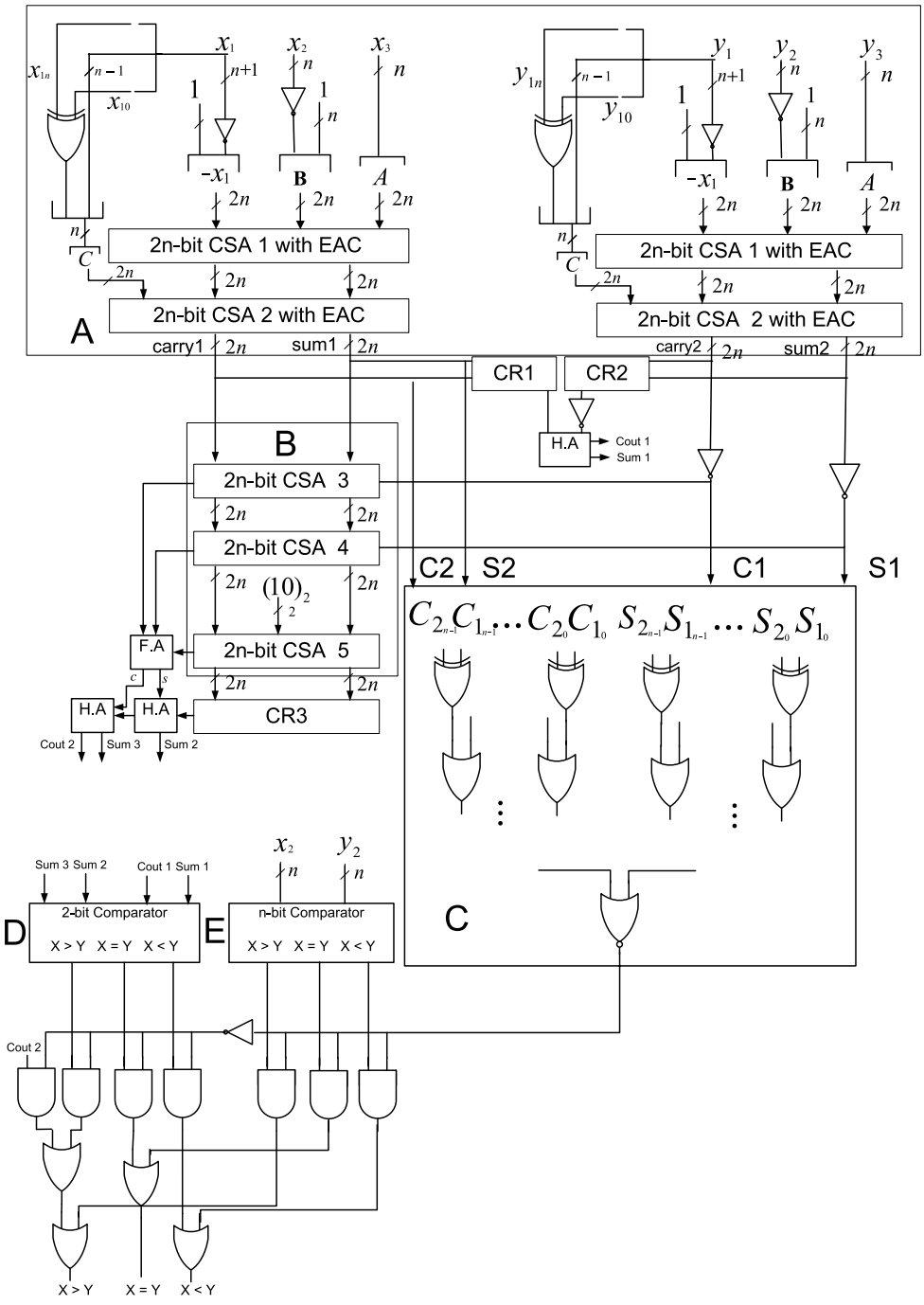

Fig. 1. The Proposed Comparator Circuit.

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circuit is proposed in this paper to compare numbers in residue presentation without using a complete convertor, or redundant modules or even look-up table and also using the sign detection instead of comparison.

The main idea of this circuit (See figure 1) is doing the work in three steps

1- Some stages of backward convertor to convert the numbers to suitable system (See A in figure 1).

2- Subtraction (See B in figure 1)

3- Signs detection (That works on the result of CR1, CR2 and CR3).

The first two blocks are used to convert residues to binary. Then after the resulting numbers are used as input of the CR1 and CR2 circuit to detect the carry digit as shown in figure 2. Next cout1 and sum1 obtained by adding CR1 and CR2 that should be compared to Sum3, Sum2 as shown in figure 1.

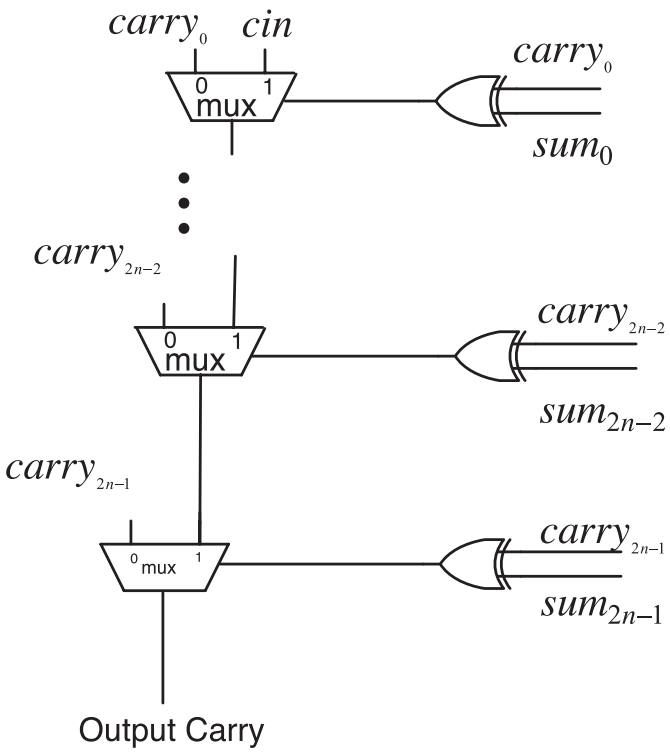

Fig. 2. The Carry Recognizer Circuit.

At the same time, the C2S2 and C1S1 are used as input for C (see figure 1) to check whether they are equal or not. At By the following Eq. (3) the first numbers (Carry1, sum1) should be added with the 2's complement of the second numbers (carry2, sum2). To calculate the 1's complement of these two numbers we use the Eq. (9) as follow.

$$(\mathrm{Carry}_2 + \mathrm{sum}_2)' = (\mathrm{carry}_2)' + (\mathrm{sum}_2)' + 1 \tag{9}$$

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Let the output of C=0. If Cout2=1 then X is greater than Y. otherwise the numbers sum3 and sum2 are compared with Cout1 and sum1 (see D in figure 1).

If C=1, then we check next n bit (x_2 and y_2) which are the reminders of X and Y mod m_2.

Figure 2 shows the carry recognition circuit (CR). Note that Cin=1 in CR1 and CR2 but it is zero in CR3.

5 Comparison

One of the fastest RNS comparators for module set $(2^n, 2^n - 1, 2^n + 1)$ is introduced in [3]. In Table I, the novel proposed comparator for this module set is compared with the previous design and the results are shown.

Table I. Compare the proposed comparison via other techniques.

	OR/AND	XOR / XNOR	INV	MUX	HA	FA	N/N+1 binary comparator	Delay
[3]	14n	2	5n	6n+ 134	28n+ 30	-	1	[log n]t_{or}+ t_{inv}+ $9t_{mux}$ $(n+8)$ t_{FA}+
Proposed	8n+15	10n+2	12n+12	6n	6n-1	8n+4	1	$4t_{not}$+$6t_{FA}$+ $5t_{and}$+$2t_{HA}$ $2nt_{mux}$+$2t_{xor}$

Performance Comparison:

Unit Gate Delay:

[3]. $4n+ 36\log_n$

Proposed: $2n+39$

Unit Gate Area:

[3]. $115n+186$

Proposed: $132n+55$

Time Complexity:

[3]. $460n^2+115n\log n$

Proposed: $264n^2$

As seen the proposed comparator for the module set $(2^n, 2^n - 1, 2^n + 1)$ is faster, but the hardware cost of the presented converter used 1.14 times more hardware. However the result of comparison causal the excellence of the novel method compared with to the previous method, which has significant reduction in comparison delay and also time complexity.

6 Conclusion

In this paper a novel parallel RNS comparator is introduced, which is faster in comparison with previous works for the module set $(2^n, 2^n - 1, 2^n + 1)$. As shown, this schema has a reduction in time complexity.

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