

Wide dynamic range transimpedance amplifier IC for 100-G DP-QPSK optical links using 1- μ m InP HBTs

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Abstract: Using 1- μ m InP HBT technology, a transimpedance amplifier (TIA) IC for optical links using 100-Gb/s dual polarization quadrature phase shift keying (100-G DP-QPSK) was designed and fabricated. Its wide dynamic range of 0.2~2 mAppd input current and good linearity of less than 3.3-% total harmonic distortion (THD) were confirmed. Also, externally controllable functions such as output amplitude adjustment, output shutdown, and auto/manual gain control switching were successfully implemented with InP HBT technology.

Keywords: transimpedance amplifier, 100 G, DP-QPSK, InP HBT

Classification: Electron devices, circuits, and systems

References

- [1] Y. Miyamoto and S. Suzuki, "Advanced Optical Modulation and Multiplexing Technologies for High-Capacity OTN Based on 100 Gb/s Channel and Beyond," *IEEE Commun. Mag.*, vol. 48, no. 3, pp. S65–S72, March 2010.
- [2] K. Murata and T. Saida, "Optical Device Technologies for Future Network Evolution," *NTT Technical Review*, vol. 9, no. 3, March 2011, [Online] <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201103fa6.html>
- [3] Optical Internetworking Forum, "Implementation Agreement for Integrated Dual Polarization Intradyn Coherent Receivers," IA # OIF-DPC-RX-01.0, Sept. 2011, [Online] <http://www.oiforum.com/public/impagreements.html>
- [4] K. Sano, T. Yoshimatsu, H. Fukuyama, and Y. Muramoto, "Photodiodes and Transimpedance Amplifiers for 100-Gbit/s Digital Coherent Optical Communications," *NTT Technical Review*, vol. 9, no. 3, March 2011, [Online] <https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr201103fa10.html>
- [5] C. Knochenhauer, B. Sedighi, and F. Ellinger, "40 Gbit/s transimpedance amplifier with high linearity range in 0.13 μ m SiGe BiCMOS," *IEE Electronics Letters*, vol. 47, no. 10, pp. 605–606, May 2011.
- [6] C. R. Doerr, L. L. Buhl, Y. Baeyens, R. Aroca, S. Chandrasekhar, X. Liu, L. Chen, and Y.-K. Chen, "Packaged Monolithic Silicon 112-Gb/s

- Coherent Receiver,” *IEEE Photon. Technol. Lett.*, vol. 23, no. 12, pp. 762–764, June 2011.
- [7] K. Murata, T. Saida, K. Sano, I. Ogawa, H. Fukuyama, R. Kasahara, Y. Muramoto, H. Nosaka, S. Tsunashima, T. Mizuno, H. Tanobe, K. Hattori, T. Yoshimatsu, H. Kawakami, and E. Yoshida, “100-Gbit/s PDM-QPSK Coherent Receiver with Wide Dynamic Range and Excellent Common-mode Rejection Ratio,” *European Conference and Exhibition on Optical Communication (ECOC) 2011*, Tu.3.LeSaleve.1, Sept. 2011.
- [8] Y. K. Fukai, K. Kurishima, M. Ida, S. Yamahata, and T. Enoki, “Highly reliable InP-based HBTs with a ledge structure operating at a current density over $2\text{ mA}/\mu\text{m}^2$,” *Int. Conf. Indium Phosphide and Related Materials (IPRM) 2005*, pp. 339–342, May 2005.

1 Introduction

To meet increasing demands for greater capacity in long-haul optical links, optical transmission systems based on 100-Gb/s dual polarization quadrature phase shift keying (100-G DP-QPSK) have attracted attentions [1, 2]. In the receiver side of the 100-G DP-QPSK systems, the transimpedance amplifier (TIA) IC is the key component for converting a varying photocurrent signal ($0.2\sim 2\text{ mAppd}$) into a constant voltage amplitude signal ($>700\text{ mVppd}$). Moreover, differing from traditional TIAs for on-off keying (OOK) optical systems, the TIAs for 100-G DP-QPSK systems are required to have good input-output linearity represented by a total harmonic distortion (THD) of less than 5% and to equip many externally controllable functions such as output amplitude adjustment, output shutdown, and automatic/manual gain control switching [3]. These requirements are originated from the unique receiver architecture of 100-G DP-QPSK systems, in which the TIAs’ analog output are digitized by analog-to-digital converters (ADCs) and then processed in digital domain by digital signal processors (DSPs) [2]. So far, some TIA ICs for 100-G DP-QPSK systems have been reported in the literature using InP HBTs [4] (our previous work), and SiGe BiCMOS [5, 6]. However, these reports describe only a few IC performances such as gain and THD, and externally controllable functions are not included [4, 5] or not explicitly shown [6]. This paper reports 100-G DP-QPSK TIA IC with wide a dynamic-range ($0.2\sim 2\text{ mAppd}$ input dynamic-range), good linearity (less than 3.3-% THD), and externally controllable functions (output amplitude adjustment, output shutdown, and auto/manual gain control switching). The IC was designed and fabricated with $1\text{-}\mu\text{m}$ InP HBT technology which has only npn-type as a kind of transistor.

2 IC Design and fabrication

Figure 1 (a) shows the circuit diagram of the TIA. To convert and amplify the input current signal into a constant voltage signal, the first stage TIA (FS TIA), balance adjuster (BA), variable gain amplifier 1 (VGA1), variable gain amplifier 2 (VGA2), and output buffer (OBF) are cascaded. The FS

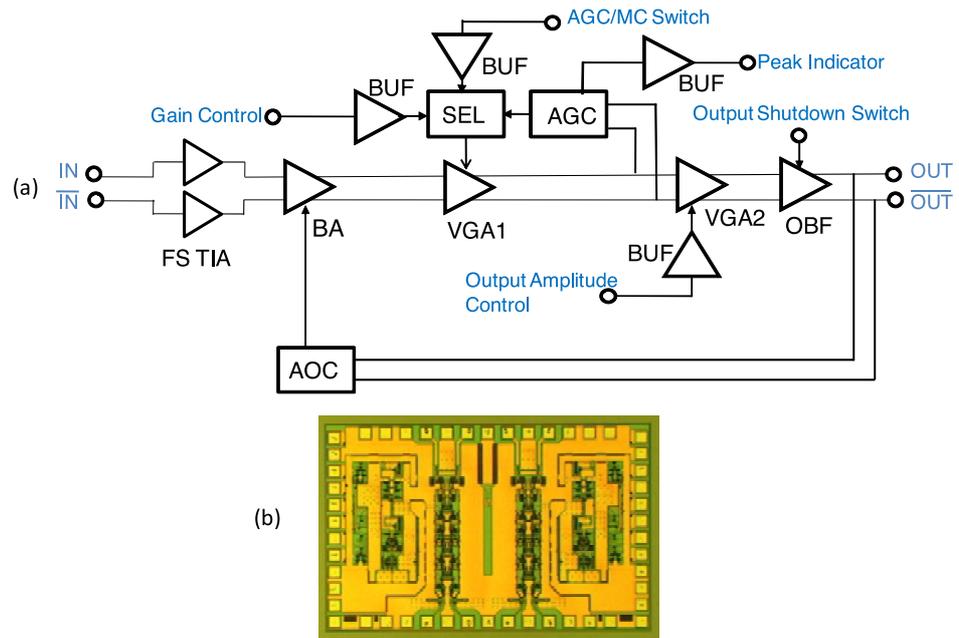


Fig. 1. InP HBT TIA for 100-G DP-QPSK Optical Links
(a) Circuit block diagram, (b) IC chip photo

TIA comprises two of a single-ended shunt-shunt resistor feedback amplifier. Each single-ended amplifier amplifies a true or complementary component of the differential input current. The BA consists of two differential pairs which share collector resistor loads. One of the differential pairs is for amplifying the output signals of the FS TIA, and the other is for canceling DC offset utilizing the signal from the auto offset cancel amplifier (AOC). The VGA1 consists of four cascaded amplifiers: 1st variable gain amplifier by the Gilbert cell, 1st fixed gain amplifier by a simple differential amplifier, 2nd variable gain amplifier by the Gilbert cell, and 2nd fixed gain amplifier with parallel resistor feedback. By using two variable gain amplifiers, large variable gain range of more than 20 dB is attained, which leads to a constant output amplitude for a wide input dynamic range of 0.2~2 mAppd; 0.2~2 mAppd corresponds to an optical signal input dynamic range of $-20\sim 0$ dBm in a 100-G DP-QPSK receiver [7] for +15-dBm local optical power input. This $-20\sim 0$ dBm range satisfies a standard 100-G DP-QPSK system requirement [3]. Furthermore, in order to maintain good input-output linearity, the gain of a following amplifier is set to be larger than that of a preceding one. This gain setting prevents an overly large voltage amplitude input in the cascaded amplifiers, and provides good input-output linearity. Also, for the VGA1, an auto gain control loop can be formed. The auto gain control amplifier (AGC) senses the voltage amplitude of the VGA1 output and controls the VGA1's gain automatically so that the VGA1 output has a designated amplitude designed in the AGC. At the output of the AGC, the gain control signal selector (SEL) is placed. The SEL selects the gain control signal either from the AGC or the buffer following the gain control terminal. If the AGC (the buffer following gain control terminal) is selected, the TIA's gain is controlled under the auto

(manual) gain control mode. Switching between auto/manual gain control modes is done through the AGC/MC switch terminal, which accepts low-voltage transistor-transistor logic (LVTTL) level. If low/high level of LVTTL (0–0.8 V/2.0–3.3 V) is applied to the AGC/MC switch, the TIA operates under the manual/auto gain mode. The VGA2 is made of two cascaded amplifiers: fixed gain amplifier by a simple differential amplifier and variable gain amplifier by the Gilbert cell. The gain of the Gilbert cell in the VGA2 is varied by the output amplitude control terminal, and this architecture provides the function of output amplitude adjustment. Finally, the OBF, made of a simple differential pair, outputs the amplified voltage signal of up to >700 mVppd. In the OBF, an output shutdown switch is also deployed. The principle of the output shutdown is halting of a voltage generator for current sources in the OBF. The interface of the output shutdown control is also LVTTL level. In the case where output shutdown control is in the low/high level of LVTTL, output shutdown is enabled/disabled.

The TIA IC was fabricated with using highly reliable 1- μm InP HBT technology [8], whose current cut-off frequency (f_t) is 170 GHz. Since the TIAs for 100-G DP-QPSK need to cover up to 32-Gbaud for one channel and 22-GHz bandwidth at least [2, 3], this InP HBT technology is attractive in terms of obtaining high-speed and wide-bandwidth performances. Figure 1 (b) is a photograph of the TIA IC. Two TIA circuits are integrated in one IC chip, shown in Fig. 1 (b). Chip size is 1.65 mm x 2.5 mm. Since a 100-G DP-QPSK receiver uses four TIAs [2, 7], two sets of this chip are used in the receiver. The power supply voltage for the TIA is designed to be +3.3 V, a common supply voltage in transponder modules, while our previous InP HBT TIA IC [4] required –5.2 V. One of the TIA dissipates 0.43 W at +3.3 V.

3 IC measurements

We measured the fabricated TIA IC on wafer. Figure 2 (a) shows the frequency responses of differential gain (S_{DD21}) under input dynamic range (0.2~2 mAppd). The frequency-gain curves of maximum/minimum gain in the figure are corresponding to ones for minimum (0.2 mAppd)/maximum (2 mAppd) input current, respectively. These curves were measured in the manual gain control mode with changing of the voltage of gain control terminal. Responding to 20-dB variation of the input current, the TIA IC changes its differential gain in the range from 34 dB to 14 dB. The –3 dB-down-gain frequencies (i.e. bandwidth) were slightly lowering as the gain was decreased (25.1/24.3 GHz for the maximum/minimum gain), but they exceeded the least required bandwidth of 22 GHz. Figure 2 (b) shows the differential output voltage amplitude change under the input dynamic range. Here the input signal was a 32-Gbps NRZ differential voltage one, and we transformed the input voltage swing into a current one in the figure with using TIA's input impedance of $\sim 50 \Omega$ (for single-ended). In this measurement, auto gain control mode was selected, and output amplitude control voltage was set so

that the available maximum output amplitude was obtained. In the input dynamic range from 0.2 mAppd to 2 mAppd, an almost constant output amplitude of >800-mVppd was confirmed. This behavior of constant output amplitude means that the gain variable coverage is sufficient and that the AGC loop works well. Also, this maximum >800-mVppd output amplitude sufficiently exceeds a typical requirement of ref. [3] (500 mVppd). Figure 2 (c) shows the THD variation under input dynamic range. Here, we used a 1-GHz sinusoidal differential voltage signal as the input, and the voltage swing was transformed into a current one using the $\sim 50\text{-}\Omega$ input impedance of the TIA. The auto gain control mode was chosen and the output amplitude was set so to be about 500-mVppd, which is the condition denoted in ref. [3]. Across the input dynamic range, the THD was kept as low as below 3.3%, which meets the requirement of ref. [3]. Also, this low THD value validates that gain distribution design in VGA1 is effective in order to maintain good input-output linearity.

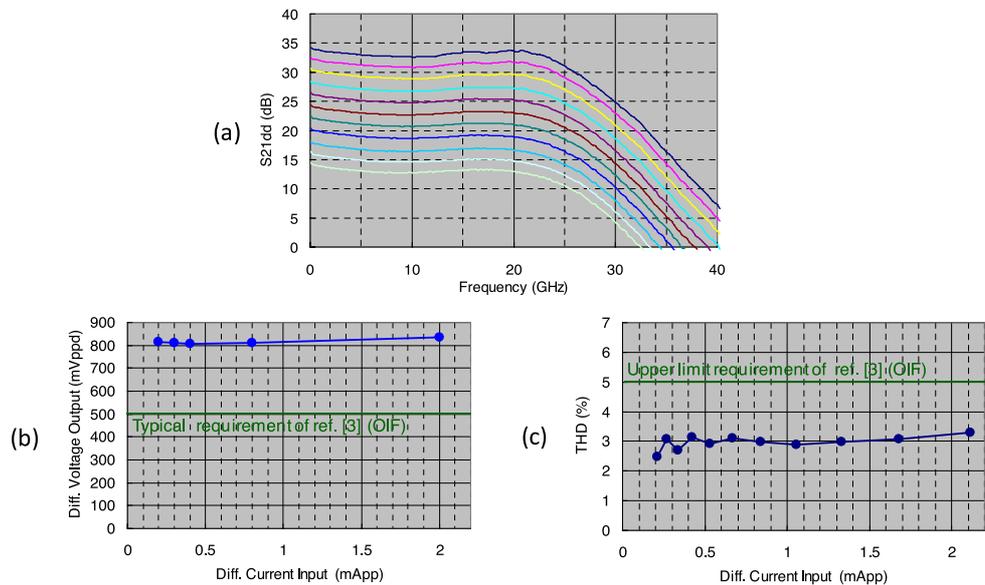


Fig. 2. Measured characteristics of TIA (a) Frequency responses of differential gain (b) Differential current input vs. differential voltage output for 32 Gbps NRZ signal (c) Differential current input vs. THD for 1 GHz sinusoidal wave

We also confirmed externally controllable functions implemented in the TIA. Figure 3 (a) shows the output amplitude control characteristic through the terminal of output amplitude control (OA). With varying of the voltage of OA in an analog manner, the differential output amplitude is adjustable in the range from ~ 100 mVppd to ~ 800 mVppd. Figure 3 (b) is the signal output behavior controlled by output shutdown function. Here, the true component of the differential output is shown. When a high level of LVTTL (2.0 V and 3.3 V) was applied into the terminal of output shutdown switch (SHD), ~ 400 m-Vpp single-ended output voltage swing and clear 32-Gbps

NRZ eye pattern were confirmed. In the case where SHD voltage is a low level of LVTTL (0 V and 0.8 V), the swing was reduced to less than 20 mVpp. This behavior agrees with the design of output shutdown function.

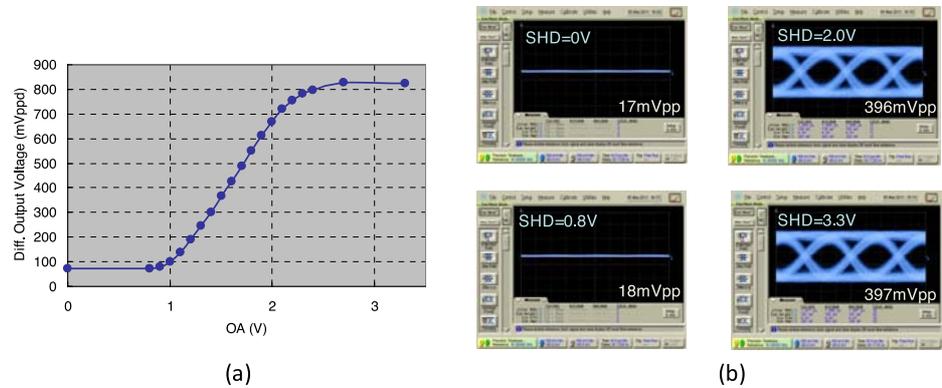


Fig. 3. Externally controllable functions in TIA (a) Output amplitude control (b) Output shutdown

4 Conclusion

100-G DP-QPSK TIA IC was designed and fabricated using 1- μ m InP HBT technology. A wide dynamic range of 0.2~2 mAppd and high linearity of less than 3.3-% THD in the input dynamic range were confirmed. Also, externally controllable functions such as output amplitude adjustment, output shutdown, and auto/manual gain control switching were successfully implemented. These performance levels are favorable for use in 100-G DP-QPSK receivers.

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