

Design of switching-mode CMOS frequency multipliers in sub-Terahertz regime

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Abstract: Switching mode CMOS frequency multipliers are studied in sub-Terahertz regime. Analysis on the multiplier architectures and optimal gate bias at CMOS switch are investigated to maximize output power at designated harmonics. Utilizing a differential pair, a 195 GHz tripler having a hair-pin filter is designed to maximize 3rd harmonics with -14.8 dB of conversion gain (CG) from $P_{in} = +13$ dBm of the balanced input, while the 260 GHz quadrupler utilizes quadruple-push pairs which achieves $CG = -16$ dB from two $+13$ dBm of the balanced I/Q driving signals in a 65 nm digital CMOS process.

Keywords: sub-Terahertz, CMOS, multiplier, tripler, quadrupler

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Recently CMOS transceivers beyond 100 GHz have been widely investigated for sensing and wireless communication applications [1, 2]. As frequency becomes even beyond the maximum oscillation frequency (f_{max}) of the CMOS, a compact and highly efficient frequency multiplier has been one of the interesting topics.

This paper studies on the architecture and design trade-off of the switching-mode CMOS frequency multipliers. Based on the simplified model with switch ON resistor (R_{ON}) and the drain parasitic capacitance (C_D), we derive an optimal gate

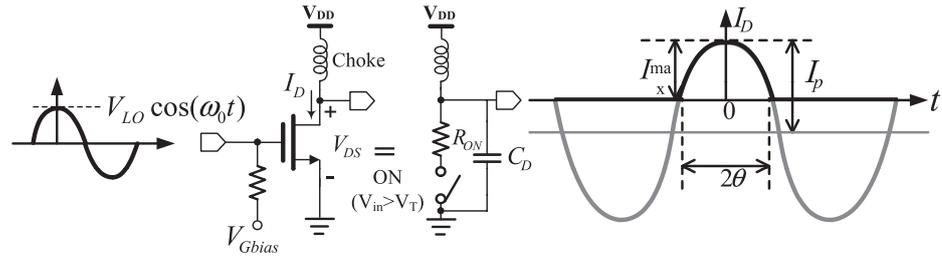


Fig. 1. Equivalent model used in deriving an optimal gate bias point under the hard switching-mode operation.

biasing voltage for the maximal harmonic generation for the switching-mode CMOS multipliers. The upper limit of the switch size should be determined based on the bandwidth and output matching inductance at the sub-THz as well as the driving LO power. Based on the design analysis, 195 GHz tripler and 260 GHz quadrupler are presented in 65 nm CMOS.

2 Design considerations on CMOS frequency multipliers

2.1 Optimal biasing voltage for the harmonic generation in CMOS

Theoretically, the conversion gain (CG) of generating a k^{th} harmonic power is limited by $1/k^2$ from positive nonlinear resistors [3]. In order to generate the sub-terahertz signal higher than f_{max} of the 65 nm CMOS, the frequency multipliers must be carefully designed since the MOS device in triode regime can achieve at best -9.54 dB and -12.04 dB of maximum CG for the tripler and the quadrupler, respectively. Therefore it is essential to find an efficient way to combine harmonic powers to generate required output power at (sub)-THz regime. Moreover a strong fundamental signal at the output should be effectively suppressed or rejected to prevent undesired intermodulation. For this purpose a pseudo-differential pair driven by the balanced fundamental signal must be an appealing odd-harmonics generator owing to the suppression of even harmonics. For even harmonic generation, N -push structure driven by balanced fundamental driving signals provide efficient harmonic current combining from separate clamping devices [1]. Fig. 1 represents a simplified switching model with the NMOS clamping device. The conduction angle (2θ) of the hard switching device is determined by

$$\theta = \cos^{-1}(1 - I_{\text{max}}/I_{pk}). \quad (1)$$

Practically the gate driving LO signal should be strong enough to avoid undesirable stability issue and noise bump from the switching mode operation [4]. When the clamping MOS device is driven by high swing fundamental signal ($V_{LO} \cdot \cos(\omega_0 t)$) at the gate, the device is in the triode region during ON/OFF transition period. The conductance of the device equals to the channel resistance at triode, the maximum drain current ($I_{D\text{max}}$) is given by:

$$I_{D\text{max}} = G_{ON} V_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{LO} + V_{G\text{bias}} - V_T) V_{DS}. \quad (2)$$

where $V_{G\text{bias}}$ is the gate bias voltage which determines the conduction angle (2θ).

Thus the required gate bias voltage for a given conduction angle θ is

$$V_{Gbias} = V_T - V_{LO} \cos \theta. \quad (3)$$

where V_T is the threshold voltage of the switching MOS.

From the Fourier expansion of the clamped current waveform, the k^{th} harmonic component of the drain current can be expressed as a function of θ given by [5]

$$I_{D(k)} = \frac{2}{\pi} \frac{\sin(k\theta) \cos(\theta) - k \sin(\theta) \cos(k\theta)}{k(k^2 - 1)} I_{pk} = f_k(\theta) I_{pk}. \quad (4)$$

Thus we find that the output of the even-harmonic generator including the quadrupler is maximized at $V_{Gbias} = V_T(2\theta = \pi)$, while the output of tripler is maximized with $2\theta = 2\pi/3$ which sets $V_{Gbias} = V_T - 0.5V_{LO}$ from Eq. (3). Hence V_{Gbias} must be chosen close to zero in the strong LO driving condition for the tripler.

2.2 CMOS switching-mode frequency multiplier design

To maximize CG of the multiplier, the load of an arbitrary frequency multiplier should force unwanted output harmonic powers to zero by providing zero impedance while it must be conjugate-matched to the designated frequency. For odd harmonics generation, a differential pair can be used to realize the frequency selective load since the load resonator can be placed between the two drain nodes differentially as shown Fig. 2. As a result, the resonant inductor L_{DM} can absorb drain capacitances ($0.5C_D$) while it provides the power supply path throughout the common mode center-tap. The load resonator can provide relatively low impedance at f_0 , and other odd harmonics with moderate quality factor (Q). With $Q = 10$, the load impedances at the fundamental and 5th harmonic drops to 13.5% and 12.5% of the impedance at the resonate frequency, respectively.

For even harmonics generation, N -push structure is promising since odd harmonic currents are neutralized at the common node of the N -push pairs. Thus a bulky and lossy filter is unnecessary. Moreover, higher even harmonics at $kN\omega_0$ are usually negligible. A narrow DC supply line made of $\lambda_g/4$ T-line at 4th harmonic is one way to suppress 8th harmonic in the quadrupler. Fig. 3 shows an equivalent model used for estimating design parameter trade-off in the quadrupler. Ideally the device having bigger gate width (W) achieves higher output power and better efficiency since effective channel resistor R_{on} is inversely proportional to W . The upper limit of W is constrained by the parasitics at the drain node. But increased gate width requires larger LO driving signal to achieve a proper switching mode operation.

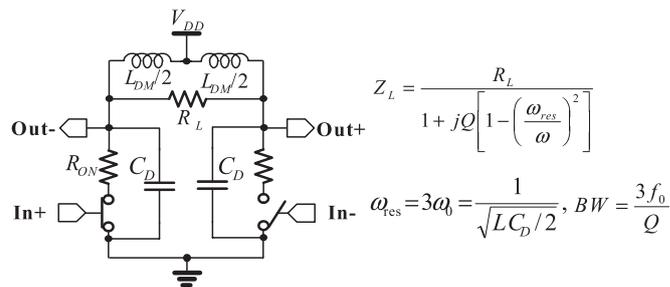


Fig. 2. Equivalent model for a balanced tripler with a pseudo differential pair.

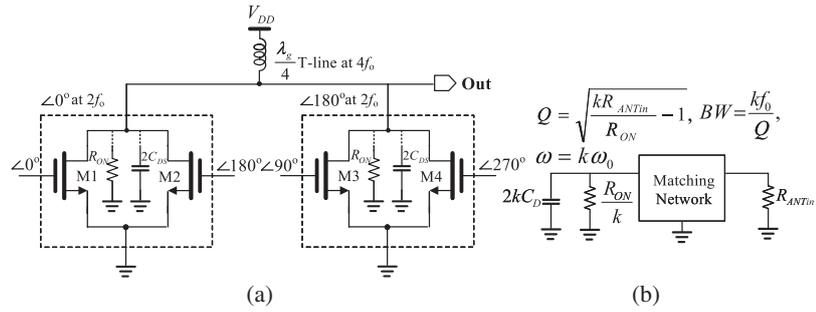


Fig. 3. (a) Equivalent model used in analyzing the quadrupler consisting of two push-push pairs, and (b) Design relations between device size and bandwidth (BW).

Moreover, the reduction of R_{ON} requires higher output matching Q due to increased C_D which also limits the antenna input impedance and the bandwidth ($BW = k\omega_0/Q$) as well. In sub-THz regime, matching sensitivity is mainly constrained by the matching inductor size. When C_D at drain node is not properly resonated-out, the CG drops significantly due to the residual capacitive loading. Thus the advantage of the gate-length scaling-down is clear which results in less R_{ON} and smaller C_D .

3 Sub-THz frequency multipliers design in 65 nm CMOS

3.1 195 GHz tripler with a pseudo differential pair

As presented in section 2, a pseudo-differential pair is a useful configuration to combine odd harmonics by suppressing even harmonics efficiently. The drawback of using the differential pair is a strong fundamental signal exists, which leaks directly to output. From Eq. (4), the fundamental signal is 6 dB larger than the 3rd harmonic from the hard switching differential pair. Even with $Q = 10$ of the differential resonator, the leakage at f_0 is only 2.79 dB smaller than the 3rd harmonic power. To reject the leakage effectively, the microstrip T-line (MSTL) hair-pin band pass filter is used as shown in Fig. 4-(a). By folding the parallel coupled $\lambda_g/2$ wavelength resonator into “U” shape, the hairpin resonator is obtained. The differential output from the filter is routed to the load using the Coplanar Strip-line (CPS). The designed filter has 1.9 dB of insertion loss (IL), and provides more than 10 dB of fundamental signal rejection as shown in Fig. 5-(a). The output resonator is tuned to 3rd harmonic including the hair-pin filter.

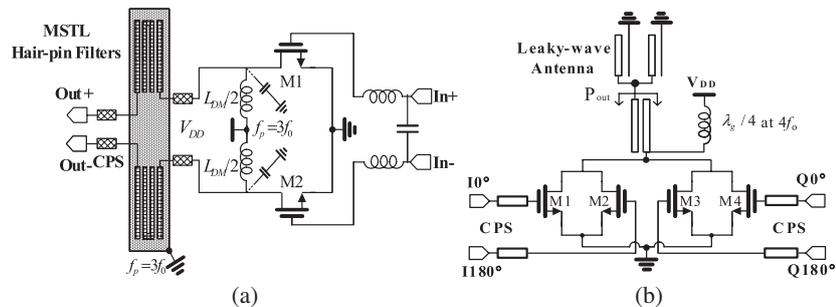


Fig. 4. Circuit diagrams of (a) 195 GHz tripler with the pseudo-differential pair combined with output hair-pin filter, (b) 260 GHz quadrupler with two push-push pairs with a frequency selective antenna as a load.

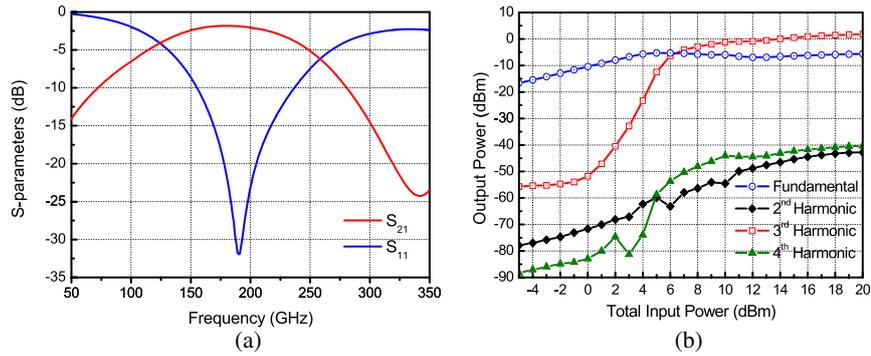


Fig. 5. (a) Simulated s-parameters of hair-pin filter, (b) tripler harmonics vs. P_{in} .

Fig. 5-(b) presents the harmonic output powers from the differential pair before the hair-pin filter at output. The hard switching-mode is well established when driving P_{in} is larger than 10 dBm. With $M1 = M2 = 20 \mu\text{m}$, the output power of the third harmonic saturates around +13 dBm of the input power from the driving PA.

3.2 260 GHz quadrupler

The quadrupler utilizes a quadruple-push driven by the balanced I/Q signals as shown in Fig. 4-(b). The gate bias close to V_T is applied from the center tap of the transformer of the driving PA. I/Q signals are routed with CPS having $Z_0 = 92 \Omega$ ($W = 8 \mu\text{m}$, $G = 6 \mu\text{m}$) and the series inductor L_{gM} is realized with by increasing the line spacing of the CPS where conjugated LC matching is used. Considering R_{ON} , 10% of the matching BW , and the LO drivability, the width of switch is set to $20 \mu\text{m}$ where it maximizes the CG from the 13 dBm PA. The output coupled line serves as a filter which also blocks DC from the half-width leaky-wave antennas with one of the edges shorted to ground [6]. With $P_{in} = +13 \text{ dBm}$ applied to each I/Q push-push pair (total +16 dBm), the 4th harmonic output achieves -0.3 dBm to the antenna with $8.9-j24 \Omega$ of antenna impedance (Fig. 6-(a)). The output power of each harmonic is presented as a function of I/Q phase mismatch in Fig. 6-(b). Since each pair is driven by the balanced PA separately, I/Q mismatch at LO signal is only considered. The combined 4th harmonic power is minimized with $\pm 45^\circ$ of mismatch ($\Delta\Phi$) at f_0 which becomes $\pm 180^\circ$ at $4f_0$. Since two push-push pairs are used, the 2nd harmonic can dominate over the 4th harmonic power when $|\Delta\Phi| > 10^\circ$.

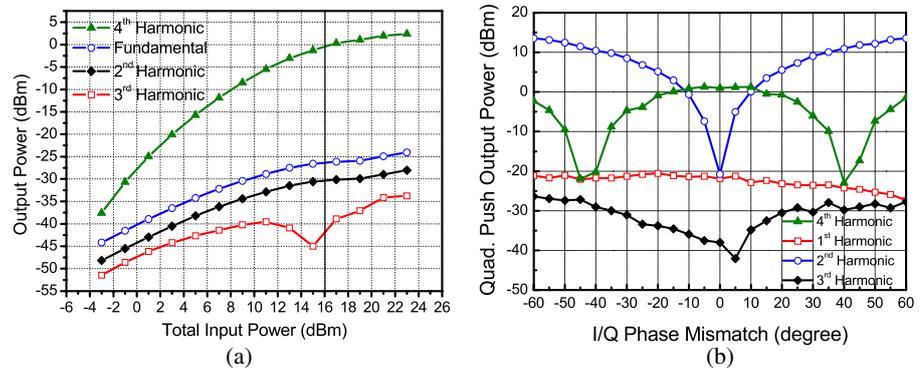


Fig. 6. Simulated quadrupler harmonics vs. (a) input power, (b) I/Q phase mismatch.

4 Measurement

Fig. 7 presents an implemented 260 GHz transceiver in 65 nm CMOS [1]. The tripler driven by +13 dBm of PA at V-band was used as a 195 GHz LO driver for the down-converting mixer. The Tx powers from two separate quadruplers were spatially combined to achieve higher output power. Using an Erickson power-meter, WR-3.4 VDI 25 dB gain horn antenna, and a waveguide transition, +5.0 dBm of maximum EIRP were measured with $V_{Gbias} = 0.41$ V at 246 GHz while +6.8 dBm of EIRP was expected in simulation. As shown in Fig. 8, the functionality of the Rx with the tripler was verified with a wireless data-link over a 40 mm with 6 Gb/s of toggling signal. The signal was maximized by setting V_{Gbias} of tripler close to zero.

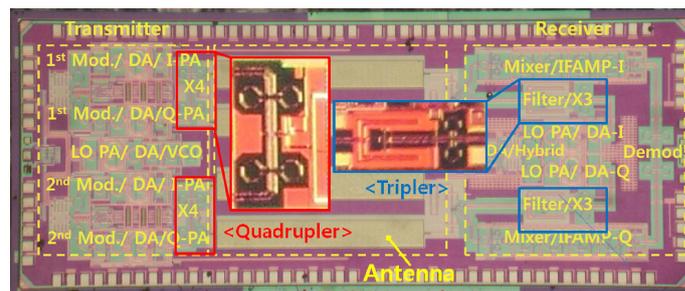


Fig. 7. Microphotograph of the fabricated fully integrated transceiver having 260 GHz quadrupler (red) and 195 GHz tripler (blue) (size: 4.0×1.5 mm²).

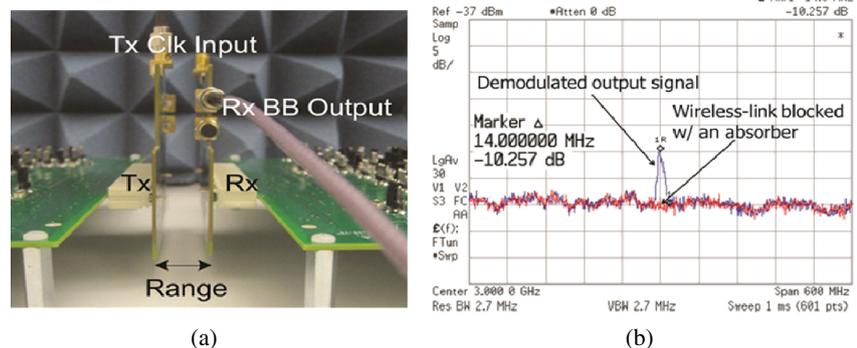


Fig. 8. (a) Wireless chip-to-chip link setup, (b) measured demodulated 6 G/b toggling signal over 40 mm of wireless link (red: signal blocked with an absorber).

5 Conclusion

Switching mode CMOS tripler and quadrupler in sub-THz range were analyzed and implemented in 65 nm CMOS. The optimal gate biasing and switch sizing were studied under hard switching condition which would serve as a useful guideline for the similar frequency multiplier design in the THz regime.

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