ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.12, No.7, 1–6

# Gate-All-Around Silicon Nanowire Transistors with channel-last process on bulk Si substrate

**Xiaolong Ma, Huaxiang Yin[a)], and Peizhen Hong**

*Institute of Microelectronics, Chinese Academy of Science,*

*No. 3 of Bei-Tu-Cheng West Road, Chaoyang, Beijing 100029, China*

a) *yinhuaxiang@ime.ac.cn*

**Abstract:** For the first time, a Gate-All-Around (GAA) Silicon Nanowire Transistor (SNWT) with one special nanowire channel-last (NCL) process technology on silicon (Si) substrate is reported. Different from the traditional approach that the nanowire channels are formed and released at the initial steps of the process flow, the NCL process features the release of nanowire channels in high-k/metal gate-last process during the integration of conventional bulk-Si FinFET. It provides a stable way for the introduction of nanowire transistors in the FinFETs process for mass productions. The fabricated n-type transistors with the effective nanowire diameter ($D_{NW}$) of 12 nm~17 nm and the gate length of 100 nm demonstrated excellent subthreshold characteristics (subthreshold swing = 64 mV/V and drain induced barrier lowering = 24 mV/V). Meanwhile, it's found that the $H_2$ baking process as well as the optimized interface gate oxidation on NW channels greatly improved the device's SS and off-current parameters.

**Keywords:** nanowire, FinFET, Si, channel last

**Classification:** Electron devices, circuits, and systems

## References

[1] K. J. Kuhn: IEEE Trans. Electron Dev. **59** (2012) 1813. DOI:10.1109/TED.2012.2193129

[2] R. K. Cavin, P. Lugli and V. V. Zhirnov: Proc. IEEE **100** (2012) 1720. DOI:10.1109/JPROC.2012.2190155

[3] J. P. Colinge and S. H. Dhong: IEEE Custom Integr. Circ. Tech. Dig. (2013) 11-3. DOI:10.1109/CICC.2013.6658401

[4] S.-Y. Wu, C. Y. Lin, M. C. Chiang, J. J. Liaw, J. Y. Cheng, S. H. Yang, M. Liang, T. Miyashita, C. H. Tsai, B. C. Hsu, H. Y. Chen, T. Yamamoto, S. Y. Chang, V. S. Chang, C. H. Chang, J. H. Chen, H. F. Chen, K. C. Ting, Y. K. Wu, K. H. Pan, R. F. Tsui, C. H. Yao, P. R. Chang, H. M. Lien, T. L. Lee, H. M. Lee, W. Chang, T. Chang, R. Chen, M. Yeh, C. C. Chen, Y. H. Chiu, Y. H. Chen, H. C. Huang, Y. C. Lu, C. W. Chang, M. H. Tsai, C. C. Liu, K. S. Chen, C. C. Kuo, H. T. Lin, S. M. Jang and Y. Ku: IEDM Tech. Dig. (2013) 224. DOI:10.1109/IEDM.2013.6724591

[5] J. Zhuge, Y. Tian, R. S. Wang, R. Huang, Y. Q. Wang, B. Q. Chen, J. Liu, X. Zhang and Y. Y. Wang: IEEE Trans. Nanotechnol. **9** (2010) 114. DOI:10.1109/



DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015

TNANO.2009.2022537
[6] Y. Song, Q. X. Xu, J. Luo, H. J. Zhou, J. B. Niu, Q. Q. Liang and C. Zhao: IEEE Trans. Electron Dev. **59** (2012) 1885. DOI:10.1109/TED.2012.2194785
[7] S. Bangsaruntip, K. Balakrishnan, S.-L. Cheng, J. Chang, M. Brink, I. Lauer, R. L. Bruce, S. U. Engelmann, A. Pyzyna, G. M. Cohen, L. M. Gignac, C. M. Breslin, J. S. Newbury, D. P. Klaus, A. Majumdar, J. W. Sleight and M. A. Guillorn: IEDM Tech. Dig. (2013) 526. DOI:10.1109/IEDM.2013.6724667

## 1 Introduction

The Gate-All-Around (GAA) Silicon Nanowire Transistors (SNWT) has attracted considerable attention during the last decades as a promising candidate to overcome the scaling issues of MOSFETs at the roadmap of integration circuit process technology [1, 2, 3]. With multi-gate structures, GAA-SNWT demonstrates the best gate control and subsequently, the excellent parameters of the subthreshold slope (SS) and the drain induced barrier lowering (DIBL) to suppress serious short-channel effect (SCE) in ultra-short channels. For the purpose of applying the SNWT structures into the fabrication process flow of conventional bulk-silicon (Si) FinFETs for mass production, the fabrication technologies of GAA-SNWTs are necessary to be compatible with current state-of-the-art integration technology [4]. However, the traditional approach to fabricate GAA-SNWTs is to form and release the NW channels in the initial step of the transistor's fabrication and it causes a series of integration challenges [5, 6, 7]. The nanoscale NWs suspended on source/drain (S/D) pads are vulnerable to be broken during the gate etch and S/D engineering. Meanwhile, the S/D resistance is high due to a contact issues on NWs. The poly-Si dummy gate etch process always leaves the residual film distributing between stacked NWs for the shadowing effect. Some reported process methods are incompatible with the mainstream fabrication technology.

In this paper, a novel technology of NW channel-last (NCL) based on up-to-date high-k/metal-gate (HKMG-last) FinFET process is reported for the first time. The GAA-SNWT with the NCL approach is successfully fabricated and the integration process technologies as well as the excellent electrical characteristics are investigated in the paper.

## 2 Device fabrications

Fig. 1 shows the fabrication flow of the GAA-SNWT with NCL process. It is modified on the integration flow of conventional bulk-Si FinFETs [4]. On the normal Si substrate, the fin is patterning with general spacer-transfer lithography (STL) and it forms a sea of fins with the same pattern across whole the wafer. The landing pads with large geometry sizes, which are generally used for physical supporting the suspended NWs in previous reports [5, 6, 7], are removed from this process. A special etch process for a notched fin is developed for the formation of NW channels in later steps. The process approach of the fin notch etching is shown in Fig. 2(a). The process is similar to that of Bosch process for the deep Si-trench etching. It includes three main steps: Step-I is with an anisotropic Si etch for the


DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015

formation of upper Si fin; Step-II is with an isotropic Si etch for the notches formation on both sidewalls of the fin; Step-III is again with an anisotropic Si etch for the formation of lower Si fin. Between Step-I and Step-II, and Step-II and Step-III, a polymer passivation layer is formed on the surface of etched Si so as to protect the profile of the fin and notches. The size of later NW channel is determined by the height of the upper fin in Step-I. The notch is used for the isolation of the NW channel from the substrate. The height of the lower fin decides the thickness of STI oxides for adjacent device's isolations.

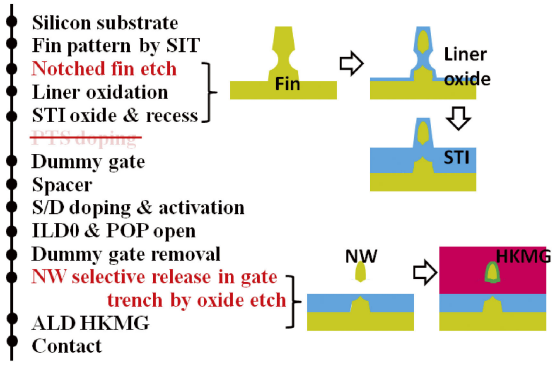



**Fig. 1.** The fabrication method of GAA-SNWT with NCL process based on the integration flow of conventional bulk-Si FinFETs.

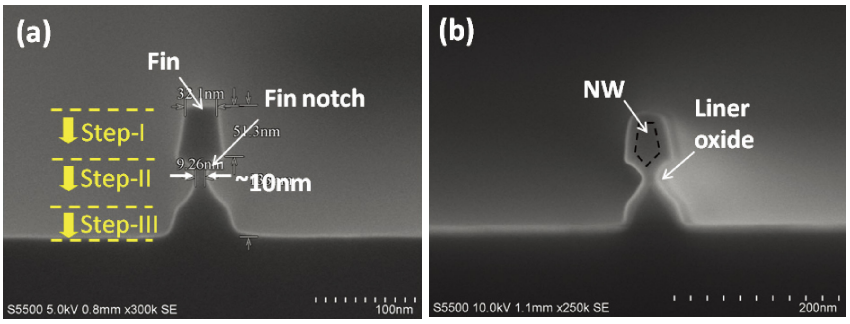



**Fig. 2.** (a) The notched fin by a special Si etch process with three steps; (b) The isolated NW structure supported by the oxide after a liner oxidation process.

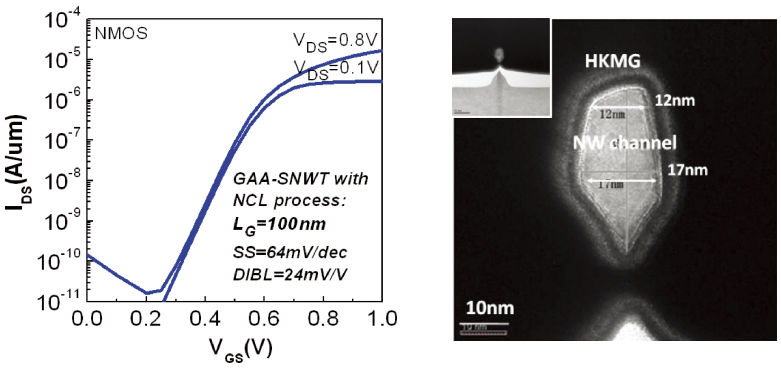
In Fig. 2(b), with 10 nm liner oxidization, the upper part of the notched fin is fully isolated from the bulk substrate and to form a floating fin structure. After a corner rounding and size scale-down by the oxidation step, the floating structure is finally turned into a special NW structure, which is physically supported by the oxide beneath the channel. Next, STI oxides are deposited and etched back to form a fin-like structure as shown in Fig. 1. The channel punch-through stopper (PTS) doping which is necessary for the bulk-Si FinFET is also skipped for the new structure. After that, the poly-Si dummy gate and the 3D spacer process as well as the source/drain (S/D) doping engineering are performed with the same technology of the bulk-Si FinFET. Following with inter-layer-dielectrics (ILD) deposition and planarization, the poly-Si dummy gate is removed with TMAH solution. In the dummy gate trenches, the NW channels on the oxide are released after an oxide


DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015

deep etch process. The $H_2$ baking process is also performed the surface passivation as well as the rounding of the NW channel. The new NWs are selectively formed in channel regions and are suspending on S/D regions in a self-aligned method. The NW channels are fabricated after the formation of S/D process and the new technology is named in NCL process. Next, the process of the multi-layered HKMG (IL/$HfO_2$-2.2 nm/TiN-2 nm/TaN-1 nm/W-100 nm) stack is finished all by ALD for the good surrounding around the floating NW channels in the gate trenches. Finally, the contact process is finished for the device's metalization.

## 3 Results and discussion

Fig. 3(a) shows the measured $I_{DS}$-$V_{GS}$ curves of the fabricated n-type GAA-SNWT by the NCL process with the gate length ($L_G$) of 100 nm. The cross-sectional image of the NW channel is shown in Fig. 3(b). The shape of the fabricated NW channel is more like an irregular diamond with the effective nanowire diameter ($D_{NW}$) of 12 nm~17 nm. The whole effective channel width ($W_{eff}$) is close to 47 nm. The multi-layered HKMG are well surrounding around the irregular channel and demonstrates good film uniformity. It provides a uniform MG effective-work-function (EWF) distribution around whole the channel. The threshold voltage ($V_{TH}$) of the device is defined with the constant current method ($V_{GS}$ while $I_{DS} = 10\,nA * W_{eff}/L_G$). The linear $V_{TH\text{-}lin}$ is 0.45 V and the value is little larger than that expected in the design. It is because a large MG EWF of ~4.4 eV in the gate stacks without a TiAl layer. The deposition process of TiAl is normally finished by a PVD sputtering process and it always induces a serious film fill issues at bottom part of the NW channel. Therefore, the film of TiAl is removed in the fabricated device. The drain-induced barrier lowering (DIBL) and the sub-threshold swing (SS) of the fabricated device are 24 mV/V and 64 mV/V, respectively. DIBL is defined as the $V_{TH}$ difference between the saturation region ($V_{DS} = 0.8$ V) and the linear region ($V_{DS} = 0.1$ V) for a unit drain voltage. The SS is defined as the slope for the $I_{DS}$-$V_{GS}$ curve under the saturation region. The results are much close the ideal value and demonstrate excellent electrical potential integrity in the NW channel due to a strong gate control for the GAA structure.




(a) (b)

**Fig. 3.** (a) The $I_{DS}$-$V_{GS}$ curves of the fabricated n-type GAA-SNWT by NCL process with $L_G = 100$ nm; (b) The cross-sectional image of the NW channel with multi-layered HKMG stacks.


DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015

In the GAA-SNWT device, the channel is formed with the special NCL process. The profile and the interface of the NW channel have a great effect the electrical parameters of the device. Fig. 4 compares the $I_{DS}$-$V_{GS}$ curves between those fabricated devices with and without $H_2$ baking process. The interface layer (IL) between the HK and the NW surface is also optimized. In case-I, the NW channel is oxidation with a high ozone concentration (~10 ppm) and with a $H_2$ baking process (780 °C, 1 min). In contrast, the NW channel in case-II is with a low zone concentration (~3 ppm) and without a $H_2$ baking process. The SS and the off-current ($I_{DS}$ while $V_{GS} = 0$ V and $V_{DS} = 0.8$ V) parameters of devices between case-I and case-II are 64 mV/dec, $1.4 \times 10^{-10}$ A/μm and 123 mV/dec, $2.2 \times 10^{-9}$ A/μm, respectively. The device in case-I demonstrates a clear performance advantage. It is expected from a nice interface and profile (a better corner rounding in case-I) with the optimized IL oxidation and $H_2$ baking process. The gate leakage ($I_G$) between the MG and the NW channel are shown in Fig. 5, too. $I_G$ in case-I ($2.0 \times 10^{-12}$ A/μm) is smaller than that of case-II ($2.0 \times 10^{-11}$ A/μm) and it also confirmed the speculation in previous sentences.

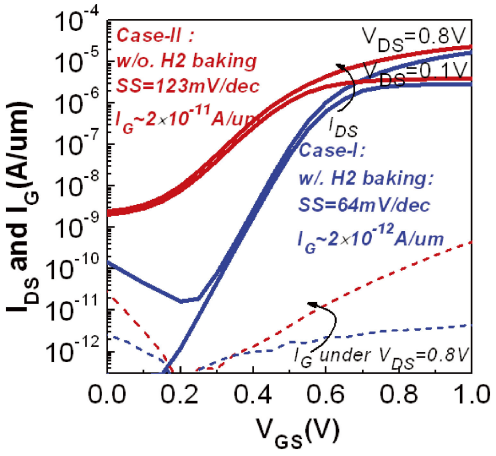



**Fig. 4.** The comparisons of $I_{DS}$-$V_{GS}$ characteristics between the GAA-SNWT with $H_2$ baking process and optimized IL process (case-I) and that without $H_2$ baking process and normal IL process (case-II).

## 4 Conclusion

In this paper, a new integration scheme of nanowire transistors featuring with NCL process fully compatible with conventional bulk-Si FinFET technology is reported. The fabricated n-type GAA-SNWT by NCL process demonstrated excellent SS (< 65 mV/V) and DIBL (< 25 mV/V) as well as off-current (< $2 \times 10^{-10}$ A/μm) parameters after $H_2$ baking and gate interface oxidation optimization on NW channels in gate-last process. The new technology provides a promising approach for the integration of nanowire technology into the industrial FinFET flow for mass production in next generations.


DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015

## Acknowledgments

This work was supported by "16/14 nm Basic Technology Research" of national 02 IC projects in China (No. 2013ZX02303). The authors would like to thank engineers in Integrated Circuit Advanced Process Center, IMECAS for their support in wafer processing.


DOI: 10.1587/elex.12.20150094
Received January 26, 2015
Accepted March 9, 2015
Publicized March 23, 2015
Copyedited April 10, 2015