ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.10, No.2, 1–6

A current-shaping technique for static MOS current-mode logic prescalers

Jian Shi[1a)], **Taishan Mo**[1,2], **Chengyan Ma**[1,2], **and Tianchun Ye**[1]

[1] *Institute of Microelectronics of Chinese Academy of Sciences, No.3, North Tucheng West Road, Chaoyang District, Beijing, 100029, P. R. China*

[2] *Hangzhou Zhongke Microelectronics Co., Ltd., 10F Innovation Tower, No.3850, Jiangnan Road, Binjiang District, Hangzhou, 310053, P. R. China*

a) *shijian@casic.ac.cn*

Abstract: This letter presents a current-shaping technique for static MOS current-mode logic (MCML) prescalers. Simply with two extra current-shaping capacitors the self-oscillating frequecy is increased. A current vector model is also presented to illustrate the principles. The prescaler with the current-shaping technique was fabricated in a 0.18-μm CMOS technology with a reference classic one. The measurement results show that the self-oscillating frequency of the prescaler with current-shaping achieves an improvement of 10%, resulting a 6 GHz highest operating frequency while the classic one could only work at 5.3 GHz. Consequently, the current-shaping technique improves the maxim divide range of the prescaler with 13.2%.

Keywords: current-mode logic, prescaler, current-shaping

Classification: Integrated circuits

References

[1] M. Alioto, R. Mita, and G. Plumbo, "Design of high-speed power-efficient MOS current-mode logic frequency dividers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1165–1169, Nov. 2006.

[2] R. Nonis, E. Palumbo, P. Palestri, and L. Selmi, "A design methodology for MOS current-mode logic frequency dividers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 245–254, Feb. 2007.

[3] U. Singh and M. M. Green, "Dynamics of high-frequency CMOS dividers," *Proc. ISCAS*, vol. 5, pp. 26–29, May 2002.

[4] T. H. Lee, "Oscillators and synthesizers," *The Design of CMOS Radio-Frequency Integrated Circuits*, second edition, Cambrige University Press, New York, 2004.

1 Introduction

Low-cost CMOS technology has become popular in fully-integrated radio-frequency transceivers for wireless communication. MOS current-mode logic (MCML) prescalers are essential building blocks in applications as frequency

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013

synthesis, synchronization, clock generation and data recovery. Owing to the characteristic of highest operating frequency, the trade-off between the speed and power dissipation becomes critical for a prescaler [1, 2].

The analysis of dynamics of the static MCML prescalers has been presented by Singh and Green [3]. The self-oscillation phenomenon gives a deeper understanding of the operational principle. Higher self-oscillating frequency means higher operation speed. In this letter, a current-shaping technique is proposed to improve the self-oscillating frequency and broaden the divide range. With the same power consumption, prescalers adopting this technique acquire 10% and 13.2% improvement in self-oscillating frequency and maximum divide range separately.

2 Principle of the design

The proposed prescaler is shown in Fig. 1. Two D flip-flops are connected in the master-slave form to attain quadrature output. They operate between the sensing mode and latching mode periodically and alternately. Two current-shaping capacitors C1 and C2 are added between the source sensing transistors (M5, M6 and M9, M10) and ground.

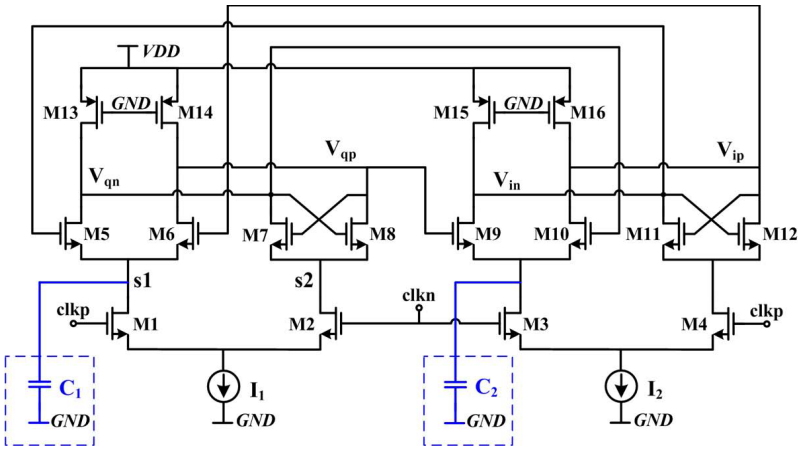

Fig. 1. Schematic of the static MCML prescaler with current-shaping technique

The self-oscillation happens when the product of the small signal transconductance of the latching transistor and the equivalent loading resistor R greater than one. As mentioned above, higher operating frequency requires higher self-oscillating frequency. In order to achieve this, a current vector model is proposed to give some insight into the self-oscillating frequency. As shown in Fig. 2, the axes represent the quadrature output of the prescaler. It can be noticed that the drain current of a loading transistor is equal to the sum of the drain current of a sensing transistor and a latching transistor. For instance:

$$I_{13} = I_5 + I_7. \tag{1}$$

where I_{13}, I_5 and I_7 represent the drain current of transistors M13, M5 and

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013

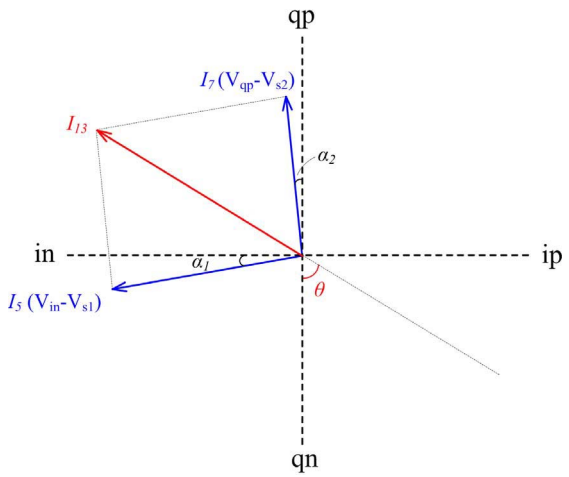

Fig. 2. The drain current vector diagram of M13, M5 and M7

M7 separately.

Under large signal condition, the phase of drain current is the same as the V_{gs} of the transistor [4]. Furthermore, there are tiny phase offsets between V_{gs} and the gate voltage V_g if we take the source parasitic capacitance into account. In Fig. 2, these tiny phase offsets are expressed as α_1 and α_2. In static MCML prescalers, the transistor M13 works in linear region as a load resistor. The current I_{13} flows past the RC network composed by M13 and the load capacitance of the output node to generate output voltage V_{qn}. Fig. 2 indicates the phase relationship between I_{13} and V_{qn}. In order to maintain stable self-oscillating state, a phase delay θ should be provided by the loading RC network. Similarly, this requirement shoud be satisfied at each quadrature output node.

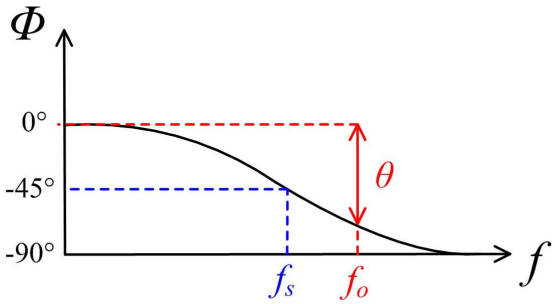

Fig. 3. The phase-frequency characteristic of the RC network

The phase-frequency characteristic of the RC network is shown in Fig. 3. f_s represents the pole and we could have:

$$f_s = \frac{1}{2\pi \cdot RC} \tag{2}$$

f_o represents the self-oscillating frequency of the prescaler. Assuming the current of sensing transistor I_5 is the same with that of the latching transistor

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013

I_7, if we ignore the tiny phase offsets α_1 and α_2, the phase delay provided by the RC network should be 45° and f_o equals f_s. From Fig. 3 we could get the conclusion that a larger θ means higher self-oscillating frequency.

The proposed current vector model provides a different angle to the research on the operating frequency restriction of prescalers. However, the results of our model have some common points with the classic delay-based theory proposed by [1, 2]. In our model, a smaller RC product means the oscillating frequency should be higher to compensate θ. Meanwhile, this implies a smaller time constant in delay-based theory. Therefore, a same conclusion is attained through two different ways.

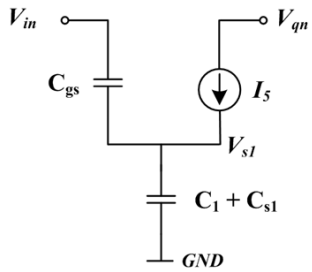

Fig. 4. Simplified small signal equivalent circuit when M5 is on and M6 is off

To obtain a larger θ, two small capacitors C_1 and C_2 are adopted to shape the amplitude and phase of the drain current of the sensing transistors. During the self-oscillation period, when M5 is on and M6 is off, the simplified small signal equivalent circuit of M5 is shown in Fig. 4. The drain current of M5 can be derived as:

$$I_5 = g_m \cdot V_{gs} = \frac{g_m \cdot V_{in} \cdot j\omega_0(C_1 + C_{s1})}{g_m + j\omega_0(C_{gs} + C_1 + C_{s1})} \tag{3}$$

where g_m is the transconductance of M5 and C_{gs} is the gate-source capacitance. From (3) the amplitude and phase advance of I_5 are obtained:

$$|I_5| = \frac{g_m \cdot \omega_0(C_1 + C_{s1}) \cdot |V_{in}|}{\sqrt{{g_m}^2 + {\omega_0}^2(C_{gs} + C_1 + C_{s1})^2}} \tag{4}$$

$$\alpha_1 = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega_0(C_{gs} + C_1 + C_{s1})}{g_m}\right) \tag{5}$$

From (4) and (5) we notice that the amplitude of I_5 is raised along with the increase of C_1. Meanwhile, the phase lead α_1 is decreased. Furthermore, Fig. 2 indicates that a raised $|I_5|$ will enlarge θ while a reduced α_1 will play the opposite role. Consequently, we can choose an optimal value of C_1 and C_2 to achieve a highest self-oscillating frequency. In this work, the two current-shaping capacitors are chosen to be 50 fF combining the calculation above and simulation results. To achieve smaller process deviation and a more accurate simulation model, the capacitors are implemented by radio-frequency MIM (Metal-insulator-Metal) capacitors with deep N-well and guard ring around. Besides, simulation results indicate that a 10% deviation of the capacitors will not degrade the performance of the prescaler obviously.

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013

3 Experimental results

Two static MCML prescalers have been implemented in a commercial 0.18-μm CMOS technology and the chip microphotograph is shown in Fig. 5. The only difference between the proposed prescaler and the classic one is two current-shaping capacitors are added. Each prescaler consumes 1 mA from a 1.8 V power supply.

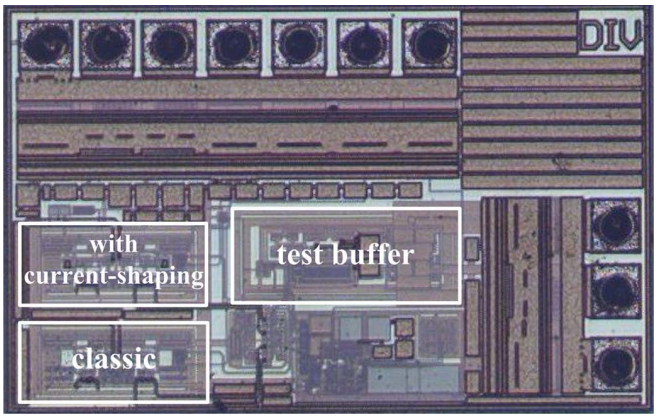

Fig. 5. Microphotograph of the proposed prescaler and the classic one

Fig. 6 shows the comparison of the two prescaler's sensitivity curves. The highest operating frequency of the MCML prescaler with the current-shaping technique is 6 GHz while the classic one could only work at 5.3 GHz which is further confirmed by Fig. 7.

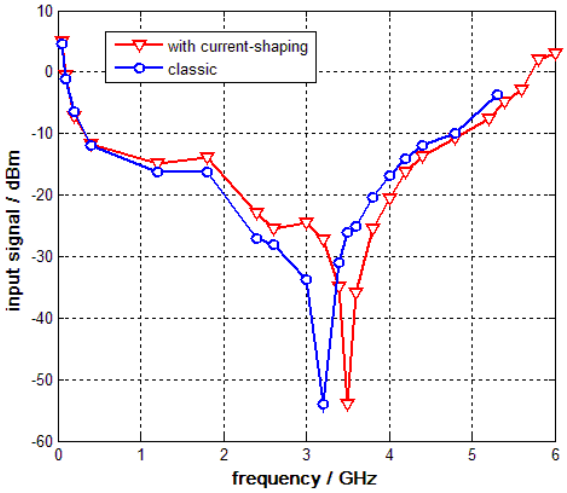

Fig. 6. Comparison of the two prescaler's sensitivity curves

In addition, Fig. 6 indicates this current-shaping technique has no influence on the divide characteristic in the low frequency region. Consequently, the novel MCML prescaler has a wider divide range. The maximum divide

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013

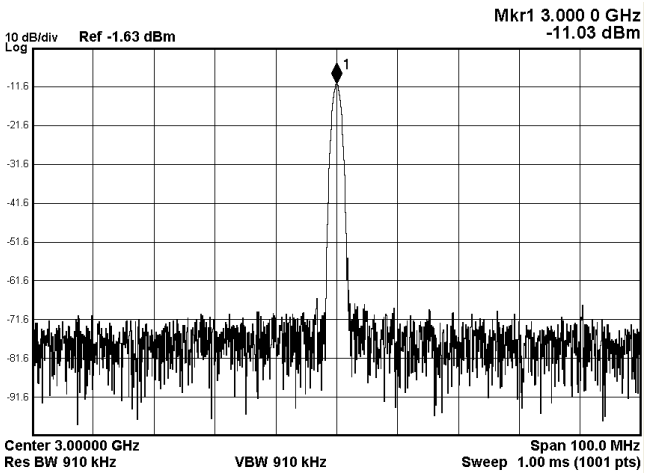

Fig. 7. The output spectrum of the prescaler with current-shaping when operating at 6 GHz

range of the prescaler with the current-shaping technique has a 13.2% improvement compared with the classic one.

4 Conclusion

A current-shaping technique based on a current vector model for static MCML prescalers is presented. This technique improves the self-oscillating frequency merely with two extra capacitors. The prescaler was fabricated in a 0.18-μm CMOS process. Compared with a reference classic prescaler, the one adopting the current-shaping technique acquires 10% and 13.2% improvement in self-oscillating frequency and maximum divide range separately.

DOI: 10.1587/elex.10.20120887
Received November 23, 2012
Accepted December 17, 2012
Published January 22, 2013