ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.13, No.11, 1–10

Dual SPDT/SP3T SOI CMOS switch adopting alternative bias strategy with enhanced performance compared to the conventional case

Zhi-hao Zhang, Gary Zhang, Kai Yu[a)], Jun-ming Lin, Liang Huang, and Zu-hua Liu

School of Information Engineering, Guangdong University of Technology, No.100 Waihuan XiRd, Guangzhou 510006, People's Republic of China

a) *k.yu@gdut.edu.cn*

Abstract: A dual single-pole double-throw (SPDT)/single-pole three throw (SP3T) distribution switch without the employment of negative voltage generator (NVG) for multi-mode multi-band applications has been designed and fabricated in a 0.18 µm silicon-on-insulator (SOI) CMOS process. To reduce power dissipation and prevent the noise from affecting the RF signal, an alternative bias strategy driven only by the positive voltage generator (PVG) is presented. Besides, LC impedance matching network are designed in both series and shunt branch to improve the insertion loss (IL) and isolation, respectively. For comparing the potential performance distinction, a switch version with conventional negative bias method is also implemented, which shows an IL of 0.41/0.65 dB and minimum isolation of 26.9/23.6 dB at 0.9/1.9 GHz, respectively. The presented switch adopting alternative bias scheme achieves improved IL of 0.37/0.53 dB and minimum isolation of 24.2/32.5 dB at 0.9/1.9 GHz, respectively. Both cases reveal comparative power handling capability and harmonic performance, while the active current consumption in the stand-by mode is significantly reduced with the new bias strategy.

Keywords: distribution switch, SOI CMOS, alternative biasing, multi-mode multi-band

Classification: Integrated circuits

References

[1] J.-H. Park: "Fabrication and measurements of direct contact type RF MEMS switch," IEICE Electron. Express **4** (2007) 20070525 (DOI: 10.1587/elex.4.319).

[2] J. Lee, *et al.*: "A low-loss single-pole six-throw switch based on compact RF MEMS switches," IEEE Trans. Microw. Theory Techn. **53** (2005) 3335 (DOI: 10.1109/TMTT.2005.855746).

[3] Z. Gu, *et al.*: "Low insertion loss and high linearity PHEMT SPDT and SP3T switch ICs for WLAN 802.11 a/b/g applications," Radio Frequency Integrated

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

Circuits (RFIC) Symp. (2004) 505 (DOI: 10.1109/RFIC.2004.1320667).
[4] O. C. Shin, *et al.*: "Implementation of new SP6T switch achieving high quality and small size at same time," Asia-Pacific Microwave Conference (2010) 473.
[5] S. Wang and Z.-K. Li: "A 6-32 GHz T/R switch in 0.18-μm CMOS technology," IEICE Electron. Express **9** (2012) 20120325 (DOI: 10.1587/elex.9.590).
[6] M. Ahn, *et al.*: "A High-Power CMOS Switch Using A Novel Adaptive Voltage Swing Distribution Method in Multistack FETs," IEEE Trans. Microw. Theory Techn. **56** (2008) 849 (DOI: 10.1109/TMTT.2008.919047).
[7] P. A. Rabbeni, *et al.*: "RF SOI: Revolutionizing RF System Design," Microw. J. **58** (2015) 20151015.
[8] A. Tombak, *et al.*: "Design of High-Order Switches for Multimode Applications on a Silicon-on-Insulator Technology," IEEE Trans. Microw. Theory Techn. **61** (2013) 3639 (DOI: 10.1109/TMTT.2013.2277989).
[9] J. Cui, *et al.*: "Monolithic Single-Pole Sixteen-Throw T/R Switch for Next-Generation Front-End Module," IEEE Microw. Wireless Compon. Lett. **24** (2014) 345 (DOI: 10.1109/LMWC.2014.2309082).
[10] M. Ahn, *et al.*: "Ultra low loss and high linearity SPMT antenna switch using SOI CMOS process," IEEE Eur. Microw. Conf. (2010) 652.
[11] Z. Zhang, *et al.*: "A novel body self-biased technique for enhanced RF performance of a SP8T antenna switch in partially depleted CMOS-SOI technology," Solid-State and Integrated Circuit Tech. (2014) 596 (DOI: 10.1109/ICSICT.2014.7021253).
[12] K. Yu, *et al.*: "Enhanced ESD power clamp for antenna switch controller with SOI CMOS technology," Electron. Lett. **51** (2015) 871 (DOI: 10.1049/el.2014.4160).
[13] J. Cha, *et al.*: "Analysis and Design Techniques of CMOS Charge-Pump-Based Radio-Frequency Antenna-Switch Controllers," IEEE Trans. Circuit Syst. I, Fundam. **56** (2009) 1053 (DOI: 10.1109/TCSI.2009.2016129).

1 Introduction

Over years, evolving versions of smart phones have supported an increasing number of wireless standards ranging from GSM to LTE, which makes the RF switches the key components in the front-end circuits for enabling multiple frequency bands of operation. Conventionally, a high-throw antenna switch was put at the antenna to connect various RF paths of duplexers and single-band amplifiers. System specifications for 3G and 4G LTE, however, demand the multi-standard band transmit functions, which has given multi-mode multi-band power amplifier modules (MMMB PA) an upper hand in the front end for circuit scheme simplification and chip cost saving. Owing to the multi-band platforms, distribution switches are of great demand to be adopted to route signals both pre-PAs and post-PAs.

Micro-electro-mechanical systems (MEMS) [1, 2], gallium arsenide (GaAs) psuedomorphic high electron mobility transistor (pHEMT) [3, 4], and silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) are three existing technologies suitable for making miniature RF switches. Although MEMS RF switches provide ultra-low insertion loss and high isolation, in which large actuation voltage requirement and special packaging are major drawbacks. The

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

GaAs pHEMT process is attractive due to its low power consumption and high power handling capability, but high control voltage and an extra CMOS-based controller are required. Bulk CMOS technology is limited by its severe lossy substrate and parasitic effect [5, 6]. As the ability to provide lower cost silicon and higher integration potential, SOI CMOS technology has become the most promising and competitive solution for the design of monolithic RF switches [7].

Generally, SOI-CMOS switches integrate a positive-voltage generator (PVG) and negative-voltage generator (NVG) on chip for the bias of the switch-FETs [8, 9, 10, 11, 12]. A charge pump to generate the negative voltage is extremely imperative in the antenna switch module and GSM-based switch applications result from the string requirements of power handling and harmonics distortion. However, a single-pole, double-throw (SPDT) or single-pole, three-throw (SP3T) switch is typically required in band/mode selecting applications depending on the number of 3G and LTE frequency bands supported. In these configurations, the negative biasing scheme will occupy larger switch chip size, cause long start-up time and increase wasteful power dissipation in a stand-by mode. Moreover, the RF signal of those switches which employing NVG will be affected by the switching noise resulted from the charge pump [13].

In this work, based on the chip-size and cost consideration, a dual SPDT/SP3T distribution switch, as shown in Fig. 1, adopting an alternative biasing technique without the employment of NVG for multi-mode multi-band applications has been combined, designed and fabricated in a 0.18-μm SOI CMOS technology. The In1 RF input is connected to one of two switched RF outputs (Out1A or Out1B), whereas the In2 RF input is switched to one of three RF outputs (Out2A, Out2B or Out2C). Switching is controlled by a power supply, VDD, and two control voltage inputs, GPIO1 and GPIO2. Additionally, a conventional negative bias strategy is also utilized for comparison.

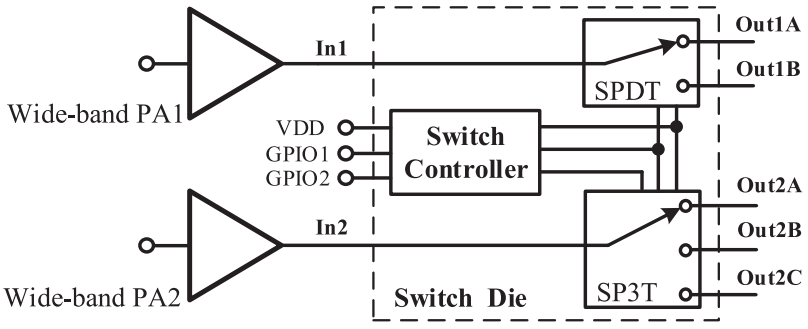


Fig. 1. Block diagram of a multi-mode multi-band front-end module, the presented dual SPDT/SP3T distribution switch is located inside the dotted line.

2 Circuit design and analysis

Fig. 2(a) depicts the conventional switch structure which incorporates a PVG and NVG to generate a positive and negative voltage for biasing switch-FETs. The PVG consists of a bandgap and low dropout regulator (LDO), while the NVG involves an oscillator, non-overlapping clock and charge pump. With the use of PVG and

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

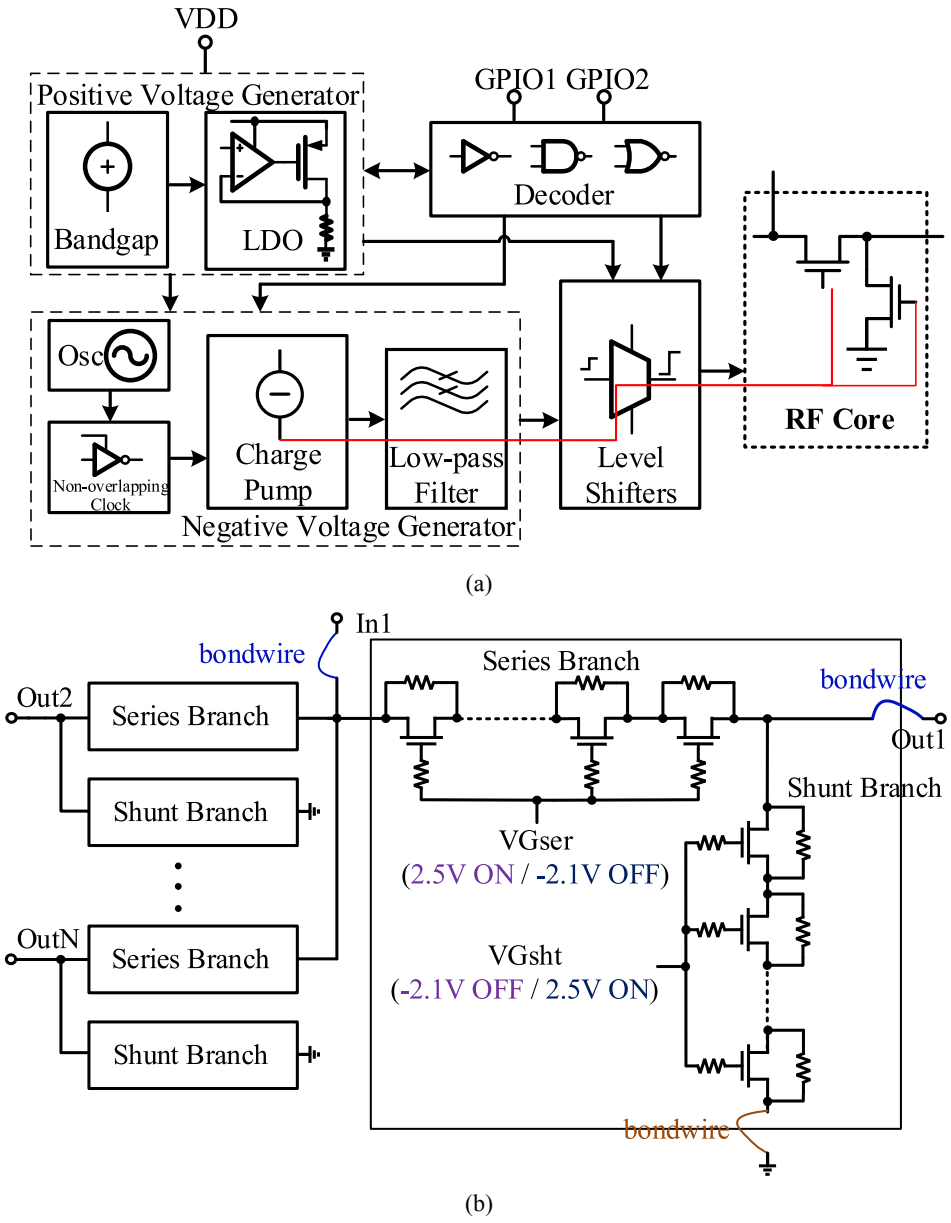


Fig. 2. (a) Conventional switch scheme with NVG; (b) Conventional RF-core circuit

NVG, as shown in Fig. 2(b), the gate voltage of switch-FETs can be biased directly at 2.5 and −2.1 V, respectively, to turn on and off the FETs.

Unfortunately, there are some demerits in the conventional switch configuration that includes NVG. Firstly, the switching noise caused from the charge pump of NVG will definitely affect the spectrum mask of RF signal and sensitivity of switch. Secondly, employing NVG for the low-throw-count distribution switch will occupy a huge area since multiple high-value capacitors and low-pass filters are employed in the charge pump. Furthermore, the parasitic inductance of bone wires will degrade the IL and isolation performance, especially in high-frequency range.

Fig. 3 describes the presented switch topology. This scheme only has the positive voltage, which is produced by the PVG, to be adopted for switch operation. In this case, the switch-FETs cannot be directly turned off due to the absence of the negative voltage. The alternative biasing technique requires extra resistors and

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

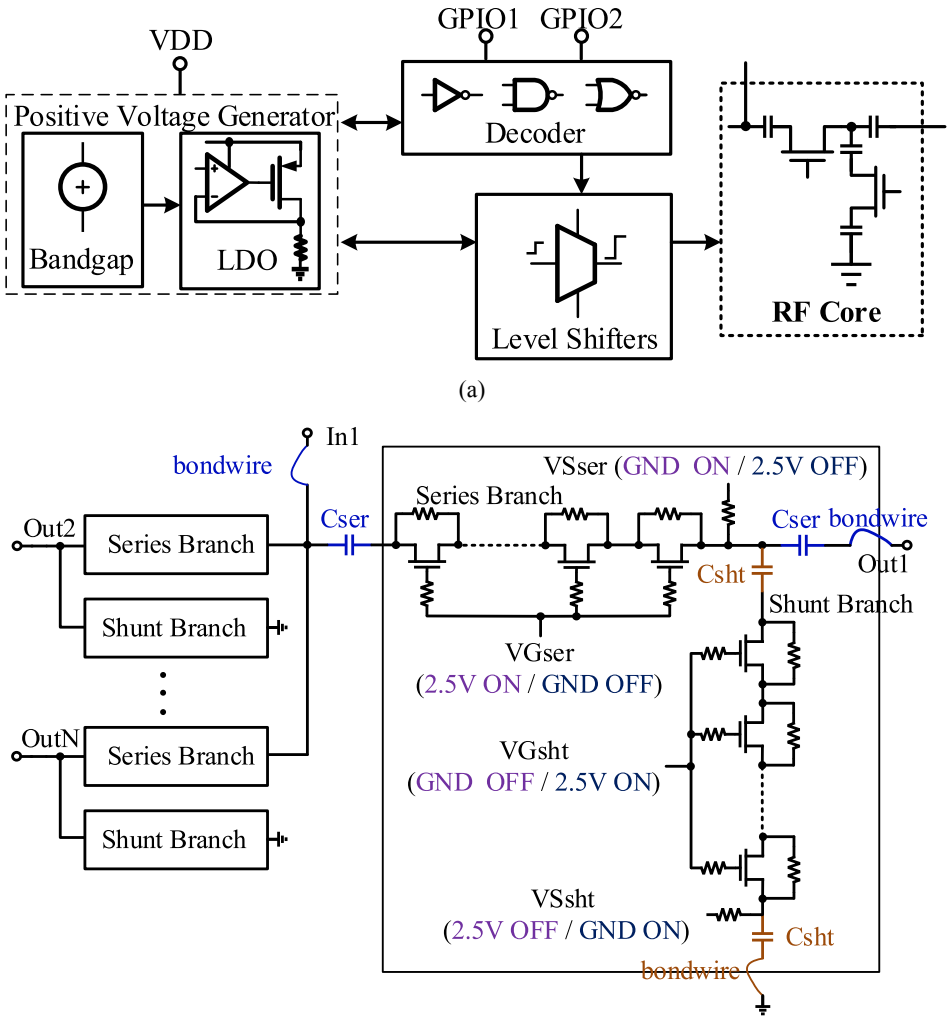


Fig. 3. (a) Presented switch scheme without NVG; (b) RF-core with alternative bias strategy.

supply for the source and drain, as well as additional dc blocking capacitors, C_{ser} and C_{sht}, in the input and output of series and shunt branches, are applied.

Without negative bias strategy, firstly, this configuration can avoid the switching noise derived from the charge pump. Secondly, even though the drawback of the alternative biasing method is the need of additional capacitors, the layout area is still smaller than that of the conventional one due to the remove of the NVG in such low-throw-count distribution switching application. More importantly, the presented scheme helps with IL and isolation improvement by LC impedance transformation network in the series and shunt branch, respectively.

Fig. 4 and Fig. 5 illustrate the simplified equivalent-circuit model of the conventional and presented SPDT for IL and isolation analyses. With $\omega \cdot C_{off} \ll Z_O$, the IL from the RF input, In1, to output, Out1, of Fig. 2(b) and Fig. 3(b), respectively, can be derived as:

$$IL_{con} = 20\,log\left[1 + \frac{R_{on} + \omega L_{t\_ser}}{2Z_o}\right] \quad (1)$$

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

$$IL_{pre} = 20\,log\left[1 + \frac{R_{on} + \left(\omega L_{t\_ser} - \frac{1}{\omega C_{t\_ser}}\right)}{2Z_o}\right] \tag{2}$$

where $L_{t\_ser} = L_{on} + 2L_{wire}$ and $C_{t\_ser} = C_{ser}/2$, where R_{on} is the on-resistance and L_{on} is the on-inductance of the series stacked-FETs in the on-state, and L_{wire} is the equivalent bond-wire inductance to RF port. For Eq. (2), if $\omega L_{t\_ser} - \frac{1}{\omega C_{t\_ser}} = 0$, it can be further expressed as:

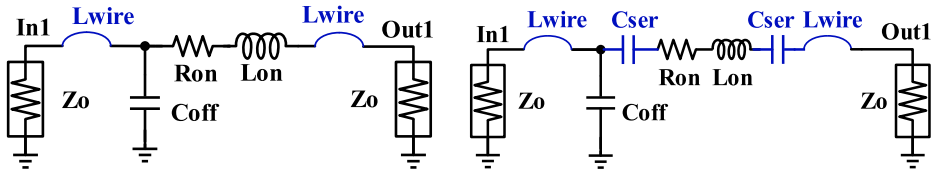
$$IL_{pre} = 20\,log\left[1 + \frac{R_{on}}{2Z_o}\right] \tag{3}$$

Also, the isolation from the RF input, In1, to output, Out1, of Fig. 2(b) and Fig. 3(b), respectively, can be derived as:

$$Iso_{con} = 20\,log\left\{\frac{Z_o}{2Z_{eqs}} + \frac{Z_o\left(\frac{1}{\omega C_{off}} + Z_{eqs}\right)}{2Z_{eqs}\cdot[Z_o\ //\ (R_{on} + \omega L_{wire\_gnd})]}\right\} \tag{4}$$

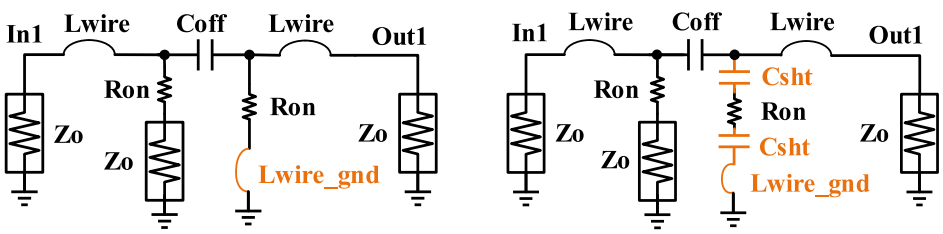
$$Iso_{pre} = 20\,log\left\{\frac{Z_o}{2Z_{eqs}} + \frac{Z_o\left(\frac{1}{\omega C_{off}} + Z_{eqs}\right)}{2Z_{eqs}\cdot\left\{Z_o\ //\ \left[R_{on} + \left(\omega L_{wire\_gnd} - \frac{1}{\omega C_{t\_sht}}\right)\right]\right\}}\right\} \tag{5}$$

where $Z_{eqs} = Z_o\ //\ (R_{on} + Z_o)$ and $C_{t\_sht} = C_{sht}/2$, where L_{wire_gnd} is the equivalent bond-wire inductance to ground. For Eq. (5), while $\omega L_{wire\_gnd} - \frac{1}{\omega C_{t\_sht}} = 0$, it can be further expressed as:



(a) (b)

Fig. 4. Equivalent-circuit model for IL analyses. (a) Conventional; (b) Presented.



(a) (b)

Fig. 5. Equivalent-circuit model for Isolation analyses. (a) Conventional; (b) Presented.

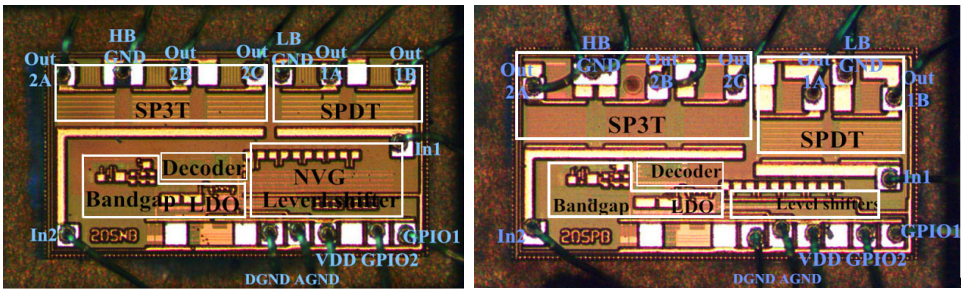
DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

$$Iso_{pre} = 20\,log\left[\frac{Z_o}{2Z_{eqs}} + \frac{Z_o\left(\frac{1}{\omega C_{off}} + Z_{eqs}\right)}{2Z_{eqs}\cdot(Z_o \,//\, R_{on})}\right] \tag{6}$$

As the analysis discussed above, the presented bias strategy is beneficial to IL and isolation optimization due to the impendence mismatching improvement.

3 Implementation and measurement

Fig. 6(a) and (b) show the die microphotographs of these two dual SPDT/SP3T switches with and without negative bias strategy. The conventional switch with negative bias method occupies a chip area of $1300 \times 700\,um^2$, whereas the presented switch adopting alternative bias strategy is with a die size of $1300 \times 650\,um^2$. It's worth noting that even though additional capacitors, C_{ser} and C_{sht}, are set to 11 pF for the low-band and 5 pF for the high-band to optimize the IL and isolation in the presented switch, the layout area is still smaller than that of the conventional one since a NVG, which occupies a large area of $520 \times 144\,um^2$, is not employed in this case. For both cases, the series and shunt arms use 8 stacking devices to satisfy the power level. The width of the stacked FETs in series and shunt arms are optimized as 3.0 and 0.5 mm, respectively.



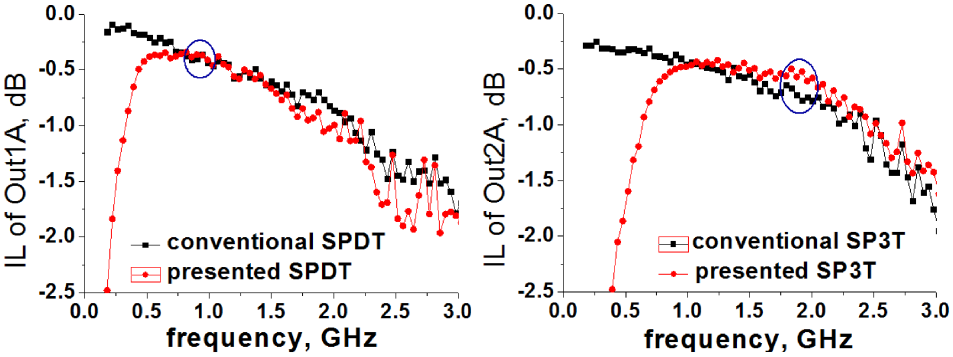
(a) (b)

Fig. 6. Die microphotographs of the dual SPDT/SP3T switches: (a) Conventional one with negative bias strategy; (b) Presented one with alternative bias strategy.

Fig. 7 depicts the comparison of the measured IL of the two dual SPDT/SP3T switches from 0 to 3.0 GHz. For the conventional and presented SPDT cases in the Out1A mode at 0.9 GHz, the IL are of 0.41 and 0.37 dB, respectively, while the IL are of 0.65 and 0.53 dB at 1.9 GHz, respectively, in the Out2A mode for the SP3T cases. The measured data for the low-band are nearly identical in both cases due to the SOI-CMOS process itself can acquire excellence performance below 1 GHz, while the presented switch without employing NVG exhibits around 0.12 dB superior IL, compared to the conventional one, in the high-band since the series bond-wire inductor resonates well with the DC blocking capacitors of series branch among these frequencies.

The tested return loss (RL) are contrasted in Fig. 8. The RL of the conventional SPDT switch varies from 23 to 26 dB for the low band, whereas the presented one

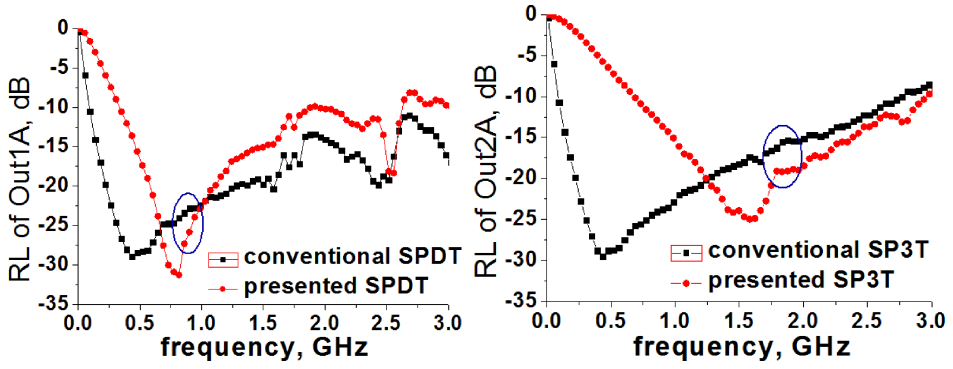
DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016



(a) (b)

Fig. 7. Comparison in IL of dual SPDT/SP3T switches: (a) IL from In1 to Out1A of the SPDT switch; (b) IL from In2 to Out2A of the SP3T switch.

achieves the RL between 24 to 29 dB. For the high band SP3T switch, the tested RL representatively varies from 15 to 19 dB and from 20 to 23 dB, respectively, in these two cases. With the alternative bias scheme, the series bond-wire inductors can be resonated by the DC blocking capacitors of series branch among the operating frequencies, which helps to the impendence mismatching improvement.

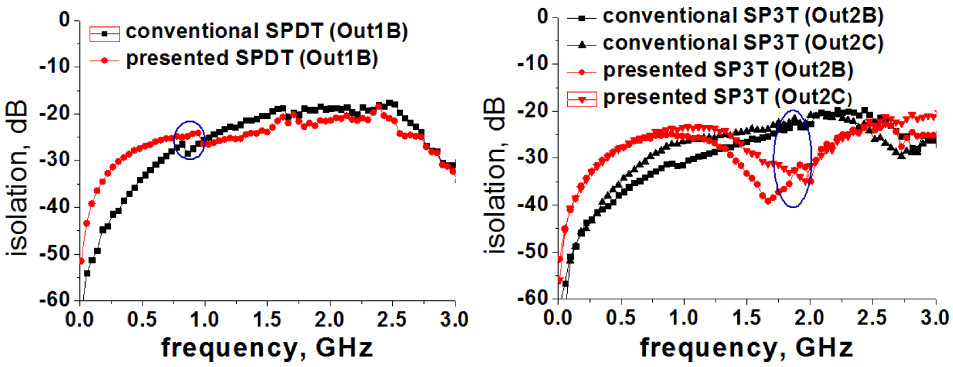


(a) (b)

Fig. 8. Comparison in RL of dual SPDT/SP3T switches: (a) RL from In1 to Out1A of the SPDT switch; (b) RL from In2 to Out2A of the SP3T switch.

The isolation measurements of these two switches have also been compared in Fig. 9. At 0.9 GHz, an Out1A to Out1B isolation of 26.9 and 24.2 dB are achieved for the conventional and presented SPDT cases. At 1.9 GHz from Out2A to Out2B/Out2C, the SP3T switch with and without negative bias strategy obtains the isolation of 25.7/32.6 dB and 23.6/32.5 dB, respectively. It can be well observed that compared with the conventional case with negative bias method, the presented SP3T switch exhibits 9.0 dB superior isolation as the ground bond-wire inductor resonates well with the DC blocking capacitors of shunt branch in the high band. However, the difference is not much pronounced between the two SPDT cases in the low band for the resonance between the bond-wire inductor and DC blocking capacitor is not easy to be achieved in the presented new scheme due to the lower frequency and constrained DC blocking capacitance.

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016



(a) (b)

Fig. 9. Comparison in Isolation of dual SPDT/SP3T switches: (a) Isolation from In1 to Out1A of the SPDT switch; (b) Isolation from In2 to Out2A of the SP3T switch.

A comparison in performance to the two switches is summarized in Table I. Adopting alternative bias strategy reduces the current consumption from 51.4 to 24.2 μA, in contrast to the conventional one with negative biasing scheme. Besides, High $P_{-0.1dB}$ of >30 dBm and Low harmonics of <−50 dBm are achieved for both cases. The presented switch obtains 2nd and 3rd harmonic of −55.2/−50.7 dBm and −60.9/−53.7 dBm with a 28 dBm input power at 0.9/1.9 GHz, respectively, which is slightly worse than that of the conventional case, but the difference is not noticeable. It can be concluded that the switch structure with NVG is good for high-throw-count applications due to its favorable linearity performance and the absence of the extra DC blocking capacitors, but for band/mode selected and low battery-operated switch applications that demand low IL and high isolation, the presented alternative bias strategy that without employing NVG is a better solution.

Table I. Performance comparison of the two switches

Configuration	Conventional case		Presented case	
Switching path	Out1A	Out2A	Out1A	Out2A
Frequency (GHz)	0.9	1.9	0.9	1.9
Insertion loss (dB)	0.41	0.65	0.37	0.53
Return loss (dB)	22.8	15.3	25.8	19.1
Isolation (dB)	26.9[1]	25.7/23.6[2]	24.2[1]	32.6/32.5[2]
$P_{-0.1dB}$ (dBm)	>30		>30	
2nd harmonics (dBm)[3]	−57.3	−51.3	−55.2	−50.7
3rd harmonics (dBm)[3]	−62.6	−54.9	−60.9	−53.7
Chip size (μm²)	1300 × 700		1300 × 650	
Supply current (μA)	51.4		24.2	

[1]The isolation from Out1A to Out1B port
[2]The isolation from Out2A to Out2B/Out2C port
[3]Input power P_{IN} = 28 dBm

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016

4 Conclusion

This work describes a novel dual SPDT/SP3T SOI CMOS band switch using alternative biasing scheme. With LC impedance transformation network achieved in this configuration, low IL of 0.37/0.53 dB and high isolation of 24.2/32.5 dB at 0.9/1.9 GHz are obtained by the presented new switch scheme with a small size of $1300 \times 650\,um^2$ and a low dc supply current of 24.2 μA. The presented structure without negative voltage generator is extremely suitable to the design of distribution switches for 3G/4G multimode multiband applications.

Acknowledgments

This work was supported by National Natural Science Foundation of China (Grant 61574049 and 61404032), Leading-Talent Specific Foundation of Guangdong Province, China (Grant 400130002), Pearl River Nova Program of Guangzhou (Grant 201506010090), and Guangdong Innovative Research Team Program (Grant 2014ZT05G157). The authors also would like to acknowledge China Scholarship Council (CSC).

DOI: 10.1587/elex.13.20160322
Received March 31, 2016
Accepted April 7, 2016
Publicized May 13, 2016
Copyedited June 10, 2016