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Evaluating the single event sensitivity of dynamic comparator in 5 Gbps SerDes

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Abstract: The radiation induced soft error of dynamic comparator for a 65 nm CMOS technology in 5 Gbps half-rate SerDes (serializer and deserializer) is evaluated using three-dimensional TCAD mixed-mode simulation. The sensitivity of MOSFET is simulated combined with the polarity of differential inputs and the working phases. Four types of single-event (SE) response are classified and the sensitivity grades are summarized. Our research presents that the NMOS of the cross-coupled inverter is the most sensitive.

Keywords: dynamic comparator, SE sensitivity, LET threshold, sensitive window rate

Classification: Integrated circuits

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1 Introduction

With the rapid development of integrated circuits, the system on chip (SOC) has been used widely in the aerospace system. In the SOC, the serializer and deserializer (SerDes) is the key component for the different components to realize high-speed transmission between each other. At present, the radiation induced soft errors of the SerDes has become a great concern, and the single event transient (SET) in analog circuits of SerDes such as differential amplifier and bias circuit is researched widely [1, 2, 3].

Comparator is also known as samples and is one of the speed-limiting circuits in SerDes whose date rate is up to several Gbps ~ tens of Gbps [4, 5]. The error of comparator is fateful to the bit error rate (BER) of the whole system which is normally below 10^{-12}, and has influence on the jitter of recovering clock [6]. In general, comparator can be classified into static comparator and dynamic comparator. There are many works about single event sensitivity in static comparator [7, 8] which indicate SET is a great threat to the sampling result. However, the work about single event sensitivity in dynamic comparator is limited, though dynamic comparator is more attractive comparing to static comparator due to its faster speed profited from cross couple structure and lower power profited from the clock controlling [9, 10].

Wang et al. evaluated the single-event transient effects of the dynamic comparators in different well technologies designed with a 90 nm CMOS process [11] and showed that vulnerability was a strong function of technology. But his research is lack of attention on the polarity of differential inputs, the working phases and the SE relationship between striking moment and clock edge. Other studies on dynamic comparators focus on larger input swing, lower operating voltage, and so on which are not related to single event [12, 13, 14].

In this paper, based on three-dimensional technology computer-aided design (TCAD) numerical simulations, the single event sensitivity of a dynamic comparator in a 5 Gbps SerDes designed with 65 nm bulk technology is researched. Both the incident ion energy and the phase difference between clock and SET are considered to evaluate the effect of SET in each transistor. The single event sensitivity of each transistor is discovered, and the effect of phase difference is also under research.

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2 Circuit structure

Fig. 1 shows the circuit structure of the dynamic comparator which is under study in a certain 5 Gbps half-rate SerDes. The clock frequency can be up to 2.5 GHz. As shown in Fig. 1, the bilateral symmetry circuit has differential structure with input transistors pair N2 and N3. The transistor P0, P1, P2 and P3 are the precharge transistors, and the N0-P4 and N1-P5 are the cross-coupled inverters.

The working principle of the dynamic comparator includes precharge and evaluation phases. In precharge phase, the precharge transistors are turned on by clk. The node vop and vom will be precharged to HIGH. Then in evaluation phase, the precharge transistors are turned off and it will come into strong positive feedback once the difference between vi_p and vi_m exists. The output stabilizes quickly.

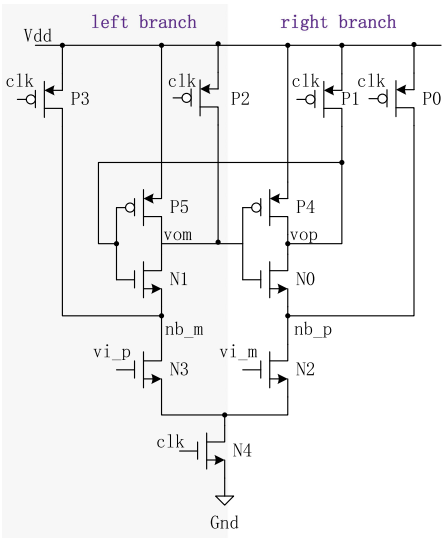

Fig. 1. Schematic of dynamic comparator.

In this circuit, the supply voltage is set to 1.2 V. The input common-mode voltage is 730 mV and the differential-mode voltage is 300 mV. What's more, the clk is set to 2.5 GHz, which means the clock period is only 400 ps. Geometry size parameters are listed in Table I.

3 Simulation setup

In this section, the three-dimensional TCAD mixed-mode simulation is adopted to investigate the SE sensitivity of the dynamic comparator in Fig. 1. The layout structure of this structure is implemented by using the commercial 65 nm CMOS process as shown in Fig. 2(a). The size of each transistor is set according to Table I. Table I shows that the width of transistors is much larger than the one in digital standard cell library.

For the mixed-mode simulation, the studied transistors are modeled as the TCAD model acquired from Synopsys Sentaurus Device Version E-2010.12, and other transistors are modeled as the corresponding 65 nm SPICE models. For instance, as shown in Fig. 2, it is assumed the transistors N1 would be studied.

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Table I. Size of the transistors for the comparator

Transistors	Width (um)	Length (um)
P1,P2	3	0.06
P0,P3	2	0.06
P4,P5,N0,N1	3.6	0.06
N2,N3	4	0.08
N4	3	0.06

Thus, the transistor N1 will be modeled as the TCAD model. The other models are the SPICE models.

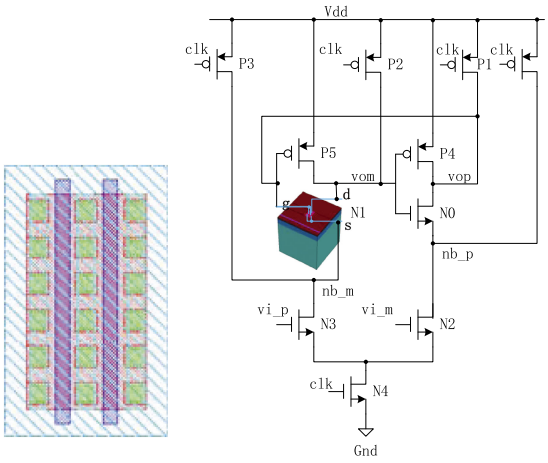

Fig. 2. Three-dimensional TCAD mixed-mode simulation setup. (a) layout, (b) the mixed circuit with N1 modeled as TCAD device.

There are 11 transistors in this dynamic comparator including one NMOS at the bottom of the circuit sharing by left and right branch simultaneously. Combined with the polarities of differential input and the working phases, there are 44 cases ($2 \times 2 \times 11 = 44$) to be simulated. As the circuit in Fig. 1 is symmetrical, we only evaluate the single-event sensitivity of the transistors on left branch of the comparator. The simulated cases can be described in Table II. It can be predicted that the transistors on right branch has the same sensitivity as the corresponding transistors on the left.

All simulations are conducted with normal strike on the drain center of the TCAD numerical model under 2.5 GHz. During the simulations, the LET value of incidence ions is varied from 5 MeV-cm^2/mg (LET5 for abbreviation) to 30 MeV-cm^2/mg (LET30 for abbreviation, similar to the following). The following physical models are adopted: Fermi-Dirac statistics, band-gap narrowing effect, Auger recombination, and doping dependent, etc. Unless other specified, the default models and parameters provided by TCAD tool are used. This is consistent with other previous works in our researching group [15, 16, 17].

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Table II. Simulated cases

Polarities of Differential Input	Working Phases	Simulated Transistors
vi_m is higher than vi_p	Precharge phase	P2, P3, P5, N1, N3, N4
	Evaluation phase	P2, P3, P5, N1, N3, N4
vi_p is higher than vi_m	Precharge phase	P2, P3, P5, N1, N3
	Evaluation phase	P2, P3, P5, N1, N3

4 Simulation results

4.1 vi_m is higher than vi_p

4.1.1 Precharge phase

For the precharge phase, the clk is in low half cycle. And the node vom, vop, nb_m as well as nb_p will be precharged to HIGH. Fig. 3(a) shows the cases as the incident ion strikes transistor P5 at 540 ps. It can be noted that there exists overshooting voltage at node vom, and no error occurs in evaluation phase. The results are similar when ion strikes on other PMOS transistors. The PMOS under this case is of the highest single event immunity.

However, when ion strikes on N1 at the same moment, the error occurs as shown in Fig. 3(b). The effect of ion strike extends to evaluation phase and causes error. In this case, the charge has no enough time for depletion on the condition of 2.5 GHz whose effective time is half cycle, about 200 ps. In fact, the depletion will occupy orders of hundreds of picoseconds. The imbalance charge between left branch under strike and right branch free of strike leads to that the voltage of vom is lower than the one of vop at the end of precharge phase. When the circuit comes into evaluation phase, the following strong positive feedback is disturbed. As a result, the voltage of vop is higher than the one vom at the end of evaluation phase which is not as expected. We call this as transfer error. Therefore, N1 is more sensitive than P5.

Another simulation shows there is no transfer error when energy is decreased to LET10 at 540 ps, but the result may be changed as striking time changes. In order to evaluate its temporal correlation, we adjusts the strike time from 540 ps to 700 ps with an interval of 40 ps for each step. Table II shows that there is no error when hitting at 540 ps and 580 ps, but error occurs as striking time is 620 ps, 660 ps, and 700 ps. In order to weight its tolerance considering the strike time, sensitive

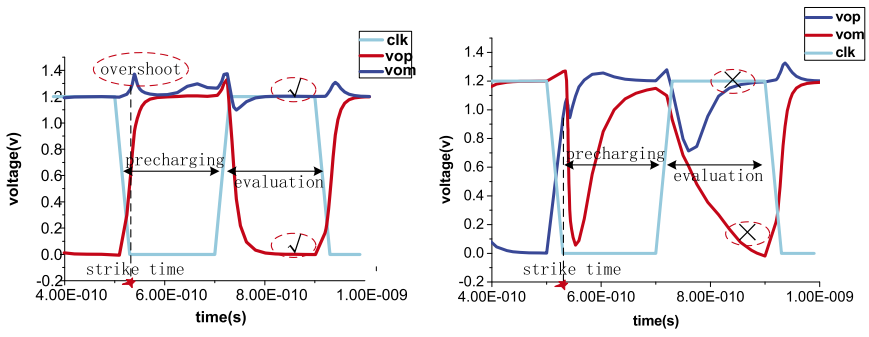

Fig. 3. Waveform when hitting happens in precharge phase. (a) no error with ion striking on P5 with LET15, (b) error with ion striking on N1 with LET15.

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window ratio is introduced in this paper. It is defined as the timing segment which has error under striking divided by the precharge period. Taking the data on Table III for example, the sensitive window ratio at LET10 is calculated as following. The precharge period is 200 ps when clock frequency is 2.5 GHz, the sensitive window ratio is 60% that is (700 ps − 580 ps)/200 ps. As can be seen, this type error on NMOS depends on not only the LET value but also the strike time. As the data rate reduces in SerDes, the frequency of dynamic comparator is decreased. Sensitive window ratio will also be decreased because the time for the ionization charge to deplete is longer.

Table III. Correctness of the comparator with ion striking on N1 in precharge phase varying strike time (LET10)

strike time	540 ps	580 ps	620 ps	660 ps	700 ps
√/× in evaluation phase	√	√	×	×	×
sensitive window ratio	60%				

The sensitivity of N3 and N4 on the same branch is also under consideration. The results are illustrated in Table IV together with N1. It indicates that the SE sensitivity of N1 is the highest among NMOS transistors. LET10 which can result in error on N1 cannot generate error on N3 and N4. This is owing to that N1 has the nearest path to the output node shown in Fig. 2(b). Combined with Fig. 4 which shows the disturbance of vom with LET15, it can be got that N4 has the weakest sensitivity. This is due to that N4 is the tail transistor which has the same influence on left and right branch, and N4 is the farthest transistor away from the output.

Table IV. Correctness of the comparator with ion striking on NMOS in precharge phase (540 ps)

	N1	N3	N4
LET10	√	√	√
LET15	×	√	√
LET20	×	√	√
LET25	×	√	√

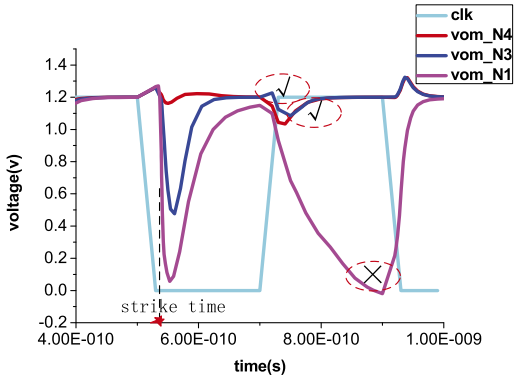

Fig. 4. Waveform of vom with ion striking on NMOS with LET15.

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4.1.2 Evaluation phase

Table V lists the correctness of the comparator when ion strikes on N1 with different LET values in evaluation phase. For ease of comparison, the correctness of the comparator when ion strikes on N1 in precharge phase is also listed. Compared with precharge phase, strike in evaluation phase can affect the output more directly and quickly. There is no error in both phases when LET value is 5 MeV-cm^2/mg. When LET value increases to 10 MeV-cm^2/mg, error occurs in evaluation phase but no error occurs in precharge phase which shows that the LET threshold of evaluation phase is lower than that of precharge phase. The striking on N1 lowers down vom and locks vop to HIGH through cross coupling which is completed less than 30 ps observed from simulation. As the output stabilizes quickly, the sensitive window ratio is ignored during evaluation phase. Strike on N3 or N4 has no effect on the output because it just causes undershooting voltage on the drain of NMOS. Besides, the PMOS on this case is also SEU immune and just brings overshooting voltage.

Table V. Correctness of the comparator with ion striking on N1 in precharge (540 ps) and evaluation phase (800 ps) varying LET

	precharge phase	evaluation phase
LET5	√	√
LET10	√	×
LET15	×	×
LET20	×	×

Totally, the NMOS in cross coupling pair is more sensitive when vi_m is higher than vi_p, while the NMOS which is far away from output node is less sensitive. The strike time in precharge phase is more sensitive than that in evaluation phase. The PMOS is immune to ion strike.

4.2 vi_p is higher than vi_m

4.2.1 Precharge phase

For precharge phase, when the ion strikes on any NMOS transistor, the voltage in node vom is disturbed as shown in Fig. 5. However, vom is still correct in the following evaluation phase because vom should be low even without hitting. What's more, the transition rate of vom in evaluation phase is faster compared to the one without hitting.

When ion strikes on any PMOS transistor in precharge phase, it only induces overshooting on node vom and has no effect on the correctness of node vom and vop in the following evaluation phase as shown in Fig. 6.

The simulation result of NMOS and PMOS on this case is shown in Table VI. Under this circumstance, all MOSFETs are immune to ion strike.

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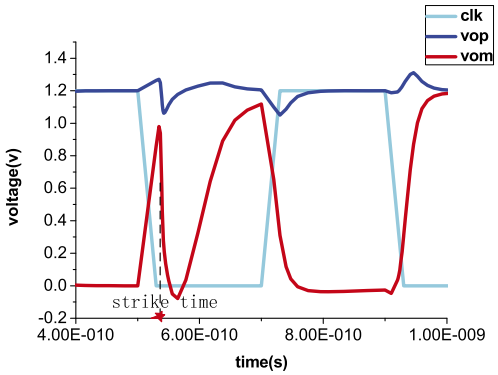

Fig. 5. Waveform with ion striking on N1 in precharge phase with LET20.

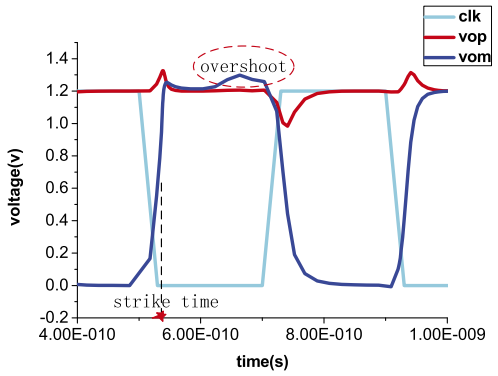

Fig. 6. Waveform with ion striking on P5 in precharge phase with LET15.

Table VI. Correctness in precharge phase varying LET (540 ps)

	LET15	LET20	LET30
NMOS	√	√	√
PMOS	√	√	√

4.2.2 Evaluation phase

For the evaluation phase, the ion strike on NMOS transistor only accelerates vom from HIGH to LOW. No error occurs.

When ion strikes on P5, the waveform is shown in Fig. 7. Although vom and vop are disturbed seriously, they have the same direction and vop is still larger than vom. Other PMOS-strike has similar result.

The reason can be explained as follows: before ion strikes, the nodes of the cross-coupled inverters are stable. The node vom is LOW and the source of N0 is HIGH. As ion strike happens, V_{GS} (vom - nb_p) of N0 is increased, but $V_{GS} \geq V_{TH}$ still cannot be met and N0 keeps turnoff. As the depletion of charge goes on, vom resumes towards LOW. Under this case, vom and vop have the shortage of no-full swing. This disadvantage can be compensated on next dynamic comparator or buffer. For the extreme case, when ion strike occurs closely to the next clock edge,

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the error cannot be avoided. In general, when vi_p is higher than vi_m, most MOSFETs are not sensitive to ion strike.

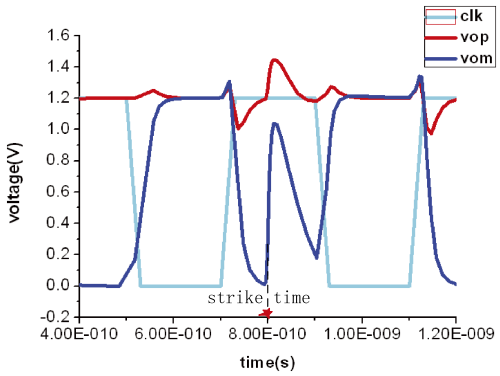

Fig. 7. Waveform with ion striking on P5 in evaluation phase (800 ps, LET15).

5 Discussion

The single-event sensitivity of the dynamic compactor is summarized in this section. According to the symmetry of dynamic comparator, we just investigated half cases of all the cases on left branch and situation is similar on right branch. The response is related with the polarity of inputs, ion strike position, strike time and LET value. The various responses under ion strike are classified into four types according to the severity as shown in Table VII.

Table VII. Correctness in precharge phase varying LET (540 ps)

No.	Responses	Severity	Corresponding section
type1	Overshooting or undershooting without error	weak	PMOS in section 4.1 N3,N4 in section 4.1.1 PMOS in section 4.2.1
type2	disturbance without error	weak	NMOS in section 4.2.1 PMOS in section 4.2.2
type3	direct error	strong	N1 in section 4.1.2
type4	transfer error	medium	N1 in section 4.1.1

Tpye1 and type2 will not result in an error and have the weakest influence. Type3 means hitting on N1 MOSFET in evaluation phase with higher vi_m. It has direct error and has lower LET threshold compared to the precharge phase. Type4 is most complicated and may generate transfer error which spans from precharge to evaluation phase and is sensitive to the LET value and strike time. The SE sensitivity about strike time can be weighted by the sensitive window rate which is closely related with the clock frequency. As the frequency of dynamic comparator goes up, sensitive window rate will be increased.

In addition, it can be concluded that NMOS in cross-coupled circuit is most sensitive and can generate error in both precharge and evaluation phase. As to the

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LET threshold, it is lower in evaluation than in precharge phase. Other NMOS has less sensitivity because they are far away from the output node.

6 Conclusions

In this paper, the radiation sensitivity of high speed dynamic comparator is analyzed carefully by considering the polarity of differential inputs and working phases in this paper. The three-dimensional TCAD mixed-mode simulations present that there are four types of responses for an ion strike. Among them, the most sensitive part is NMOS in the cross-coupled inverters with the sensitive elements involving both LET threshold and the sensitive window, and it can cause direct error in evaluation phase. The weak types only arouse overshooting/undershooting or disturbance without error on outputs. The result in this work can be used as a reference for analyzing and hardening SerDes and other high-speed A/MS circuits.

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