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A high gain, wide-band, fast settling amplifier with no-miller capacitor compensation

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Abstract: A high DC gain, wide band and fast settling fully differential amplifier is presented. The pole zero cancellation technique is used in order to increase the band width of the OTA. Also, a new technique for pole zero cancellation in three-stage OTAs is presented. The proposed OTA simulated in standard TSMC 0.18 μm CMOS technology with a 1.8 V power supply. The DC gain of the OTA is 85 dB, the unity gain band width is 740 MHz and the phase margin of 60 degree is achieved. The amplifier consumes only 18.8 mW.

Keywords: operational trans-conductance amplifier (OTA), frequency compensation, sample and hold (S/H)

Classification: Integrated circuits

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1 Introduction

Operational Trans-conductance Amplifiers (OTAs) are among the most important building blocks of analog integrated circuits. The design of an OTA with high DC gain, wide band width and fast settling time is always a challenging problem. Because of decreasing the channel length of the MOS transistors in new technologies, reaching to high DC gain in single stage amplifiers has been very difficult. Therefore, for reaching to high DC gain, amplifiers with more than one stage are used [1, 2, 3]. Increasing the gain of the amplifier by increasing the number of stages has some problems, such as stability and power consumption. Adding more stages in cascade with each other introduces more than one dominant low frequency pole because of the existing high impedance nodes in the output of stages. One of the most common ways to compensate the two-stage amplifier is the "Miller" technique [1]. In this method of compensation, a low frequency pole is generated by placing a miller capacitor across the second gain stage. A similar method is used for compensating three-stage OTA which is called "Nested Miller compensation" [2]. Another method of frequency compensation is explained in [4]. In this method, an AC path is used to stabilize the amplifier. Also the additional path improves the unity gain band width and slew rate of the OTA. All of the discussed methods of compensation use a capacitor in such a way to create a dominant pole or to split the poles in order to increase the phase margin of the OTA and make it stable. But adding a capacitor to the circuit not only increases the area but reduces the slew rate of the circuit. Therefore it is interesting to use a way to compensate the OTA without using any capacitor. The Non-capacitor compensation technique [5] is used in this paper to propose a new structure of frequency compensation which is expressed in details in the next section.

2 No capacitor feed-forward compensation

One of the interesting methods of compensation is presented in [5] which use no Miller capacitor to compensate the OTA. Fig. 1 a shows the feed forward frequency compensation method proposed in [5]. In this type of compensation, the input signal passes through two paths. In the first path

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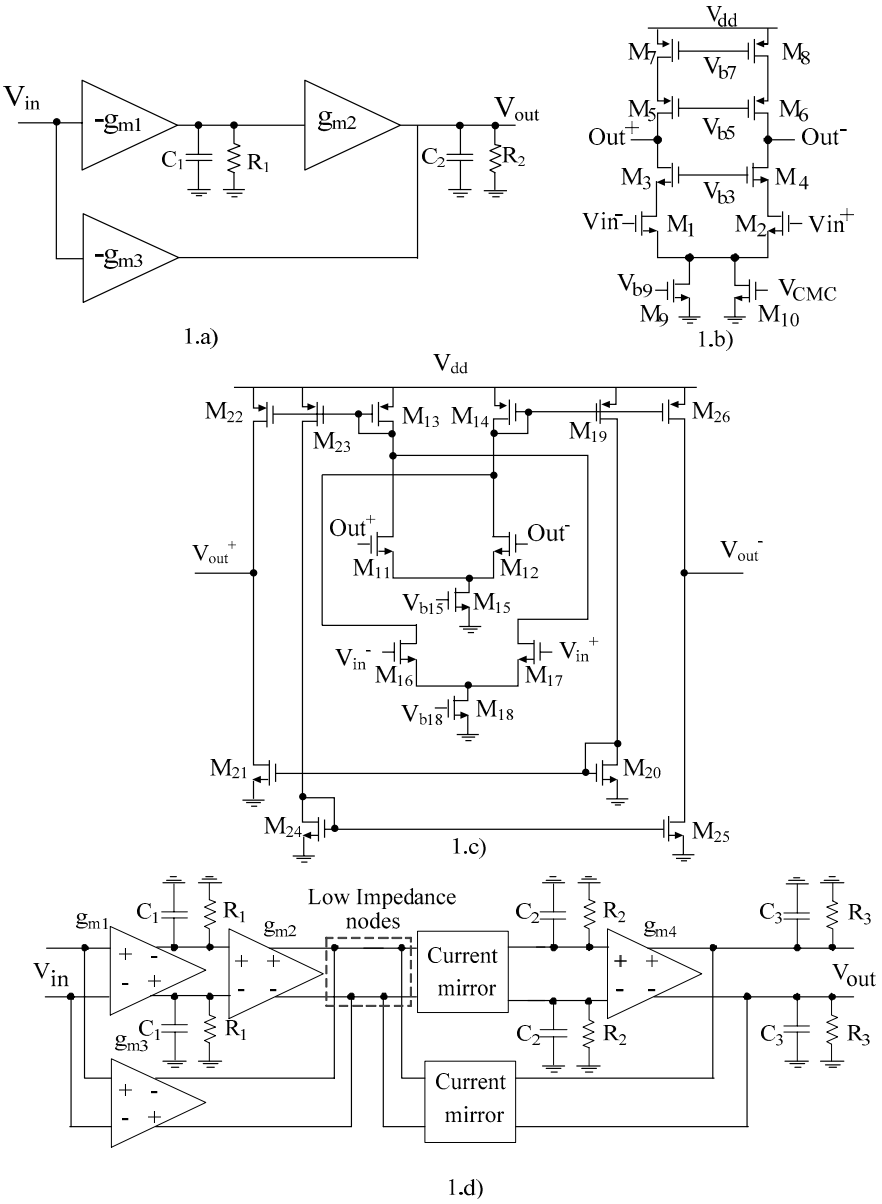

Fig. 1. a) Proposed amplifier structure, b) first stage implementation, c) second and feed-forward stage implementation, d) Generalized architecture for the increased number of stages

the signal is significantly amplified amplified through g_{m1}, g_{m2} as shown in Fig. 1 a. The second path is the high speed path in which the signal passes from input directly to the output through g_{m3}. Using this architecture leads to a dominant pole at the output of the first gain stage (g_{m1}) and a non-dominant pole at the output of the amplifier. The OTA has also a left half plane (LHP) zero which is made by the feed forward path (g_{m3}) from input to the output of the amplifier. The pole zero cancellation technique which is presented in [6] is used to cancel out the second pole by the LHP zero in order to increase the phase margin and the band width of the amplifier. In order to optimize this method of compensation, the pole zero cancellation should occur at high frequencies according to [6]. The open loop transfer

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function of the amplifier is given in (1).

$$\frac{V_o(S)}{V_{in}(S)} = -\left(g_{m3} + g_{m2}\frac{g_{m1}R_1}{1+R_1C_1S}\right)\left(\frac{R_2}{1+R_2C_2S}\right). \quad (1)$$

According to (1), the system has two poles and one zero. The frequency of the poles and zero are given in (2), (3) and (4) respectively.

$$\omega_{p1} = \left(\frac{-1}{R_1C_1}\right). \quad (2)$$

$$\omega_{p2} = \left(\frac{-1}{R_2C_2}\right). \quad (3)$$

$$\omega_z \approx \left(\frac{-g_{m1}}{C_1}\right) \times \left(\frac{g_{m2}}{g_{m3}}\right). \quad (4)$$

Where R_1 and R_2 are the output impedances of the first and the second stages, the g_{m1}, g_{m2} and g_{m3} are also the trans-conductance of the first, the second and the feed-forward stages respectively. It can be seen that the second pole can be canceled out by the LHP zero. The pole zero cancellation cannot occur at a specified frequency. Nevertheless, this compensation method is not very sensitive to the difference between frequencies of second pole and zero [5].

3 Circuit level design

In order to design an OTA with less sensitivity to common mode signals than single ended structures, the fully differential architecture has been selected. As can be seen in Fig. 1 a, the input stage (g_{m1}) amplifies the signal and the second stage (g_{m2}) amplifies the signal again. Therefore, the voltage swing at the output of the first amplifier (g_{m1}) is not very large. So, a high gain and low speed amplifier can be used as the first stage. The telescopic cascode amplifier can be the best candidate for the first stage as shown in Fig. 1 b. To increase the output impedance of the first stage it should be biased by a very low current density. Meanwhile, the output capacitance of the first stage is the input capacitance of the second stage; therefore the first stage must load very small capacitance and as a result, the slew rate of the first stage is not a limiting parameter of the whole circuit. A common mode feedback (CMFB) circuit is necessary to adjust the output DC voltage of the first amplifier. The switched capacitor CMFB circuit is a good choice if the OTA is used in a switched capacitor application. The M_9 in Fig. 1 b is used as the tail transistor to set the bias point of the circuit and M10 close the CMFB loop by changing the transistors bias current.

The voltage gain of the first stage will be as (5).

$$A_{v1} \approx g_{m1}(g_{m4}r_{o4}r_{o2}||g_{m6}r_{o6}r_{o8}). \quad (5)$$

The second and feed-forward stages are designed, such that the speed of these two stages need to be high enough not to produce any undesirable pole within the unity gain band width of the total amplifier. High current density is used for these two stages to increase the speed and the slew rate of the total amplifier.

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The voltage gain of these two stages is not necessary to be high; therefore all the transistors are used with minimum channel length size. The circuit of the second and feed-forward stages are shown in Fig. 1 c. The voltage gains of the second and the feed-forward stages are given in (6), (7) respectively.

$$A_{v2} = g_{m11}\left(\left(\frac{(W/L)_{22}}{(W/L)_{13}}\right) + \left(\left(\frac{(W/L)_{19}}{(W/L)_{14}}\right)\left(\frac{(W/L)_{21}}{(W/L)_{20}}\right)\right)\right) R_{out}. \quad (6)$$

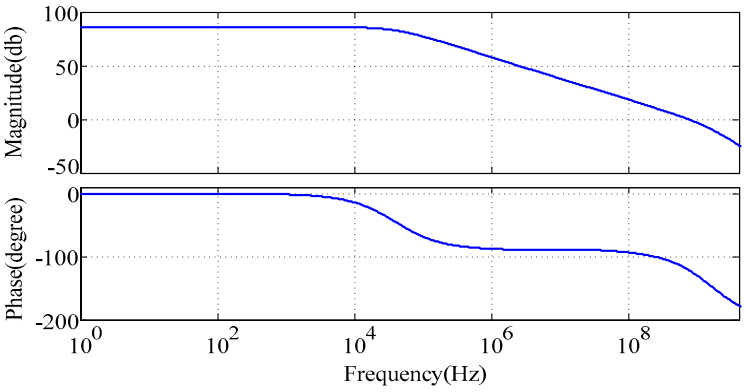
$$A_{v3} = g_{m17}\left(\left(\frac{(W/L)_{22}}{(W/L)_{13}}\right) + \left(\left(\frac{(W/L)_{19}}{(W/L)_{14}}\right)\left(\frac{(W/L)_{21}}{(W/L)_{20}}\right)\right)\right) R_{out}. \quad (7)$$

In which, R_{out} is the output impedance which is equal to, $r_{o22}||r_{o21}$.

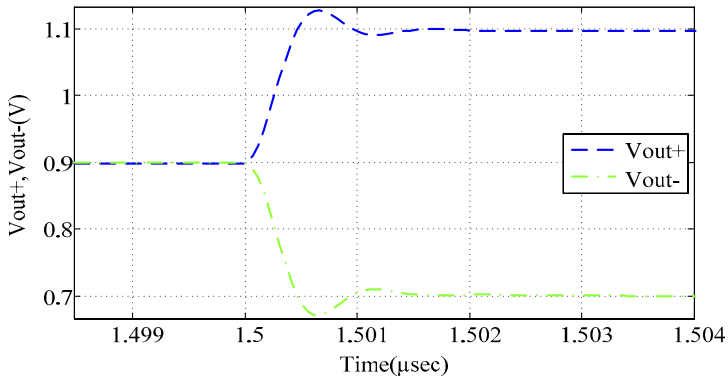
Generalized architecture for designing high-DC gain, wideband OTA is shown in Fig. 1 d for 3stage structure. In this structure, the pole zero cancellation occurs in each two consecutive gain stages and therefore the circuit can be designed very easily in comparison to the method that is explained in [5].

4 Simulation results

The explained stages in Figs. 1 b, 1 c are placed next to each other according to Fig. 1 a to form the total amplifier. The total OTA is simulated with standard TSMC 0.18 μm CMOS technology with 1.8 V power supply using the Hspice circuit simulator. The output common mode voltage is set to 0.9 V



(a)



(b)

Fig. 2. a) Frequency response of the amplifier, b) the step response of the OTA in sample and hold structure

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Table I. Specification comparison of the designed OTA with recent designs

	Gain (dB)	BW (MHz)	C_L (pf)	Power (mW)	V_{DD} (V)	Settling Time (nsec)
[5]	94	300	12	15.8	2.5	20
[7]	100	100	100	76	8	60
[8]	102	47	40	6.9	3	100
[9]	86	392	2	12	1.8	15
[10]	80	20	1	0.57	1.5	50
This Work	85	738	8	18.84	1.8	3.5

to increase the output voltage swing. The frequency response of the OTA as the Bode diagram is shown in Fig. 2 a. The Bode plot of the system shows that the system is stable with a phase margin of about 60° which is suitable for fast settling applications. It can be seen that the pole zero cancellation has less effect on the frequency response of the system and its Bode diagram is the same as a simple two-pole system.

In order to verify the speed of the circuit, the OTA is used in a sample and hold structure. A sampling capacitor is 2 pF and a load capacitor of 8 pF is used. The input voltage is a 0.2 V step signal. The output step response of the sample-and-hold is shown in Fig. 2 b. The positive and negative outputs settled in about 3.5 nsec with 0.1% error which shows the fast response of the circuit.

Table I compares this OTA with some other published OTAs.

5 Conclusion

A high-gain wideband and fast settling amplifier without using miller capacitor for frequency compensation was presented. The pole zero cancelation technique was used to increase the band width of the OTA. A new method of increasing number of stages was proposed which is very robust for implementation. The simulation results showed that this method of compensation can be used for wideband application. Also the good settling time of the OTA makes it a very good candidate for many switched capacitor circuits.

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