

The stability of adiabatic reversible logic using asymmetric tank capacitors and its application to SRAM

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Abstract: The stability of adiabatic stepwise charging reversible logic is discussed. In the case of adiabatic logic with asymmetric tank capacitors, we derive a matrix which connects the initial state and the final state after the charge-recycle process. From the analytical discussion, it is proved that the absolute value of the eigen value of the matrix is less than 1. Therefore, it is shown that a step waveform is spontaneously generated after many charge-recycle processes. Next, an adiabatic stepwise charging SRAM is proposed. The SRAM is immune to hot-carrier effects and electromigration even in the less-than-45-nm process, while it maintains an operating voltage of 1 V or more. The SRAM is suitable for nanoscale circuits.

Keywords: adiabatic reversible logic, tank capacitor, SRAM, nanocircuit

Classification: Electron devices

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1 Introduction

Nanoscale devices have been widely researched [1, 2, 3, 4] for large-scale integration. In CMOS technology, the 45-nm process is being researched and 10-nm node might become possible in future. Reducing the operating voltage V_{DD} according to the scaling law is very difficult because the threshold voltage V_{th} of a transistor can not be decreased due to the leakage current and V_{th} variation. Therefore, it has been proposed that V_{DD} should be kept at 1 V or more for low-power-consumption SRAM [5]. In this case, as the size of transistors is reduced, the electric field in them increases and the source-drain current I_{ds} increases. This leads to several problems, such as hot-carrier effects and electromigration. Adiabatic logic has been researched mainly for low-energy operation [6]. However, it has another important role: its quasi-static operation could offer a highly reliable SRAM that is immune to those problems in a less-than-45-nm-process circuit. Adiabatic logic using a switched capacitor regenerator with symmetric tank capacitors has been shown to be very stable [6, 7]. In this letter, the stability of adiabatic logic using asymmetric tank capacitors is shown. From this result, it is clearly shown that adiabatic logic using the switched capacitor regenerator is not analog but something like a digital circuit. Next, an adiabatic SRAM circuit and its operation method are proposed, and it is shown that the adiabatic SRAM is very suitable for nanocircuits.

2 Stability of adiabatic logic with asymmetric capacitors

The switched capacitor regenerator with asymmetric capacitors and its timing chart are shown in Figs. 1 (a) and (b), respectively. V_{Ci} is the voltage of the tank capacitor C_i . C_1 , C_2 , and C_3 are 100, 50, and 400 pF, respectively. Load capacitance C_L is 2 pF. Simulation results are shown in Fig. 2. For the simulation, switching transistor resistance was 1 k Ω . The period of a four-step waveform cycle was 1 μ s, which means operating speed was 1 MHz. V_{DD} was 5 V and the initial V_{Ci} was set to 2.5 V. After 400 μ s, V_{Ci} becomes $i/4 \cdot V_{DD}$, spontaneously. From this result, it is clear that the operation of the switched capacitor regenerator is not dependent on C_i , so that this circuit is not analog but close to digital.

Next, we investigate the reason for the stability analytically. When trans-

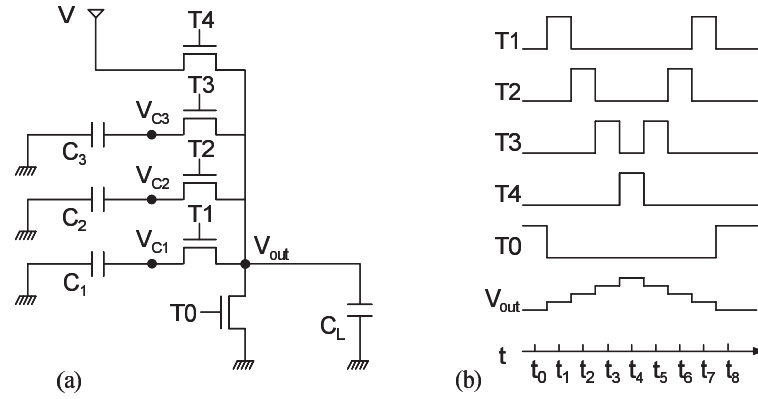


Fig. 1. Switched capacitor regenerator with asymmetric tank capacitors. (a) Circuit, (b) Timing chart of (a).

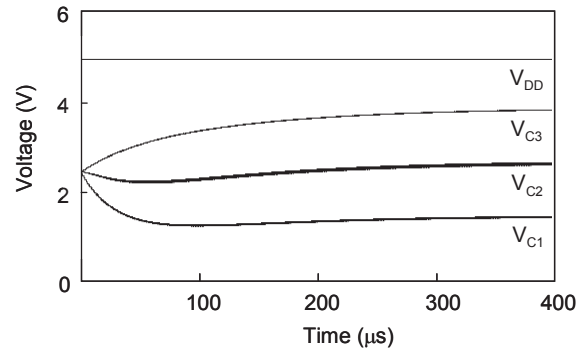


Fig. 2. Voltage change of the tank capacitor.

ferring the charge quantity Q_{ti} from C_i to C_L [Fig. 3 (a)], the following equation is derived from the voltage equality [7]:

$$(C_i V_{ci} - Q_{ti})/C_i = (C_L V_{c(i-1)} + Q_{ti})/C_L, \quad (1 \leq i \leq N-1) \quad (1)$$

In the case of $C_i \gg C_L$, we have

$$Q_{ti} \cong C_L (V_{ci} - V_{c(i-1)}), \quad (1 \leq i \leq N-1), \quad (2)$$

where we define $V_{c0} = 0$.

When restoring the charge Q_{ri} from C_L to C_i [Fig. 3 (b)], the following equation is derived from the voltage equality:

$$(C_i V_{ci} + Q_{ri})/C_i = (C_L V_{c(i+1)} - Q_{ri})/C_L, \quad (1 \leq i \leq N-1). \quad (3)$$

In the case of $C_i \gg C_L$, we have

$$Q_{ri} \cong C_L (V_{c(i+1)} - V_{ci}), \quad (1 \leq i \leq N-1), \quad (4)$$

where we define $V_{cN} = V_{DD}$. ΔQ_i (the change of Q_i) at tank capacitor C_i after 1 cycle of charging and restoring can be written as

$$\Delta Q_i = -Q_{ti} + Q_{ri} = C_L (V_{c(i-1)} - 2V_{ci} + V_{c(i+1)}), \quad (1 \leq i \leq N-1). \quad (5)$$

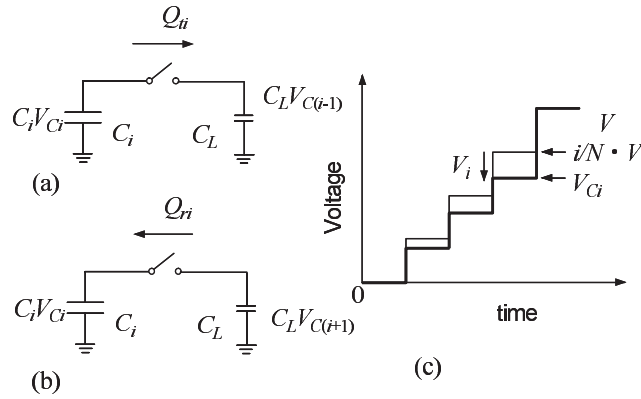


Fig. 3. Definitions of charge and voltage in the switched capacitor regenerator.
(a) Q_{ti} is transferred from C_i to C_L .
(b) Q_{ri} is restored from C_L to C_i .
(c) V_i is the difference between V_{ci} and $i/N \cdot V$.

We define V_i as [Fig. 3 (c)]

$$V_i = V_{ci} - \frac{i}{N}V. \quad (6)$$

Using (6) and (5), we have

$$\Delta Q_i = C_L(V_{i-1} - 2V_i + V_{i+1}), \quad (1 \leq i \leq N-1). \quad (7)$$

We define the change of V_i as ΔV_i . Therefore,

$$C_i \Delta V_i = \Delta Q_i, \quad (1 \leq i \leq N-1). \quad (8)$$

We define V'_i as V_i after the charge-recycle process. Using (7) and (8), we have

$$\begin{aligned} V'_i &= V_i + \Delta V_i \quad (1 \leq i \leq N-1) \\ &= K_i V_{i-1} + (1 - 2K_i) V_i + K_i V_{i+1} \quad (1 \leq i \leq N-1), \end{aligned} \quad (9)$$

where K_i is C_L/C_i . From $C_i \gg C_L$, $0 < K_i \ll 1$ is satisfied. V_0 and V_N are zero from the definition. Formula (9) is rewritten as

$$\begin{pmatrix} V'_1 \\ V'_2 \\ V'_3 \\ \vdots \\ V'_{N-1} \end{pmatrix} = \mathbf{A} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ \vdots \\ V_{N-1} \end{pmatrix}, \quad \mathbf{A} = \begin{pmatrix} 1-2K_1 & K_1 & 0 & \cdots & 0 \\ K_2 & 1-2K_2 & K_2 & \ddots & \\ 0 & K_3 & 1-2K_3 & \ddots & 0 \\ \vdots & \ddots & \ddots & \ddots & K_{N-2} \\ 0 & \vdots & 0 & K_{N-1} & 1-2K_{N-1} \end{pmatrix}. \quad (10)$$

The characteristic equation is

$$\det |\mathbf{A} - \lambda \mathbf{E}| = \begin{vmatrix} 1 - 2K_1 - \lambda & K_1 & & & 0 \\ K_2 & 1 - 2K_2 - \lambda & \ddots & & \\ & \ddots & \ddots & \ddots & K_{N-2} \\ 0 & & & K_{N-1} & 1 - 2K_{N-1} - \lambda \end{vmatrix} = 0. \quad (11)$$

We define E_n as

$$E_n = \begin{vmatrix} a_1 & -1 & & 0 \\ -1 & a_2 & \ddots & \\ & \ddots & \ddots & -1 \\ 0 & & -1 & a_n \end{vmatrix}, \quad (12)$$

where

$$a_i = 2 + (\lambda - 1)/K_i. \quad (13)$$

Using the relation $\det(\mathbf{a}_1, \dots, c\mathbf{a}_j, \dots, \mathbf{a}_n) = c \cdot \det(\mathbf{a}_1, \dots, \mathbf{a}_j, \dots, \mathbf{a}_n)$, formula (11) is transformed as

$$E_{N-1} = 0. \quad (14)$$

Here, we assume $|\lambda| \geq 1$. In this case, we have $|a_i| \geq 2$ using $0 < K_i \ll 1$ and formula (13) (Appendix).

Here, we can write E_n using E_{n-1} and E_{n-2} as follows [8]:

$$E_n = a_n E_{n-1} - E_{n-2} \quad (15)$$

Here, we define $E_0 = 1$ and $E_1 = a_1$. Then, we have $E_3 = a_3 a_2 a_1 - a_3 - a_1$ using (15), which is consistent with the definition (12). Now, we prove $|E_{k+1}| > |E_k|$ assuming $|E_k| > |E_{k-1}|$.

$$\begin{aligned} \frac{|E_{k+1}|}{|E_k|} &= \frac{|a_{k+1}E_k - E_{k-1}|}{|E_k|} \geq \frac{||a_{k+1}E_k| - |E_{k-1}||}{|E_k|} = \frac{||a_{k+1}| |E_k| - |E_{k-1}||}{|E_k|} \\ &= \frac{|a_{k+1}| |E_k| - |E_{k-1}|}{|E_k|} = |a_{k+1}| - \frac{|E_{k-1}|}{|E_k|} > 2 - 1 = 1 \end{aligned} \quad (16)$$

Therefore, $|E_{k+1}| > |E_k| > \dots > |E_1| > |E_0| = 1$ is satisfied. This is inconsistent with formula (14). Therefore, it is proved that $|\lambda| < 1$.

In general, any matrix \mathbf{A} can be written as $\mathbf{A} = \mathbf{P}^{-1} \mathbf{J} \mathbf{P}$, where \mathbf{J} is a Jordan matrix. It is well known that \mathbf{J}^n becomes zero when $n \rightarrow \infty$ in the case of $|\lambda| < 1$. Therefore, $\mathbf{A}^n = \mathbf{P}^{-1} \mathbf{J}^n \mathbf{P}$ becomes zero when $n \rightarrow \infty$. Then, V_i' becomes zero after many charge-recycle operations from (10). This means V_{Ci} becomes $i/4 \cdot V_{DD}$ spontaneously.

3 Adiabatic SRAM

The adiabatic SRAM is shown in Fig. 4 (a). The difference from a previous SRAM [9] is that the voltage of the memory cell power line (MCPL) in the present SRAM is not constant. Instead, it changes according to the stepwise power clock (PCK) during the writing mode. One of the two bit lines [BL

in Fig. 4(a)] is also driven by the stepwise PCK, while the other (NBL) is fixed at ground (GND). When charging, the PCK is ground at first and then increases stepwise. When the PCK reaches V_{th} , transistors in the memory cell turn on, writing is done, and the voltage further increases stepwise to avoid the soft error problem. This architecture is suitable for nanoscale circuits because V_{DD} can be designed to be much larger than V_{th} , while I_{ds} can be reduced due to of the adiabatic charging, compared with conventional CMOS. This I_{ds} reduction is a fundamental quality of adiabatic logic and leads to the reduction of hot-carrier effects and electromigration.

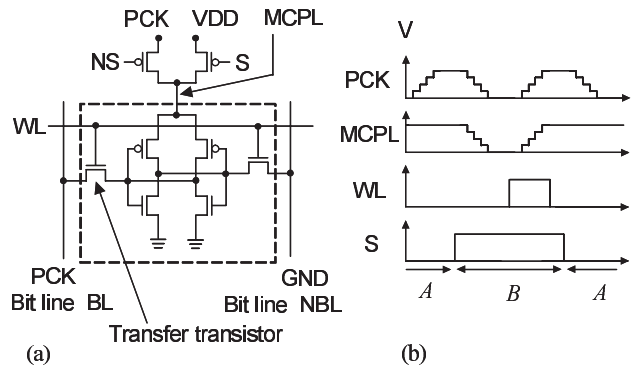


Fig. 4. Adiabatic SRAM. (a) Circuit. (b) Timing chart of adiabatic SRAM

The timing chart of the adiabatic SRAM is shown in Fig. 4(b). When conserving data (state A), the MCPL is connected to V_{DD} . When writing data (state B), the switch signal S becomes high so that the MCPL is connected from V_{DD} to the PCK. Then, the PCK decreases to zero and the voltage of the MCPL also decreases. Next, the voltage of the word line (WL) becomes high, and the voltages of the BL and MCPL increase stepwise according to the PCK. After writing, the voltage of the WL becomes low and transfer transistors turn off. When saving (or conserving) data, S becomes low so that the MCPL is again connected to V_{DD} .

4 Conclusion

In summary, we showed analytically that adiabatic logic using asymmetric tank capacitors is stable, which means the circuit is something like digital. The proposed adiabatic SRAM resolves the problems of V_{th} variation, hot-carrier effects and electromigration. The adiabatic SRAM is very attractive for the less-than-45-nm node.

Appendix

We define $\lambda = r \cos \theta + r \sin \theta \cdot i$. Using (13), we have

$$a_i = 2 + (r \cos \theta - 1)/K_i + r \sin \theta / K_i \cdot i \quad (\text{A} \cdot 1)$$

Therefore,

$$|a_i|^2 = I/K_i^2, \quad \text{where} \quad I = (2K_i + r \cos \theta - 1)^2 + (r \sin \theta)^2. \quad (\text{A}\cdot 2)$$

I is transformed as

$$I = r^2 + 1 + 4K_i^2 + 2(-r \cos \theta - 2K_i + 2K_i r \cos \theta). \quad (\text{A}\cdot 3)$$

Using (A·3), we have

$$\partial I / \partial r = 2r - 2 \cos \theta + 4K_i \cos \theta = 2(1 - 2K_i) (r / (1 - 2K_i) - \cos \theta) \quad (\text{A}\cdot 4)$$

In the case of $r \geq 1$, $r / (1 - 2K_i) > 1$ is satisfied so that we have $\partial I / \partial r > 0$.

Similarly, we have

$$\partial I / \partial \theta = 2r(1 - 2K_i) \sin \theta. \quad (\text{A}\cdot 5)$$

I becomes the minimum and maximum value at $\theta = 0$ and π , respectively, using the condition of $\partial I / \partial \theta = 0$.

Therefore, using (A·3), I becomes the minimum value of $4K_i^2$ when $r = 1$ and $\theta = 0$. In this case, $|a_i|$ becomes the minimum value of 2 using (A·2). This means $|a_i| \geq 2$.