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A complete analysis of noise in inductively source degenerated CMOS LNA's

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Abstract: A complete analysis of noise in inductively source degenerated CMOS LNA's is presented. One parameter that has great impact on the noise performance of the LNA is L_s. For small L_s the noise of M_1 is dominant, but increasing the L_s causes the output noise power due to other components grow noticeably. We use the MATLAB for simulating the LNA whereas all parasitics are extracted from a 0.35 μm CMOS HSPICE technology file. It is supposed the LNA used in the front-end of a prototype UMTS receiver.

Keywords: channel thermal noise, gate induced noise, inductively source degenerated LNA

Classification: Integrated circuits

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1 Introduction

RF signals may experience a lot of loss in their path, due to high distance between the receiver and the transmitter, multi-path fading and so on. Therefore for receiving these signals, the RF receivers should have low noise performance and be completely matched with their sources to receive the maximum power.

The noise characteristic of the circuit is affected by the noise of all components of the circuit. Recently the inductively source degenerated LNA is the most vastly used LNA in the front-end of many RF receivers, [1, 2]. The overall structure of this LNA is shown in Fig. 1 (a). Impedance matching in this structure is obtained with no need for the signal to pass through any real

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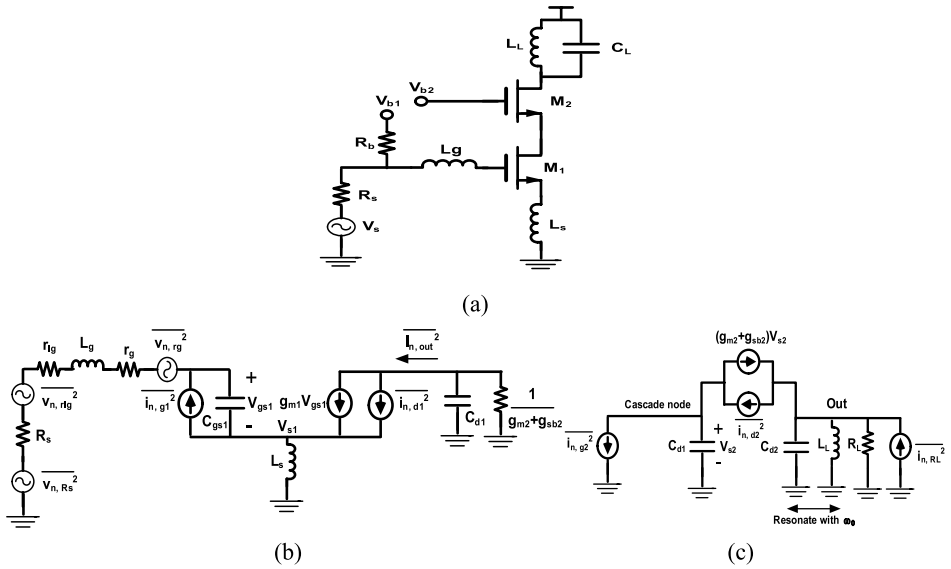

Fig. 1. The circuit of the inductively source degenerated LNA (a), the noisy equivalent circuit of the input (b) and, cascade device and the output load (c).

resistors; therefore this structure has the best noise performance compared to resistively matched LNA's [1]. Because of vastly usage of this structure a complete analysis of the noise in this structure is very useful but is not reported yet.

The paper is organized as follows: In section II the output noise power spectral density due to the input devices is calculated. The output noise power spectral density due to the cascade device and the output load is computed in section III. The overall noise factor of the circuit and discussion about it are expressed in section IV.

2 Computing the noise of the input devices

Fig. 1 (b) shows the noisy equivalent circuit of the input network of the LNA [1]. r_{lg} is the series resistance of L_g; r_g, i_{nd1} and i_{ng1} are the series resistance of the gate due to the polisilicide gate resistance, the channel thermal noise and the gate induced noise currents of the M_1, respectively. As it will be seen in the next section, it would be prefered make L_s as small as possible. Therefore its series resistance is negligible. The series resistance of the L_s makes the circuit noisier and decreases the gain of the circuit, therefore it is tried to use high Q inductor for L_s, and for example multi low Q parallel inductors can be used for obtaining higher Q inductor [2].

Firstly we compute the noise power spectral density in the cascade node due to the input resistors, R_s, the input source resistors, r_{lg} and r_g. The noisy power spectral density in the cascade node due to the input resistances can be shown to be [1]:

$$\overline{I^2_{n,\,out,\,R_{in}}} = \frac{g^2_{m1}Q^2_L}{\left(1+\frac{g_{m1}L_s}{C_{gs1}(R_s+r_{lg}+r_g)}\right)^2}\overline{V^2_{n,\,R_{in}}} \qquad (1)$$

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$$Q_L = \frac{1}{\omega_0 C_{gs1}(R_s + r_{\lg} + r_g)} \tag{2}$$

$$\overline{V^2_{n,R_{in}}} = 4kT(R_s + r_{lg} + r_g) \tag{3}$$

Where ω_0 is our frequency of interest. It should be mentioned that the C_{gd1} is neglected for simplicity but one can consider it as a parallel capacitance with the C_{gs1} considering Miller theorm. Therefore the input capacitance in fact is larger, that means lower Q_L and a higher overall NF for the circuit.

The noise power spectral density due to the channel thermal noise and gate induced noise current of M_1 in the cascade node should be computed together due to the correlation between these two noise sources. By not considering the other noise sources, hence the noise power spectral density due to these noise sources in the cascade node can be shown to be [1]:

$$\begin{aligned}\overline{I^2_{n,\,out,\,M_1}} = & \frac{\alpha_1^2 |c|^2 \frac{\delta}{5\gamma} + \left(1 + \alpha_1 |c| Q_L \sqrt{\frac{\delta}{5\gamma}}\right)^2}{\left(1 + \frac{g_{m1} L_s}{C_{gs1}(R_s + r_{\lg} + r_g)}\right)^2} \overline{i^2_{n,\,d1}} \\ & + \frac{\alpha_1^2 \left(1 - |c|^2\right) \frac{\delta}{5\gamma} \left(1 + Q_L^2\right)}{\left(1 + \frac{g_{m1} L_s}{C_{gs1}(R_s + r_{\lg} + r_g)}\right)^2} \overline{i^2_{n,\,d1}}\end{aligned} \tag{4}$$

Where $\overline{i^2_{n,\,d1}} = 4kT\gamma g_{d01}$ is the channel thermal noise power spectral density of M_1, which γ is the channel thermal noise coefficient of the NMOS and considered to be 2.5 in our simulations [1]. g_{d01} is the zero bias drain-source conductance of M_1. The power spectral density of the gate induced noise current is $\overline{i^2_{n,\,g1}} = 4kT\delta g_{g1}$ where δ is the coefficient of the gate noise and considered to be 5 in our simulation, and $g_{g1} = \frac{\omega_0^2 C_{gs1}^2}{5g_{d01}} = -\frac{(SC_{gs1})^2}{5g_{d01}}$ [1]. It should be mentioned that, the gate induced noise is expressed versus channel thermal noise where c is the correlation coefficient between them and is supposed to be $j0.395$ in our simulations [1, 3]. It should be noted that $i_{n,g1}$ has two noise parts in the cascade node, real part and imaginary part, where its real part is added directly to the channel thermal noise of M_1 in the cascade node that is completely real before squaring. The coefficient α_1 in the equation (4) is g_{m1}/g_{d01} where is smaller than unity [1].

3 Compute the noise of the cascade device and the output load

If there is no parasitic in the cascade node then the output noise due to M_2 is zero, but in practice parasitic capacitances exist at this node degrading the noise performance of the circuit [4]. The noisy equivalent circuit of the cascade device and output load is depicted in Fig. 1 (c).

The polisilicide gate resistance of M_2 can be very small using the multi-fingering technique for layout of this device; hence it is neglected for simplicity.

In Fig. 1 (c), C_{d1} indicates all the parasitic capacitances in the cascade node and consists C_{db1}, C_{sb2} and C_{gs2}. C_{d2} indicates all the capacitances

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in the output node and consists C_{db2}, C_{gd2} and the output capacitor. L_L is the required inductor in the output where resonates with C_{d2} at the desired frequency. R_L is the parallel resistance of L_L in the desired frequency. It should be mentioned that for the output noise power contributed by M_2 the other noise sources are grounded. Therefore $V_{gs1} = 0$ (so C_{gd1} is neglected), hence the only effect of M_1 that is seen in Fig. 1 (c) is C_{db1}.

The channel thermal noise of M_2 is $i_{n,d2}$, where $\overline{i^2_{n,\,d2}} = 4kT\gamma g_{d02}$. The gate induced noise current of M_2 is directly in the cascade node. Like M_1, it contains two parts, completely correlated with $i_{n,d2}$ and completely uncorrelated with $i_{n,d2}$. It can be easily shown that the noise power spectral density in the cascade node due to M_2 is:

$$\overline{I^2_{n,\,out,\,M_2}} = \overline{I^2_{n,\,out,\,M2,\,c}} + \overline{I^2_{n,\,out,\,M2,\,uc}} \tag{5}$$

$$\begin{aligned}\overline{I^2_{n,\,out,\,M2,\,c}} &= \left(\frac{SC_{d1}}{g_{m2}+g_{sb2}} - j\,|c|\,\frac{SC_{gs2}}{g_{d02}}\sqrt{\frac{\delta}{5\gamma}}\right)^2 \overline{i^2_{n,\,d2}} \\ &= \left(\left(\frac{\omega_0 C_{d1}}{g_{m2}+g_{sb2}}\right)^2 + \left(|c|\,\frac{\omega_0 C_{gs2}}{g_{d02}}\right)^2 \frac{\delta}{5\gamma}\right)\overline{i^2_{n,\,d2}}\end{aligned} \tag{6}$$

$$\overline{I^2_{n,\,out,\,M2,\,uc}} = (1-|c|^2)\left(\frac{\omega_0 C_{gs2}}{g_{d02}}\right)^2 \frac{\delta}{5\gamma}\overline{i^2_{n,\,d2}} \tag{7}$$

It can be easily shown that, the noise power spectral density in the cascade node due to R_L is ($\overline{i^2_{n,\,R_L}} = \frac{4kT}{R_L}$):

$$\overline{I^2_{n,\,out,\,R_L}} = \frac{(g_{m2}+g_{sb2})^2 + (\omega_0 C_{d1})^2}{(g_{m2}+g_{sb2})^2}\overline{i^2_{n,\,R_L}} \tag{8}$$

4 Discussion

The noise power spectral densities in the cascade node due to all the components were calculated in the previous sections perfectly. Therefore for obtaining the overall NF of the circuit we should divide the total noise power spectral density to the noise power spectral density due to R_s, in the cascade node, therefore the overall noise factor of the circuit is:

$$\begin{aligned}NF = 1 &+ \frac{r_{lg}+r_g}{R_s} + \left\{\alpha_1^2\,|c|^2\,\frac{\delta}{5\gamma} + \left(Q_L\alpha_1\,|c|\sqrt{\frac{\delta}{5\gamma}}+1\right)^2\right. \\ &\left. + (1-|c|^2)\alpha_1^2\frac{\delta}{5\gamma}(1+Q_L^2)\right\}\frac{\gamma g_{d01}}{g_{m1}^2 R_s Q_L^2} \\ &+ \left\{|c|^2\,\frac{\omega_0^2 C_{gs2}^2}{g_{d0}^2}\frac{\delta}{5\gamma} + \frac{\omega_0^2 C_{d1}^2}{(g_{m2}+g_{d0})^2}\right. \\ &\left. + (1-|c|^2)\frac{\omega_0^2 C_{gs2}^2}{g_{d0}^2}\frac{\delta}{5\gamma}\right\}\frac{\gamma g_{d02}\,(1+Q_L g_{m1} L_s\omega_0)^2}{g_{m1}^2 R_s Q_L^2} \\ &+ \frac{(g_{m2}+g_{d0})^2 + \omega_0^2 C_{d1}^2}{(g_{m2}+g_{d0})^2}\,\frac{(1+Q_L g_{m1} L_s\omega_0)^2}{g_{m1}^2 R_s R_L Q_L^2}\end{aligned} \tag{9}$$

The second term in equation (9) is due to the parasitic resistance in the input of the circuit due to the polisilicide gate resistance of M_1 and the

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series resistance of L_g. If these two noise sources are not controlled then the overall NF is degraded severely. Multi-fingering technique can be used for reducing the effect of r_g during layout procedure. We consider the width of the finger to be 2.5 μm in our simulations. For reduction the effect of r_{lg}, the only solution seems to be using an off-chip inductor. Because L_g is relatively large an on-chip inductor results in a large series resistance due to the low quality factor of the on-chip spiral inductor. Therefore the off-chip inductor solution is not very unattractive, because the structure of the LNA is narrow band and is very sensitive to its input resonance frequency; therefore using the off-chip inductor can guarantee the resonance frequency against the process variations. We consider the L_g to be off-chip with a Q of 50 in our simulations.

For investigation the noise of the circuit, the following parameters are needed, where details of them are not mentioned here for abbreviation. ν_{sat} is the saturated velocity of the carrier in the channel due to the horizontal field in the channel and θ shows the mobility reduction due to the vertical field in oxide ($V_{od} = V_{gs} - V_{th}$) [4].

$$g_{d0} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0} = \mu_0 C_{ox} \frac{W}{L} V_{od} \tag{10}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{1}{2}\mu_0 C_{ox} \frac{W}{L} V_{od} \frac{2 + (\frac{\mu_0}{2\upsilon_{sat}L} + \theta)V_{od}}{(1 + (\frac{\mu_0}{2\upsilon_{sat}L} + \theta)V_{od})^2} \tag{11}$$

$$\alpha = \frac{g_m}{g_{d0}} = \frac{2 + (\frac{\mu_0}{2\upsilon_{sat}L} + \theta)V_{od}}{2(1 + (\frac{\mu_0}{2\upsilon_{sat}L} + \theta)V_{od})^2} \tag{12}$$

Now we look into the noise characteristic of the structure. It should be mentioned that we have used the HSPICE 0.35 μm CMOS technology[1] for our simulations, and suppose that the LNA working in the UMTS band (2.11-2.17 GHz).

In the following figures the total NF of the circuit and the noise power ratio of each component divided to the noise power due to R_s in the cascade node are plotted versus W_1. Fig. 2 (a) shows the NF for different V_{gs1} versus W_1. As seen in this figure the noise due to R_L is relatively constant versus W_1 and decreases as V_{gs1} increases (It should be mentioned that R_L is considered to be 50 Ω). But this reduction is very small and is proportional with the term as follows:

$$\overline{I^2_{n,out,R_L}} \propto \left(1 + \frac{\omega_0^2 C_{d1}^2}{(g_{m2} + g_{sb2})^2}\right) \tag{13}$$

It should be noted that increasing V_{gs1} increases I_{d1} and hence increases $(g_{m2} + g_{sb2})$. The noises due to M_1 and M_2 are nearly proportional to $1/g_{d01}$ and $1/g_{d02}$ respectively which $1/g_{d0}$ is proportional to V_{od} ($V_{od} = V_{gs} - V_{th}$ where V_{th0} is roughly 0.5 V in the used technology), but this approximation is not completely true for large V_{od}, because the noises due to M_1 and M_2 have the terms that are relative with $1/g_m$ rather than $1/g_{d0}$. The noise of R_L is constant respect to W_1 and the noise of M_2 is relatively small, therefore

[1] http://www.stanford.edu/class/ee314_models.htm

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the minimum NF of the circuit for each V_{gs1} is determined by M_1. This optimum W_1 for NF decreases as V_{gs1} increases due to the reduction of α_1 (see equation (9)).

Fig. 2 (b) shows the overall noise factor and noise ratio of the various components (respect to R_s) of the circuit versus W_1 for various L_s. If we neglect the effect of C_{gd1} then the noise due to M_1 is constant for various L_s but in practice due to the Miller effect of the C_{gd1} we have higher effective C_{gs1} and then higher noise due to M_1 for larger L_s. The noises due to R_L and M_2 are proportional to L_s^2, and degrade the overall NF of the circuit severely. Therefore the L_s should be minimized as much as possible.

Fig. 2 (c) shows the overall noise factor and noise ratio of the various components (respect to R_s) of the circuit versus W_1 for various W_2. It should be noted that $I_{d2} = I_{d1} =$ constant for various W_2, therefore for larger W_2, V_{od2} is nearly proportional to $W_2^{-0.5}$ where g_{m2} and g_{d02} are proportional to $W_2^{0.5}$ therefore the noise due to M_2 is relative with $W_2^{1.5}$. Because of a little contribution of M_2 in the total NF the overall NF is not degraded so when W_2 increases.

Considering the above discussion the noises of M_1 and R_L are more important in this structure. The noise of M_1 decreases if V_{gs1} increases. But the power consumption increases too. For decreasing the effect of R_L we should use a high Q inductor at the output and a high Q as small as possible induc-

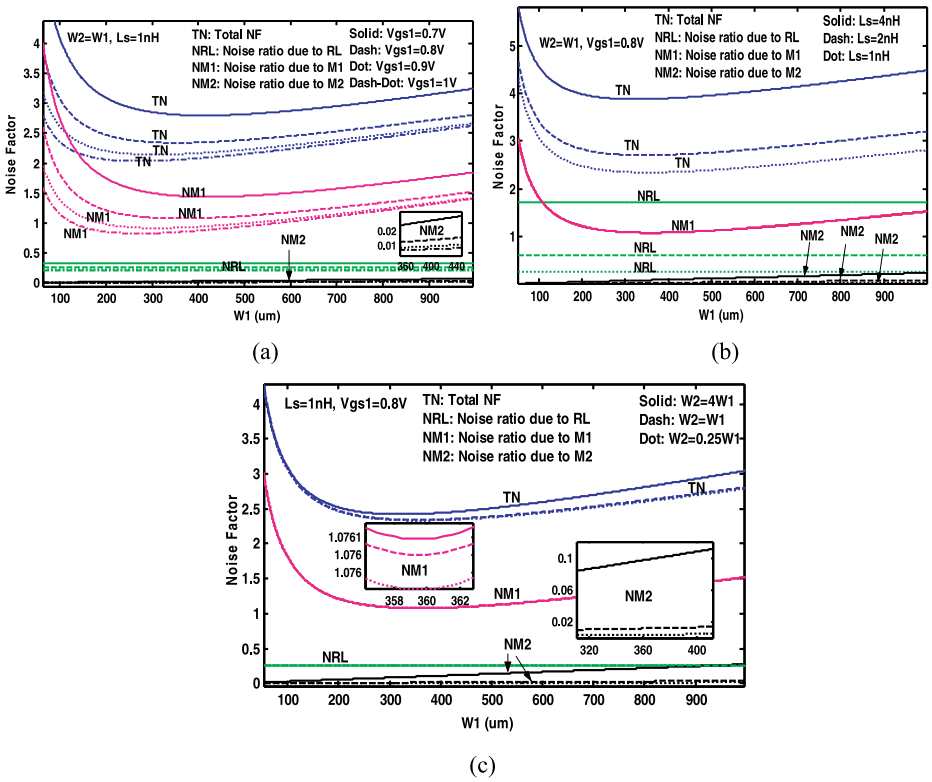

Fig. 2. Noise factor and noise ratio of the various components (respect to R_s) of the circuit versus W_1, for various V_{gs1} (a), for various L_s (b) and for various W_2 (c).

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tor for L_s. Therefore the optimum design of the LNA for the impedance and noise matching under power consumption restriction can be achieved using some optimizing techniques such as genetic algorithm.

5 Conclusion

A complete analysis of noise in inductively source degenerated CMOS LNA's is presented. One parameter that has a great impact on the *NF* of the circuit is L_s. The output noise powers due to cascade device and the output resistance load are proportional to L_s^2. So minimizing L_s is absolutely desirable. All the parasitics are extracted from a 0.35 μm HSPICE technology file, and have been used in MATLAB for our simulations. It is supposed that the LNA is used in the front-end of a prototype UMTS receiver.[2]

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