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Balanced low input impedances CMOS current comparator

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Abstract: This paper presents a continuous-time current comparator with low input impedance enhancing the accuracy of comparison. The proposed circuit employs low impedance common-gate structures as input stages and further uses common-source feedback structures to enable extremely reduction of input impedances. The input impedances are well designed to be balanced, so that the proposed design can be applied to perform precise comparison between two terminals with tiny varied currents. An implemented chip was fabricated by TSMC 0.35 μm CMOS process with its input impedances and propagation delay are 66.8 Ω, 66.6 Ω and 2.5 ns respectively while the average power consumption is about 1.64 mW.

Keywords: current comparator, input impedance, common-gate structure, common-source feedback

Classification: Integrated circuits

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1 Introduction

Over past few years, current-mode circuits have been adopted to implement high speed, wide bandwidth and low supply voltage applications. One of the important devices in these mixed-signal systems is comparator, which may limit the performance of entire system. The current-mode comparators therefore have attracted considerable attention since they achieve design requirements easier than voltage-mode comparator. With respect to application of signal processing, input impedance of current comparator is the most significant specification than operational frequency and other specifications. The lower input impedance enhances the transformation efficiency of the signal and increases the accuracy of signal process as well.

Several prior research works have reported some design approaches for current comparator on reducing input impedance. These methods can be categorized into two major types according to the number of input nodes of comparator. One type of current comparator has single-input node assuming the input current is the processed subtraction between two signals [1, 2, 3]. The function of these comparators is incomplete because the required processed subtraction is pre-performed by other circuit. Another type of current comparator has double-input nodes that can be applied to perform direct comparison between two input currents [4, 5, 6]. However, the input impedances of these circuits are unbalanced and too large. We therefore attempt to propose a balanced low input impedance continuous-time current comparator for accurately performing signal processing.

2 Description of proposed circuits

Fig. 1 shows the proposed continuous-time current comparators including single input and double inputs structures. As shown in Fig. 1 (a), the proposed single-input current comparator [7] consists of two simple bias circuits, common-gate input stage, two common-source negative feedback loops, three common-source amplifiers and two output buffers. In order to enhance the transformation efficiency of input current, the input impedance of comparator should be much lower than output impedance of previous stage. The common-gate stage, M_{10} to M_{12}, is hence utilized to be current buffer for input signal. The common-source negative feedback loop composed of C_3, C_4 and M_{14} is then inserted to the common-gate input stage to provide a controllable loop gain that indeed reduces input impedance.

Through theoretical analysis, the input impedance of the proposed single-input current comparator is expressed as:

$$R_{in1} = \frac{1}{g_{m11} + g_{mb11} + g_{ds11} + g_{m12} + g_{ds14} + \left(\frac{C_3}{C_3+C_4} \cdot g_{m14} - g_{ds11}\right) \cdot K_1} \quad (1)$$

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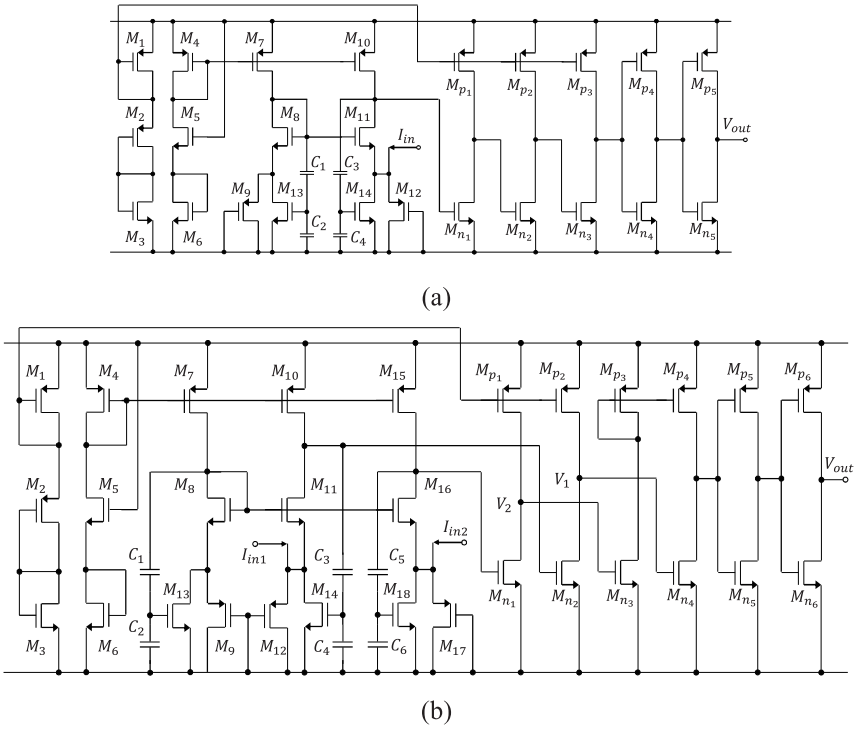

Fig. 1. The proposed (a) single-input (b) double-input continuous-time current comparators.

$$K_1 = \frac{g_{m11} + g_{mb11} + g_{ds11}}{g_{ds10} + g_{ds11}} \tag{2}$$

, where g_{mi}, g_{mbi} and g_{dsi} are transconductance, body transconductance and output conductance of transistor M_i respectively. In terms of Eq. (1), the input impedance is reduced by the factor, $C_3 g_{m14}/C_3 + C_4$, relating to the common-source negative feedback loop. Moreover, to ensure the circuit has low input impedance in the situation of sudden large variation on input current, another negative feedback loop composed of C_1, C_2 and M_{13} is added to the bias circuit of common-gate input stage. Although the common-source feedback structure of input stage greatly reduces the input impedance, the intension of resulted signal at drain of M_{11} is quite small and its driving capability is week. For this reason, the followed three stages of common-source amplifier are used to amplify output swing of the circuit and two output buffers are inserted as well to acquire rail-to-rail output signal. The resulted voltage swing of output signal is expressed as:

$$V_{out} = -I_{in} \cdot R_{in1} \cdot K_1 \cdot \prod_{1}^{3} g_{mn_i} \cdot (r_{op_i} // r_{on_i}) \cdot \prod_{4}^{5} (g_{mp_i} + g_{mn_i}) \cdot (r_{op_i} // r_{on_i}) \tag{3}$$

, where r_{op_i} and r_{on_i} are output impedances of transistors M_{p_i} and M_{n_i}.

The current comparator is usually applied to discriminate varied current signals between two terminals in many applications. Especially for the situation of input current is tiny, the most important factor regarding to accuracy of comparison is the equilibrium of impedance between two input nodes. The validity of comparison would be mistrustful if the input impedances are unbalanced. We therefore modified our design as shown in Fig. 1 (b) to properly

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perform direct comparison for two input signals. For the second input signal, the parallel common-gate input stage, M_{15} to M_{17}, is added to be input current buffer. Then, the common-source negative feedback loop consists of C_5, C_6 and M_{18} is also inserted to the common-gate input stage followed by a differential to single-end amplifier, M_{p_1} to M_{p_4} and M_{n_1} to M_{n_4}. The input impedance of second input node and voltage swing of output signal can be analogously expressed as:

$$R_{in2} = \frac{1}{g_{m16} + g_{mb16} + g_{ds16} + g_{m17} + g_{ds18} + \left(\frac{C_5}{C_5+C_6} \cdot g_{m18} - g_{ds16}\right) \cdot K_2} \tag{4}$$

, where $K_2 = \dfrac{g_{m16} + g_{mb16} + g_{ds16}}{g_{ds15} + g_{ds16}}$

$$V_{out} \cong \frac{g_{mn_3} A_{buf}}{g_{dsp_4} + g_{dsn_4}} (K_2 g_{mn_1} (r_{on_1} // r_{op_1}) R_{in2} I_{in2} - K_1 g_{mn_2} (r_{on_2} // r_{op_2}) R_{in1} I_{in11}) \tag{5}$$

, where $A_{buf} = \prod_{5}^{6} (g_{mn_i} + g_{mp_i}) \cdot (r_{on_i} // r_{op_i})$

The equivalent input stages and feedback structures in proposed circuit ideally provide balance and low input impedance. However, if we further take process variation into consideration, the input impedances are not absolutely equivalent because the bias current from M_{10} is not entirely equal to the current from M_{15}. For this reason, we have to put these two transistors and their bias circuits in the same well during physical level implement to reduce the mismatch of bias current between two input stages.

3 Experiment results

To verify the practicability of proposed designs, we implemented both proposed circuits of Fig. 1 by TSMC 0.35 μm CMOS process. The core size of proposed double-input current comparator is 123 μm $*$ 60 μm which its photograph is shown in Fig. 2 (a). The proposed double input comparator was then applied to execute direct comparison between two various signal. With 10 KHz sinusoidal signal and 100 KHz triangular signal, the measured input and output waveforms are shown in Fig. 2 (b) which demonstrates the validity of operation. In addition, we also report input impedances with respect to input current in Fig. 2 (c). The input impedance of proposed single-input current comparator is merely 66.9 Ω which is much less than that of prior work [4] and its value retains almost constant within various rang of input current. The input impedances of proposed double-input current comparator are also very small which are 66.8 Ω and 66.6 Ω respectively. As shown in Fig. 2 (c), their values retain almost constant within various input current as well and the unbalance between two input nodes is only 0.2 Ω.

We also compared our designs with several published techniques and summarized into Table I. It should be noted that all data of prior works in Table I are simulation results collected from published articles.

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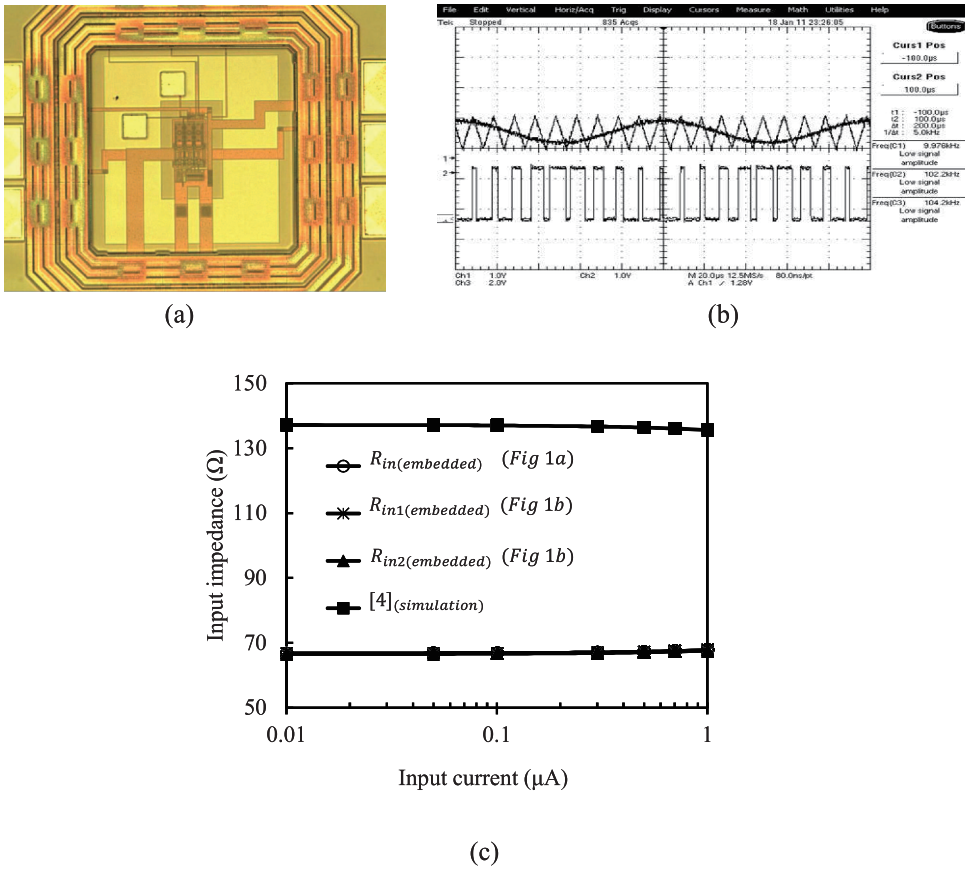

Fig. 2. (a) The chip photograph of proposed double-input comparator, (b) The measured input and output waveforms of proposed double-input comparator, (c) The input impedances of proposed comparators with respect to their input current.

Table I. Comparison of several published techniques.

Parameters	[1]	[2]	[3]	Proposed ckt. Single input (embedded)	[4]	[5]	Proposed ckt. Double input (embedded)	Proposed ckt. Double input (board)
Date	1992	2009	2009	2012	2005	2004	2012	2012
Technology (μm)	2	0.18	0.35	0.35	0.5	0.5	0.35	0.35
Supply (V)	5	1.8	1.8	3	3	3	3	3
No. of input	1	1	1	1	2	2	2	2
Input current (μA)	±1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±1
Power consumption (mW)	0.93	---	0.13	1.16	0.9	0.63	1.64	1.8
Input impedance R_{in1} (Ω)	---	---	---	66.9	137	123	66.8	87.7
Input impedance R_{in2} (Ω)	---	---	---	---	---	126	66.6	91.7
Operation freq. (MHz)	---	---	10	25	25	25	25	4
Delay (nS)	4	0.6	0.7	2.06	1.02	1.67	2.5	48

In Table I, we report the data measured from printed circuit "**board**" with implemented chip had been mounted on it. In this situation, the input impedances and propagation delay are inauthentic and greater than real case due to the influences of routing line in chip, pad of chip, bonding wire, routing line on printed circuit board, and connector on board. Although measured results on printed circuit board are inauthentic, the input impedances are about 90 Ω which are still very small. In practice, the current comparator is often used as internal silicon intellectual property for signal processing. We hence used probe station through pre-opened observation window to probe

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internal nodes of "**embedded**" core directly. The experiment results demonstrate that both the proposed single and double input current comparators provide balanced low input impedance less than 67 Ω. The reported power consumption of proposed circuit is more than prior works because it includes static power of bias circuits and output buffers on pad of implemented chip. Moreover, even if the driving capability of output amplifiers and buffers were limited to save area overhead of chip, the propagation delay of proposed circuits are still competent that within 2.5 ns. The propagation delay can be further reduced within 1 ns by increasing the driving capability of output amplifiers and buffers. Consequently, the proposed current comparator is feasible for performing precise comparison between two input terminals with high speed varied currents.

4 Conclusions

In this paper, we have proposed a balanced low input impedance continuous-time current comparator. To deal with mistrustful operation of current comparator caused by unbalanced input impedance, we employed common-gate input stage with additional common-source negative feedback to effectively reduce the input impedance. This scheme allows the proposed current comparator to enhance the accuracy while applying to perform signal comparison or modulation. The experiment results show that the input impedances of proposed comparators are within 67 Ω. In addition, the unbalance between input terminals is 0.2 Ω making the proposed comparator feasible to execute precise comparison between two high speed varied inputs than other prior works.

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