

A rectifier structure for UHF RFID transponder with high efficiency

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Abstract: This paper presents a UHF rectifier structure to overcome the drawbacks of conventional rectifiers, which cannot simultaneously realize high power conversion efficiency (PCE) and arbitrarily high output voltage. In accordance with our clear analysis policy, a novel rectifier structure based on Dickson charge pump has been developed. Also, a single-stage rectifier circuit has been designed and fabricated in a standard 0.18- μm complementary metal oxide semiconductor (CMOS) process. Experimental results show that this rectifier can provide 1 V voltage supply at a PCE of 32%, -30 dBm incident RF power.

Keywords: Radio-frequency identification (RFID), passive transponder, rectifier, power conversion efficiency, charge pump

Classification: Integrated circuits

References

- [1] D. M. Dobkin, *The RF in RFID: passive UHF RFID in practice*, Newnes, USA, pp. 34–42, 2007.
- [2] K. Finkensteller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification 2nd Edition*, John Wiley & Sons, USA, pp. 34–42, May 2003.
- [3] P. V. Nikitin, et al., “Power reflection coefficient analysis for complex impedances in RFID tag design,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2721–2725, Sept. 2005.
- [4] Z. Zhu, B. Jamali, and P. Cole, “Brief comparison of different rectifier structures for HF and UHF RFID,” *The Adelaide Auto-ID Lab, The University of Adelaide*, April 2004.
- [5] U. Karthaus and M. Fischer, “Fully integrated passive UHF RFID transponder IC with 16.7- μW minimum RF input power,” *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1605, Oct. 2003.
- [6] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, “A 950-MHz rectifier circuit for sensor network tags with 10-m distance,” *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.
- [7] S. Mandal and R. Sarpeshkar, “Low-Power CMOS Rectifier Design for RFID Applications,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1177–1188, June 2007.

1 Introduction

RFID is an emerging technology used for object identification by means of radio waves. It is widely used in logistics, security and bioengineering. In the RFID system, the query unit (reader) transmits modulated RF signal or continual wave (CW) to a remote transponder (tag) consisting of an antenna and an integrated circuit (IC). In accordance with the power supply, the transponder can be completely passive, semi-passive, or active [1]. The passive RFID tag has been widely adopted because of its compact, inexpensive, and long-life characteristics. By contrast, the semi-passive and active tags support long-distance communication by using their internal power supply. Hence they correspondingly suffer from several disadvantages such as finite battery life, high cost, and large dimensions [2]. In fact, compared with active or semi-passive tags, the passive tag has an inherent drawback with regard to communication range due to a lack of sufficient power supply arising from its battery-less. Thus, the communication range of passive tags must be extended.

The maximum forward (Reader → Tag) communication range can be calculated using the Friis free-space formula, which is given by [3].

$$r_{max} = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r (1 - |s|^2)}{P_{th}}} \quad (1)$$

λ : wavelength

P_t : power transmitted by RFID reader

G_t : gain of the tag antenna

G_r : gain of the reader antenna

$|s|^2$: power transmission coefficient

P_{th} : threshold power of tag

As shown above, the communication range of passive RFID system strongly depends on the threshold power of the tag. Additionally, the threshold power is almost totally determined by power conversion efficiency and total power consumption of the tag. Thus, improving power conversion efficiency and reducing total power consumption are efficient ways to extend the communication range. PCE is an index of the power dissipated by the load compared to total incident power and defined as the ratio of the output DC power to the incident RF power as follows:

$$PCE = \frac{P_{DC}}{P_{RF}} \times 100\% \quad (2)$$

Rectifier is the key component circuit of passive RFID tag because PCE makes a strong contribution to the communication range. In other words, high PCE means long-range communication capability. Although various rectifier structures exist, only two kinds of rectifier are practical for UHF RFID transponder owing to UHF RFID having more constrains [4]. One is the gate cross-connected bridge structure, which does not utilize diode or diode-connected MOS transistor. It does not suffer from threshold voltage

penalty, so it can provide high PCE. However due to this structure having less capability to gain as high an output voltage as the charge pump structure, it is not suitable for the applications that require high voltage supply. The other is a Dickson charge pump structure, which converts incident RF signal power into DC power supply by using a voltage multiplier. We can use numerous stages to obtain as high a voltage level as we want. However the threshold voltage drop arising from diode-connected MOS transistor may result in low PCE. On the other hand, Schottky diodes with a low forward voltage drop are available, but unfortunately implementing them is expensive because they require extra mask layers and processing steps. To solve these problems, we propose a novel rectifier structure that is compatible with the standard CMOS process and can realize a high PCE as well as the desired output voltage.

The main goal of this project is to design a high sensitivity tag by improving PCE and refining total power consumption of tag. In this paper, we focus on discussing a high performance rectifier. This paper is organized as follows. Section 2 describes the proposed rectifier structure. Simulation and measurement were carried out and the results compared in section 3. Section 4 summarizes our overall conclusions.

2 Proposed rectifier circuits

To overcome the previously mentioned drawbacks of conventional rectifiers, we developed a novel rectifier structure on the basis of the following the concepts.

1. To solve the threshold voltage drop problem, diode and diode-connected MOS transistor should be avoided.
2. Reverse current from the storage capacitor to the antenna should be suppressed as much possible.
3. The size of the MOS transistor should be optimized with regard to channel resistance and parasitic capacitor.
4. The charge pump characteristic is desired to obtain high output voltage.

Figure 1 (a) shows the proposed circuit. Sub-circuit S_1 and S_2 consist of two pMOS transistor respectively, as shown on the right. In Fig. 1 (a), MOS transistor. M_a and M_b are not diode-connected MOS transistor so the forward voltage drop arising from threshold voltage can be largely saved as much as in a gate cross-connected structure [4]. To improve the potential reverse current drawback of the gate cross-connected circuit, M_b is added. This MOS transistor will largely limit reverse current from Node N_3 to Node N_1 . Moreover, due to the current being very small in the current situation, reducing the voltage drop arising from channel resistance is less important, so we prioritize diminishing the parasitic capacitor, which may result in power loss due to charging and discharging.

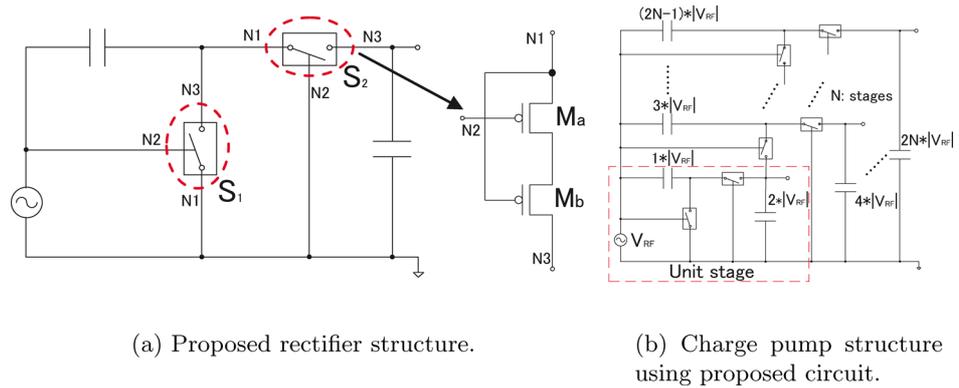


Fig. 1. Proposed rectifier structure and charge pump structure

By stacking the unit stage like in Fig. 1 (b), we can use different stages to obtain the output voltage level we want. The stage number not only affects the output voltage but also the PCE. Although the PCE of the rectifier may decline as stage number increases, the degradation of PCE can be tolerated because there is no threshold voltage penalty, but a small voltage drop arises from channel resistance over subcircuits S1 and S2 when the forward current is small. For this reason, the voltage booster we developed is more applicable for ultra-low power UHF RFID applications and more suitable for any standard CMOS process since it is only made up of MOS transistor.

3 Experimental results

To verify our design, a single-stage rectifier circuit has been fabricated in a $0.18\ \mu\text{m}$ five-metal standard CMOS process. Its active device area is $0.03\ \text{mm}^2$. The die is packaged into an 80 pin quad flat package (QFP). To decrease the reflections during UHF band, an impedance-controlled printed circuit board (PCB) also has been designed onto which the packaged device is directly mounted.

To measure the efficiency of the rectifier, a 953-MHz RF signal is applied to the rectifier IC, and matching networks are used to connect the test chip to an RF signal generator via a coaxial cable. A swing of RF power is fed into the rectifier input, and at the same time the output voltage and output current are measured at the output terminal of rectifier. Figure 2 shows the simulation and measurement results. In the simulation results, the PCE of the rectifier reaches 32% in the following conditions: Single-stage, $-30\ \text{dBm}$ P_{RF} , $1\ \text{V}$ $320\ \text{nA}$ load.

The simulation and experimental results agree well. because the output voltage is $1\ \text{V}$ at $-30\ \text{dBm}$ RF incident power and $0.32\ \mu\text{W}$ load, the threshold power of this device could be confirmed to be as low as $1\ \mu\text{W}$. Moreover, a high PCE of 32% is achieved. Note that the PCE decreases as incident RF power increase. This is because the rapid rise in forward current arising from increasing incident RF power may result in a large rise in forward voltage.

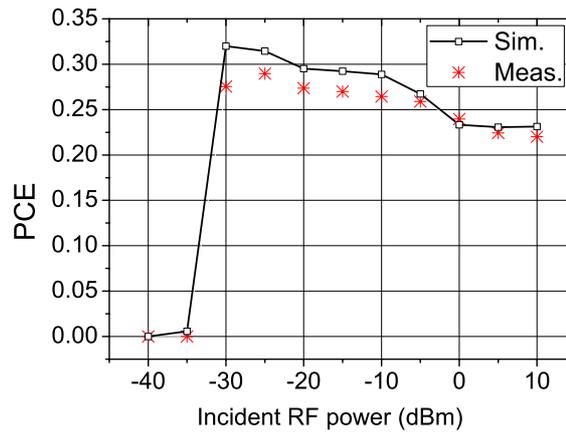


Fig. 2. Incident RF power dependence of PCE

Table I. Comparison of characteristics of the proposed and previously developed rectifiers

		ref. [5]	ref. [6]	ref. [7]	This Work
Power Conversion Efficiency		18%	16.6%	23.5%	32%
Condition	$V_{DC}[V]/I_{DC}[\mu A]$	1.5/1.5	1.5/0.4	0.5/4	1/0.32
	Die size[mm ²]	Unknown	0.64	Unknown	0.03
	Technology	0.5- μm	0.3- μm	0.18- μm	0.18- μm

Table I compares characteristics of the proposed and other rectifiers. This table proves the PCE and die area have been improved.

4 Conclusion

We presented a high-PCE rectifier structure. An arbitrarily desired output voltage can be obtained without suffering from the threshold voltage drop penalty. It is suitable for any standard CMOS process. A single-stage rectifier circuit has been fabricated in a standard 0.18 μm mixed signal CMOS process. The experimental results show a power conversion efficiency of 32%. This indicates a potential operating range of up to 30 m. We are convinced that the proposed rectifier structure is qualified to be a stronger candidate for UHF RFID rectifier circuit than the gate cross-connected bridge or Dickson charge pump structure.

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