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Tunable continuous-time ΔΣ modulator for switching power amplifier

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Abstract: A fully integrated tunable 4th-order multi-feedback bandpass delta-sigma modulator (BPDSM) fabricated in 0.25 um SiGe BiCMOS is presented. The input frequency can be tuned from 945 MHz to 988 MHz at 2.4 GHz fixed clock frequency. This modulator dissipates 110 mA from 3.3 V power supply. The peak signal-to-noise-ratio (SNR) of sinewave input is 41.1 dB in 10 MHz bandwidth and error vector magnitude (EVM) of 64QAM long term evolution (LTE) downlink is 3.16%, 3.59%, and 3.65% at different carrier frequencies.

Keywords: BPDSM, BiCMOS, LTE, Class-S, resonator

Classification: Integrated circuits

References

[1] A. Wentzel, C. Meliani, and W. Heinrich, "RF Class-S Power Amplifiers: State-of-the-Art Results and Potential," *IEEE MTT-S International Microwave Symposium Digest*, pp. 812–815, May 2010.

[2] H. Kobayashi, J. Hinrichs, and P. M. Asbeck, "Current-Mode Class-D Power Amplifiers for High Efficiency RF Applications," *IEEE MTT-S International Microwave Symposium Digest*, pp. 939–946, May 2001.

[3] T. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1091–1094, May 2007.

[4] R. Leberer, R. Reber, and M. Oppermann, "An AlGaN/GaN Class-S Amplifier for RF-Communication Signals," *IEEE MTT-S International Microwave Symposium Digest*, pp. 85–88, June 2008.

[5] J. Ketola, J. Sommarek, J. Vankka, and K. Halonen, "Transmitter utilizing bandpass delta-sigma modulator and switching mode power amplifier," *Proc. 2004 Int. Symp. Circuits and Systems*, May 2004.

[6] Y. Zhu, S. F. Al-Sarawi, C. C. Lim, and M. J. Liebelt, "Fourth-order discrete-time variable centre frequency bandpass sigma-delta modulator," *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 820–823, Dec. 2006.

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[7] "Technical Specification Group Radio Access Network; Base Station radio transmission and reception," 3GPP TS 36.104 V8.4.0, Dec. 2008.

1 Introduction

The power added efficiency (PAE) of RF power amplifier in base-station is one of the key evaluating factors for implementing low power consuming wireless communication systems [1]. The high efficiency power amplifiers (Pas) are recently focusing on switch-mode operation [2, 3, 4]. One possible solution for implementing high linearity and high efficiency transmitter is Class-S amplifier [5]. In typical Class-S concept can be classified three main parts of whole system as shown in Fig. 1. The continuous-time (CT) BPDSM converts input RF signal to single-bit digital-RF sequence. The digital signal is then amplified by means of a highly efficient power switching stage. An analog reconstruction filter at the output of this switching amplifier reconstructs the non-constant envelope signal [1]. This paper describes the CT BPDSM which plays a key component in the Class-S concept.

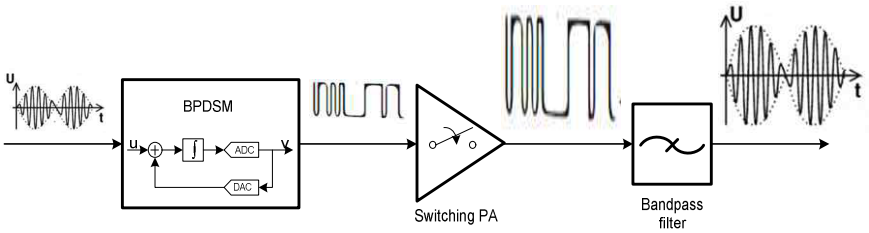

Fig. 1. Concept of Class-S power amplifier

2 System level design

A modulator topology for designing an LC bandpass delta-sigma modulator is presented in Fig. 2. This is 4th-order multi-feedback architecture for reducing the excess loop delay (ELD). Fig. 2 shows a system with return-to-zero (RZ) DAC and half-delayed-return-to-zero (HRZ) DAC feedback pulses and four loop coefficients k4r, k4h, k2r, k2h which provide four degree of freedom for implementing a desired fourth-order loop transfer function. The modulator

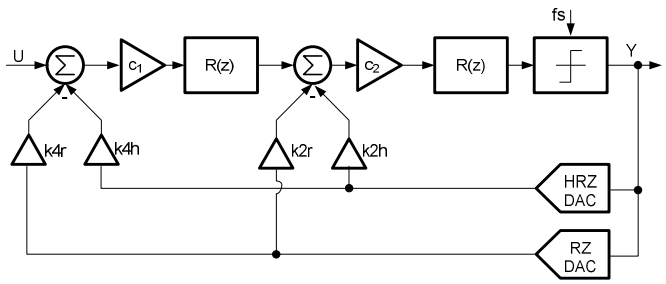

Fig. 2. 4th order multi-feedback BPDSM architecture

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consists of two Q-enhanced LC resonators. They are fed with three currents: the first is proportional to the input voltage of the preceding trans-conductor, the others are feedback currents with DAC amplitude of k during the high output of the RZ latch and HRZ latch, respectively.

The proposed 4$^{\text{th}}$-order modulator has tunable resonator R(z). It use a discrete-time (DT) loop filter based on a tunable resonator expressed in the z-domain as [6]

$$R(z) = -\frac{az+1}{z^2+2az+1} \tag{1}$$

where a is the only tunable parameter between -1 and 1.

Assuming single feedback and feedback coefficients are unity, the loop filter open loop transfer function is described as equation (2).

$$H(z) = \frac{ac_2z^3 + (2a^2c_2 + c_2 - a^2c_1c_2)z^2 + (3ac_2 - 2ac_1c_2)z + c_2 - c_1c_2}{(z^2+2az+1)^2} \tag{2}$$

In order to DT to CT conversion of 4$^{\text{th}}$-order multi-feedback modulator using the impulse invariant transformation, the DAC feedback impulse response of RZ and HRZ are calculated as

$$R_{RZ}(s) = \frac{1-e^{-\frac{T_s}{2}s}}{s}, \quad R_{HRZ}(s) = \frac{e^{-\frac{T_s}{2}s} - e^{-T_s s}}{s} \tag{3}$$

where T_s is the sampling period.

The system level simulation is performed and the result is shown in Fig. 3. The carrier over-sampling ratio (OSR) is 2.5, the tunable parameter a is 0.85, the gain of c_1, c_2 are 0.2792, 0.775, respectively. The only non-ideality of Q-factor (50) is applied in this case. The SNR result of this system is 43.1 dB at 1.0 V peak input amplitude.

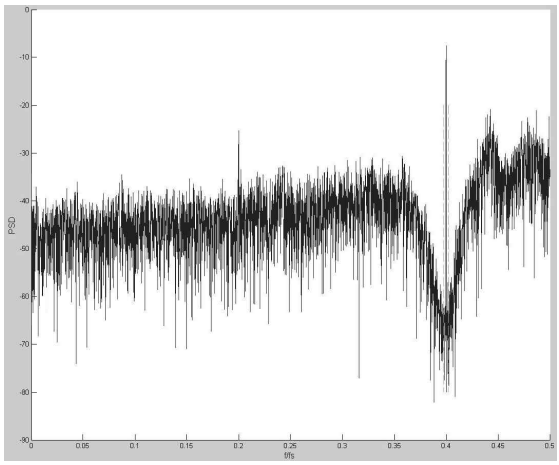

Fig. 3. System-level simulation result of BPDSM

3 Circuit level implementation

The resonator is the major component of passing the wanted band signal in BPDSM. The schematic of an LC resonator with negative resistor Q-enhancement is shown in Fig. 4. The input voltage is converted to current

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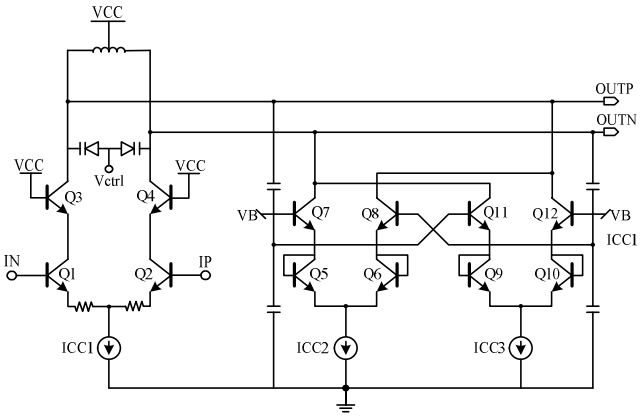

Fig. 4. Schematic of LC resonator

using emitter degenerated resistor for linearization and injected into LC tank. The center frequency of the LC resonator is tuned by varying the control voltage Vctrl of the reverse-biased p-n junction varactors. The Q of the semiconductor spiral inductor is in the range of 10, therefore it reduce the SNR of whole BPDSM system. Large Q-enhancement circuit is added using negative resistors.

The full chip BPDSM is designed in 0.25 um SiGe BiCMOS process. The size of BPDSM is 1.5 mm × 1.0 mm including the pads as shown in Fig. 5. Bottom side is input, right is clock signal input, and the top is output nodes.

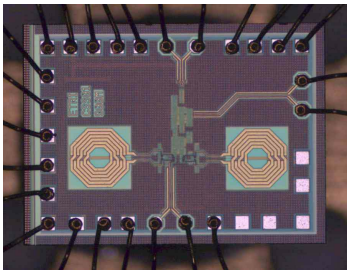

Fig. 5. Photograph of the BPDSM chip

4 Measurement results

The measurement setup consists of two signal generators for input and clock signal, the spectrum analyzer for frequency response, and vector signal analyzer for modulation characteristic.

The tunable output spectrum for an input signal frequency of 945∼988 MHz and clock frequency of 2.4 GHz can be seen in Fig. 6.

Fig. 7 shows the SNR and discrete-time (DT) coding efficiency characteristics. The measured peak-SNR is 41.1 dB in 10 MHz bandwidth for sinewave signal.

In order to test the conformance of BPDSM as a mobile telecommunication, a real LTE downlink signal which has 11 dB peak-to-average-ratio (PAPR) is applied and both of EVM and spectrum mask are measured. Fig. 8 shows the output signal constellation of 64QAM LTE and spectrum

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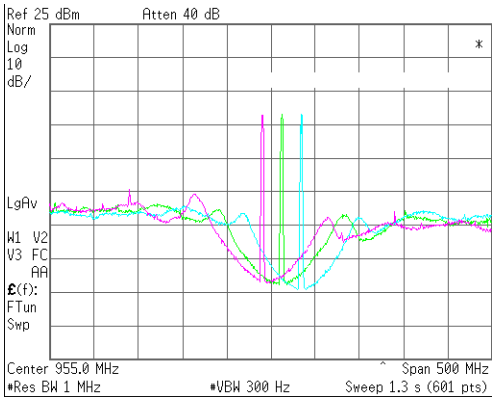

Fig. 6. Tunable frequency response of BPDSM

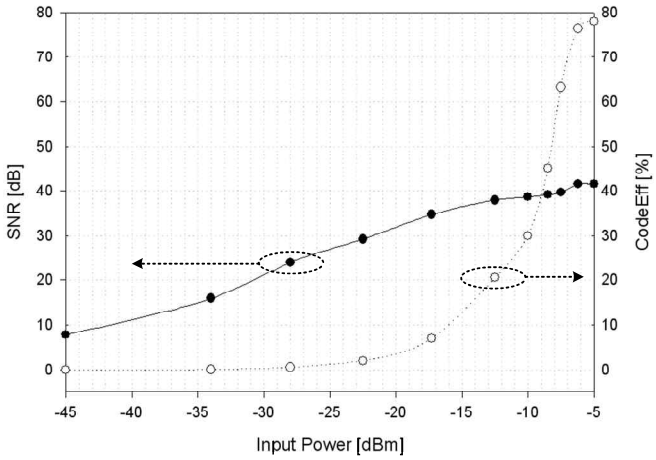

Fig. 7. Measured SNR and DT coding efficiency for sinewave input signal

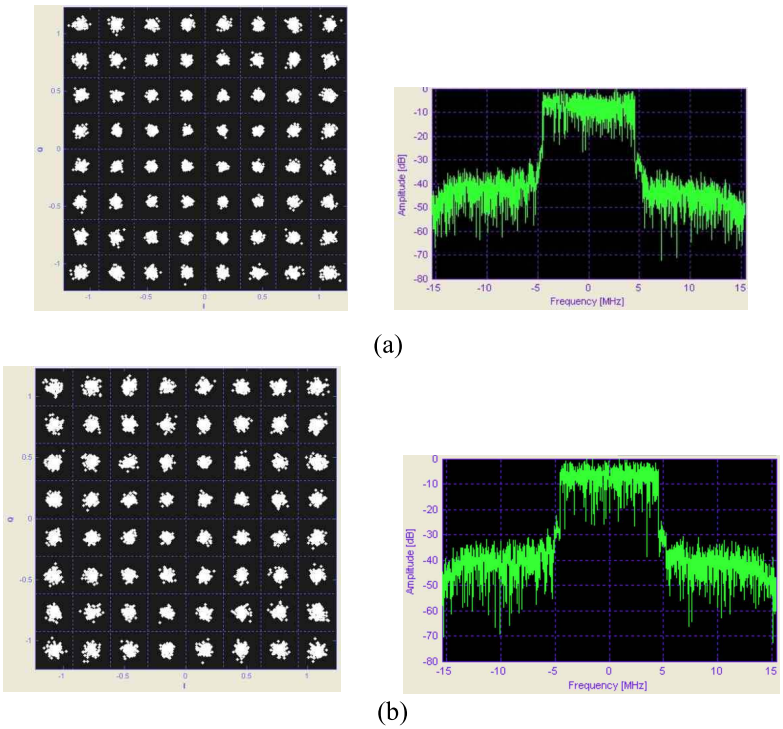

Fig. 8. Output characteristics of 64QAM LTE signal; (a) 945 MHz, (b) 955 MHz

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Table I. Performance summary

Parameter	Results
Process	0.25 um SiGe BiCMOS
Input frequency range	945-988 MHz
Sampling clock frequency	2.4 GHz
Power consumption	363 mW
Output voltage swing (differential)	1.3 Vp-p
SNR_peak (BW=10 MHz)	41.1 dB @ 955 MHz
EVM (64QAM LTE)	3.16 % @ 945 MHz
	3.59 % @ 955 MHz
	3.65 % @ 988 MHz

mask. The measured EVM is 3.16% at 945 MHz and 3.59% at 955 MHz.

The measured performance summary of BPDSM full chip is given in Table I.

5 Conclusion

An integrated tunable notch frequency BPDSM for 900 MHz band in a 0.25 um SiGe BiCMOS has been presented. In this work, tunable resonator with Q-enhancement circuit, multi-feedback current DAC, and comparator are proposed. The modulator clocked at 2.4 GHz has a tuned notch in 945∼988 MHz frequency range. EVM characteristic of 3.16%, 3.59%, 3.65% meet the 8% of 64QAM LTE downlink specification [7]. The measured performance of entirely integrated BPDSM full chip shows the capability to apply the Class-S power amplifier base-station.

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