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A Novel 100 ppm/°C current reference for ultra-low-power subthreshold applications

Bogoda A. Indika U. K.[1a)], **Daisuke Kanemoto**[2], **and Kenji Taniguchi**[1]

[1] *Division of Electrical, Electronic and Information Engineering, Osaka University, 2–1 Yamadaoka, Suita, Osaka, 565–0871 Japan*

[2] *Graduate School of Information Science and Electrical Engineering Kyushu University, Nishi ku, Moto-Oka, Fukuoka, Japan*

a) *indika@si.eei.eng.osaka-u.ac.jp*

Abstract: We proposed a novel temperature-compensated, ultra-low-power current reference based on two β-multipliers whose resistors are replaced by nMOS devices operated in the deep triode region. The circuit, designed by a 0.25 µm CMOS process, produces an output reference current of 13.7 nA at room temperature. Simulated results show that the temperature coefficient of the output is less than 100 ppm/°C in the range from −20°C to 80°C and the average power dissipation is 0.9 µW.

Keywords: current reference, subthreshold, low-power, temperature coefficient, CMOS

Classification: Integrated circuits

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1 Introduction

The increasing demand for portable electronic devices, microsensors, and biomedical sensors makes the power-efficient circuits increasingly important. As a result, subthreshold circuits are attracting attention because of their ultra-low-power consumption. One of the main drawbacks of the circuits, however, is the exponential temperature dependence of drain current, which makes the design of subthreshold circuits quite difficult. The implementation of a proper temperature-independent current source into a chip could significantly suppress the temperature dependence of the subthreshold circuit performance. Most current references based on PTAT use bipolar transistors [1, 2], while those using parasitic bipolar transistors available in the standard CMOS process show poor performances, require a large design area, and consume relatively large power. Therefore, the current references [1, 2] based on CMOS-only designs cannot be used in ultra-low-power applications. Another approach to current reference [3] based on β-multiplier, which requires resistors and consumes several dozen microwatts is still not suitable for CMOS-only and ultra-low-power designs. To overcome these problems, CMOS-only current references using subthreshold circuits have been demonstrated [4, 5]. The CMOS-only current reference proposed by Oguey and Aibischer [4] consumes very little power, and the circuit structure is very simple. However, the output reference current of the circuit is proportional to $T^{0.4}$, where T represents the absolute temperature and is not suitable to be used as a temperature-independent current source. The current reference [5] has shown reasonable temperature immunity and low-power consumption, although the circuit techniques are quite complex and the temperature coefficient is not small enough for high accuracy applications.

In this paper, we proposed a new and simple current reference circuit composed of two current subcircuits that have positive but different temperature coefficients. The operation principle and computer-based simulation results are presented. The output reference current is fairly insensitive to temperature and supply voltage variations. The power consumption of the proposed circuit is less than 1 µW. Therefore, the proposed circuit is ideal to be used as a temperature-independent current source, which will help circuit designers overcome the exponential temperature dependence of subthreshold circuit performance.

2 Proposed current reference

2.1 Operation principle

The schematic of the proposed current reference circuit is shown in Fig. 1. The proposed circuit consists of two current source subcircuits, a current subtract stage and an output stage. Each current source generates a different current with a different temperature coefficient. In the current subtract stage, the currents generated by the current sources are multiplied by proper coefficients and subtracted so that the resultant current has the minimum temperature dependence. The output stage mirrors the resultant current to

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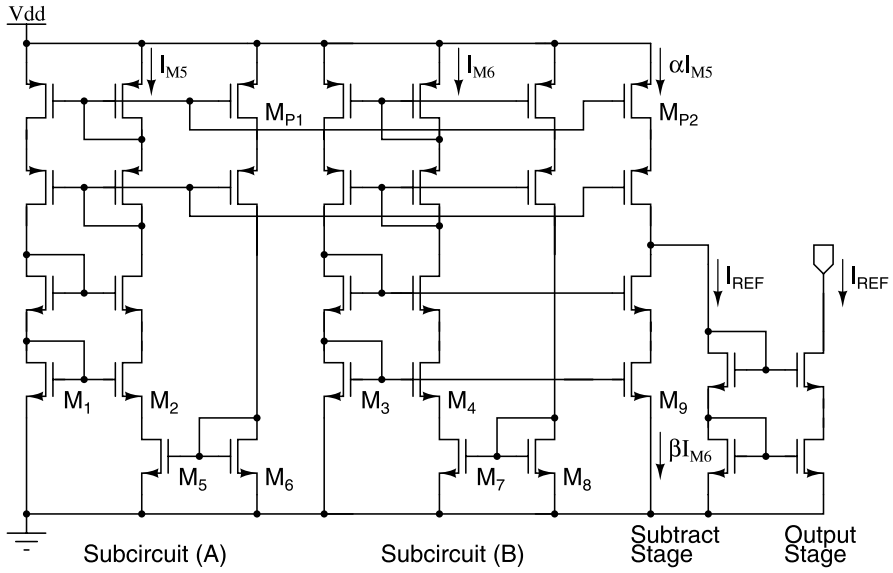

Fig. 1. Schematic of Proposed Current Reference.

the preferable output reference current.

2.2 Current source subcircuits

The current source subcircuits (subcircuit (A) and subcircuit (B) in Fig. 1) are based on a well known β-multiplier circuit; their resistors are replaced by nMOS devices (M_5 and M_7) operated in the deep triode region. The bias voltages for M_5 and M_7 are generated by diode-connected nMOS devices, M_6 and M_8, operated in the saturation region, respectively. All other transistors used in the proposed circuit are operated in the subthreshold region.

The drain current of the MOSFETs operated in the subthreshold region is mainly composed of subthreshold leakage current and can be expressed as follows [5]:

$$\begin{aligned} I_D &= K I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)\left\{1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right\} \\ I_0 &= \mu C_{OX}\left(\eta-1\right)V_T^2 \end{aligned} \tag{1}$$

where K is the aspect ratio ($= W/L$), η is the subthreshold slope factor, $V_T = (K_B T/q)$ is the thermal voltage, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, k_B is the Boltzmann constant, and q is the elementary charge. For values of $V_{DS} > 4V_T$ (approximately 100 mV at room temperature), I_D becomes almost independent of V_{DS}. Therefore, Eq. (1) can be modified as follows.

$$I_D = K I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \tag{2}$$

In the subcircuit (A) in Fig. 1, the relationship between the gate-source voltages of M_1, M_2 ($V_{GS,1}$, $V_{GS,2}$) and drain-source voltage of M_5 ($V_{DS,5}$) can be expressed as

$$V_{GS,1} = V_{DS,5} + V_{GS,2} \tag{3}$$

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All pMOS devices in subcircuit (A) share the same aspect ratios, resulting in equal drain currents through M_1, M_2, M_5, and M_6. From Eqs. (2) and (3), we have

$$V_{DS,5} = \eta V_T \ln\left(\frac{K_2}{K_1}\right) - \Delta V_{TH} \tag{4}$$

where ΔV_{TH} $(= V_{TH,2} - V_{TH,1})$ is the difference between the threshold voltages of M_1 and M_2. The value of ΔV_{TH} can be approximated by

$$\Delta V_{TH} = \gamma\left(\sqrt{2\Phi_F + V_{DS,5}} - \sqrt{2\Phi_F}\right) \tag{5}$$

where γ is the body-effect coefficient, $\Phi_F = V_T \ln(N_{sub}/n_i)$ is the Fermi potential, N_{sub} is the doping concentration of the substrate, and n_i is the intrinsic concentration of silicon. The drain current of M_5 operated in the deep triode region can be given by

$$I_{M5} = \mu C_{OX}\left(\frac{W}{L}\right)_5 (V_{GS,5} - V_{TH,5})\, V_{DS,5} \tag{6}$$

The temperature coefficient $(\frac{1}{I}\frac{\partial I}{\partial T})$ of the current given in Eq. (6) can be shown by

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{1}{(V_{GS,5} - V_{TH,5})}\frac{\partial (V_{GS,5} - V_{TH,5})}{\partial T} + \frac{1}{V_{DS,5}}\frac{\partial V_{DS,5}}{\partial T} \tag{7}$$

and the temperature dependence of mobility μ can be given by

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{8}$$

where $\mu(T_0)$ is the carrier mobility at room temperature and m is a constant.

The drain current of M_6 operated in the saturation region is given by

$$I_{M6} = \mu C_{OX}\left(\frac{W}{L}\right)_6 (V_{GS,6} - V_{TH,6})^2 \tag{9}$$

Because $I_{M5} = I_{M6}$ and both M_5 and M_6 share the same gate voltage, the temperature coefficient of I_{M5} can be calculated using Eq. (9) as follows

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{2}{(V_{GS,5} - V_{TH,5})}\frac{\partial (V_{GS,5} - V_{TH,5})}{\partial T} \tag{10}$$

Note that we assume $V_{TH,5} = V_{TH,6}$.

By using Eqs. (4) and (5), the temperature coefficient of $V_{DS,5}$ can be approximated by

$$\frac{1}{V_{DS,5}}\frac{\partial V_{DS,5}}{\partial T} = \frac{1}{T}\left\{1 + \frac{\eta V_T \ln(K_2/K_1)}{\eta V_T \ln(K_2/K_1) - \Delta V_{TH}}\right\} \tag{11}$$

From Eqs. (7), (8), (10), and (11), the temperature coefficient of the output current of subcircuit (A), I_{M5}, can be expressed by

$$\frac{1}{I_{M5}}\frac{\partial I_{M5}}{\partial T} = \frac{1-m}{T} + \frac{1}{T}\left\{\frac{\eta V_T \ln(K_2/K_1)}{\eta V_T \ln(K_2/K_1) - \Delta V_{TH}}\right\} \tag{12}$$

The value of m is approximately 1.5 for ordinary nMOS devices. Consequently, the temperature coefficient given in Eq. (12) is positive.

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Since both current sources have the same structure, the temperature coefficient of the output current of subcircuit (B), I_{M7}, can be calculated in the same manner. From a simple calculation, it can be seen that for a given temperature, the temperature coefficient given in Eq. (12) decreases with an increase in the (K_2/K_1) ratio. In the proposed design, we selected the aspect ratios of K_1 - K_4, such that $(K_2/K_1) > (K_4/K_3)$. Therefore, the current source subcircuit (A) has a smaller temperature coefficient compared with that of subcircuit (B).

Assume that the aspect ratios of M_{P1}:M_{P2} and M_4:M_9 are 1:α and 1:β, respectively. Thus, the resultant current of the subtract stage can be given by

$$I_{REF} = \alpha I_{M5} - \beta I_{M7} \tag{13}$$

By choosing proper values for α and β, the temperature dependence of I_{REF} can be eliminated.

3 Results

The proposed current reference was designed and simulated in the 0.25 µ CMOS process at a supply voltage of 2.5 V. In the proposed design, the ratios of (K_2/K_1) and (K_4/K_3) were set to 1.55 and 1.45, respectively. The current mirror ratios M_{P1}:M_{P2} and M_4:M_9 were 31:24 and 1:1, respectively.

Figure 2 (a) shows the simulated output current of the two current sources. As expected, both currents have a positive temperature coefficient, and the

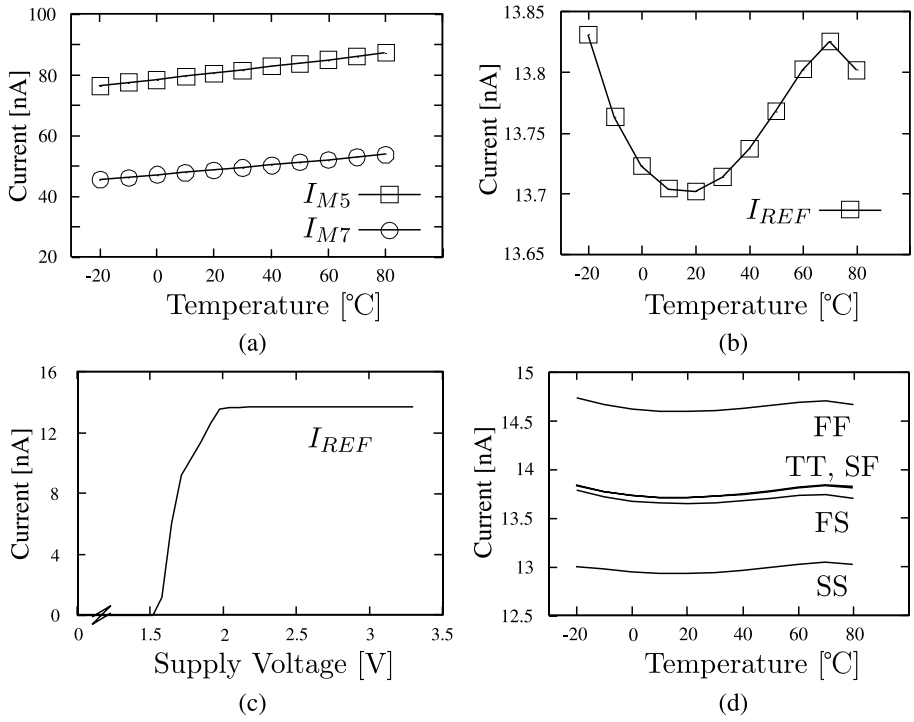

Fig. 2. Simulation Results: (a) Temperature dependence of I_{M5} and I_{M7}, (b) temperature dependence of I_{REF}, (c) power supply dependence and (d) simulated reference current in different process corners.

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Table I. Performance Summary.

	This Work	[4]	[5]
Process	0.25 µm	2 µm	0.35 µm
Temperature Range	−20 - 80°C	−40 - 80°C	0 - 80°C
Temperate Coefficient	95 ppm/°C	1100 ppm/°C	520 ppm/°C
Power Consumption	0.9 µW	0.07 µW	1 µW
I_{REF}	13.7 nA	1 - 100 nA	96 nA

temperature coefficient decreases with an increase in the current. The temperature dependence of the output reference current I_{REF} is shown in Fig. 2 (b). The temperature coefficient is approximately 95 ppm/°C in the temperature range from −20°C to 80°C. Figure 2 (c) shows the power supply dependence of the reference current. As is clear from Fig. 2 (c), the proposed current reference operates even at 2 V and this voltage could be reduced further by using operational amplifiers instead of cascode current mirrors at the expense of power consumption.

We simulated the proposed circuit using different process corners to investigate the effect of process variation on the reference current. The results are shown in Fig. 2 (d). The difference in I_{REF} at the process corners of TT, SF, and FS is negligible. In addition, I_{REF} at each process corner shows almost the same temperature dependence, because as seen from Eq. (12), the temperature coefficient of I_{M5} and I_{M7} has little process dependence and could be seen as negligible. Therefore, the temperature coefficient of the reference current also has little process dependence and could be seen as negligible.

Table I compares the performance of the current reference described in this paper with that of previously published current references. The current reference proposed in this paper shows the best performance in temperature dependence. Although the current reference circuit [4] has demonstrated low power consumption, our design is 10 times superior in temperature dependence.

4 Conclusion

A novel ultra-low-power current reference using subthreshold circuits is presented. The proposed circuit uses only CMOS devices; therefore, it can be implemented in the standard CMOS process without using parasitic bipolar transistors or resistors. The proposed circuit is designed and simulated in the 0.25 µm CMOS process. The operation principle and the simulation results are presented. The simulation results show that the output reference current I_{REF} is approximately 13.7 nA at room temperature, and that the temperature coefficient of I_{REF} is smaller than 100 ppm/°C for the temperature range from −20°C to 80°C. The average power consumption is 0.9 µW. Furthermore, the proposed current reference shows temperature independent characteristics in all process corners. This implies that the proposed circuit is ideal to be used as a current reference to compensate for temperate dependence in ultra-low-power, subthreshold designs.

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