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A wideband high-resolution time-interleaved sigma-delta modulator with VCO-based quantizer

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Abstract: A time-interleaved sigma-delta modulator with VCO-based quantizer for next generation wireless applications is presented. This proposed modulator firstly introduces the VCO-based multibit quantizer into the time-interleaved sigma-delta modulator, which can achieve the improvement of the signal bandwidth and signal-to-noise ratio simultaneously. Moreover, these performance metrics have no adverse effects on power consumption, which is more suitable for wireless applications. A two-channel proposed modulator is taken as an example, and the simulation results show that the proposed modulator achieves a signal-to-noise ratio of 112.1 dB over a 4.7 MHz signal bandwidth with a clock frequency of 300 MHz, which improves 100% in the range of signal bandwidth and 21 dB in the signal-to-noise ratio compared to the conventional sigma-delta modulator with the same clock frequency and power consumption.

Keywords: time-interleaved, VCO-based quantizer, sigma-delta modulator

Classification: Integrated circuits

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1 Introduction

In the wireless applications, there is increasing demand for wideband and high-resolution data converters. Sigma-delta ADCs can deliver high performance with low power consumption, and it is hence the ADC architecture of choice in next generation wireless applications [1, 2]. However, to be extended to new telecommunication areas, sigma-delta ADCs typically require megahertz range signal bandwidth with a high sampling clock [3]. With high sampling clocks, the CMOS implementation of modulators is problematic due to the high frequency limitations of the op-amps and sampling switches. Also, with higher signal bandwidth, the signal-to-noise ratio (SNR) of the modulator will significantly degrade [4].

In this paper, to solve the above problems, a time-interleaved sigma-delta modulator with VCO-based quantizer is presented. This proposed modulator introduces the VCO-based multibit quantizer into the time-interleaved sigma-delta modulator, which achieves the improvement of the signal bandwidth and SNR simultaneously. Furthermore, all these metrics have no adverse effects on power consumption. The rest of the paper is organized as follows. In section 2 the proposed modulator is analyzed. Simulation results are indicated in section 3 and section 4 concludes the paper.

2 The proposed sigma-delta modulator

2.1 The basic architecture

To analyze the architecture of the proposed modulator, a two-channel proposed modulator is described in this paper. As is known, the conventional

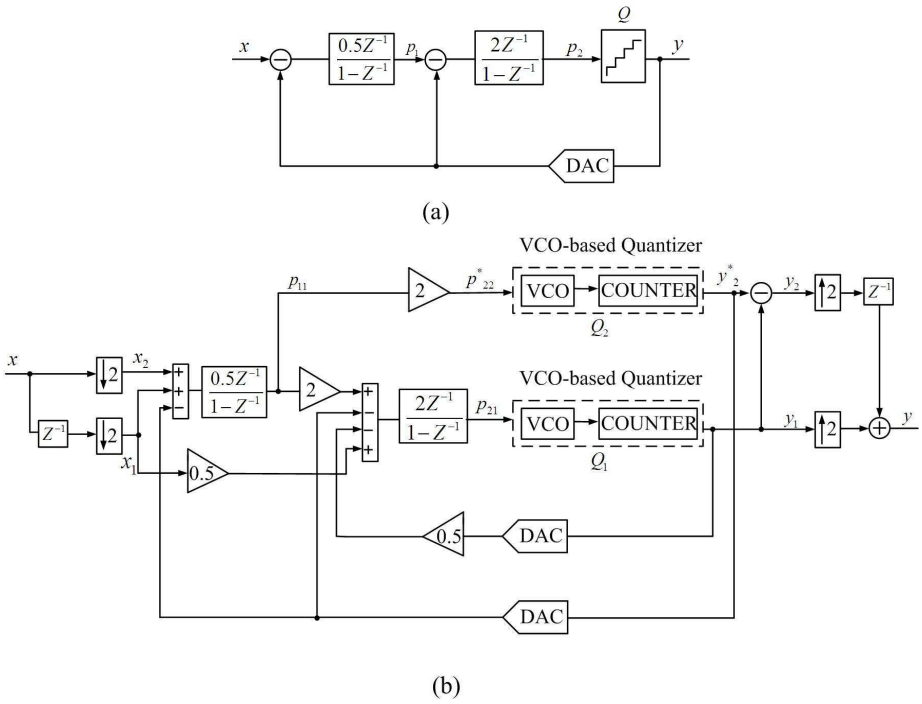

Fig. 1. Architecture of the conventional and proposed modulator (a) conventional (b) proposed.

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second-order sigma-delta modulator is shown in Fig. 1 (a), where $p_1(n)$ and $p_2(n)$ represent the output of the first and second integrators, respectively. In this case, only one output is generated for each time slot n by quantizing the output of the second integrator. However, the proposed modulator is shown in Fig. 1 (b), and the integrator outputs $p_{11}(n)$ and $p_{21}(n)$ that each correspond to $p_1(2n-1)$ and $p_2(2n-1)$ are given as below,

$$p_{11}(n) = p_{11}(n-1) + 0.5 \cdot [x_1(n-1) + x_2(n-1) - y_1(n-1) - y_2(n-1)] \quad (1)$$

$$p_{21}(n) = p_{21}(n-1) + 2 \cdot [0.5x_1(n-1) + 2p_{11}(n-1) - 1.5y_1(n-1) - y_2(n-1)] \quad (2)$$

The first output of the proposed modulator $y_1(n)$ is obtained by quantizing the integrator output $p_{21}(n)$. Furthermore, to obtain the second output $y_2(n)$, it is necessary to take a look at the successive second integrator output of Fig. 1 (a), which is given as,

$$p_2(n+1) = p_2(n) + 2 \cdot [p_1(n) - y(n)] \quad (3)$$

Thus, the successive integrator output of the proposed modulator corresponding to $p_2(2n)$ is written as,

$$p_{22}(n) = p_{21}(n) + 2 \cdot [p_{11}(n) - y_1(n)] \quad (4)$$

However, directly using Eq. 4 for the input of the second quantizer will lead to quantizer domino due to the output term $y_1(n)$. Therefore, in the proposed architecture, the incomplete integrator output $p^*_{22}(n)$ is used as the input of the second quantizer Q_2, that is,

$$p^*_{22}(n) = 2 \cdot p_{11}(n) \quad (5)$$

Noticing $y_2(n) = Q_2[p_{22}(n)]$, the quantization of Eq. 4 leads to the incomplete second modulator output $y^*_2(n)$, which is given by,

$$y^*_2(n) = y_2(n) + y_1(n) \quad (6)$$

It is shown that the incomplete output is a sum of the complete first and second outputs. Thus, the complete second output $y_2(n)$ can be simply obtained by subtracting $y_1(n)$ from Eq. 5 in the digital domain.

On the other hand, the VCO-based quantizer, shown in Fig. 1 (b), has the function of first-order noise shaping to improve the noise shaping order of the modulator. It consists of a VCO and a binary counter with a reset. An output pulse of a VCO is generated when its internal phase value reaches the value of $2n\pi$. The internal phase shift of $P(z)$ is proportional to an input voltage of $X(z)$. Assuming K is a gain constant and P_0 is an initial phase, that is,

$$P(z) = K \cdot X(z) + P_0 \quad (7)$$

The VCO output pulses are counted during a sampling period, where the counter is reset following each sampling period. The count of $Y(z)$ is a quantized value for $P(z)$. A residual phase shift at the end of the sampling

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period is quantization noise $Q(z)$, which is given by,

$$Q(z) = P(z) - 2\pi Y(z) \tag{8}$$

$Q(z)$ is held to be the initial phase shift for the next sampling period, that is, $P_0 = z^{-1}Q(z)$. From the above equations, it can be obtained a transfer function of the VCO quantizer, which is given as,

$$Y(z) = (2\pi)^{-1}[K \cdot X(z) + (1 - z^{-1}) \cdot Q(z)] \tag{9}$$

Eq. 9 shows that the quantization noise $Q(z)$ is shaped by a first-order noise shaping filter. Moreover, by increasing the quantizer bit, a dynamic range or an SNR is theoretically improved by 6 dB/bit.

2.2 The transfer function

From the above analysis, the transfer function of the proposed modulator shown in Fig. 1 (b) is obtained from the z-domain representation of the first and second outputs, that is,

$$P_{11}(z) = [X_1(z) + X_2(z) - Y_1(z) - Y_2(z)] \cdot \frac{0.5z^{-1}}{1 - z^{-1}} \tag{10}$$

$$P_{21}(z) = [2P_{11}(z) - 0.5Y_1(z) + 0.5X_1(z) - Y_1(z) - Y_2(z)] \cdot \frac{2z^{-1}}{1 - z^{-1}} \tag{11}$$

$$Y_1(z) = P_{21}(z) + (1 - z^{-1}) \cdot E_1(z) \tag{12}$$

$$Y_2(z) = 2P_{11}(z) + (1 - z^{-1}) \cdot E_2(z) - Y_1(z) \tag{13}$$

where $E_1(z)$ and $E_2(z)$ are the quantization errors of the quantizers $Q1$ and $Q2$, respectively. By combining the two outputs using poly phase decomposition, the below equation is obtained,

$$Y(z) = z^{-1}Y_2(z^2) + Y_1(z^2) \tag{14}$$

Thus, the final output expression is given as below,

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^3 \cdot [z^{-1}E_2(z^2) + E_1(z^2)] \tag{15}$$

It can be seen that the proposed modulator achieves two-channel time-interleaved, which leads to the improvement of the signal bandwidth, and also the quantization error of the proposed modulator is third-order shaped. Therefore, the range of signal bandwidth improves 100% and the improvement in the SNR is 21 dB compared to the conventional second-order modulator shown in Fig. 1 (a), when both modulators are operating at the same internal clock rate.

3 Simulation results

The performance of the proposed modulator is compared with the conventional two-order sigma-delta structures through behavioral level simulations. A flash 2-bits quantizer was used for the conventional second-order modulator shown in Fig. 1 (a), whereas a VCO-based 2-bits quantizer was used for

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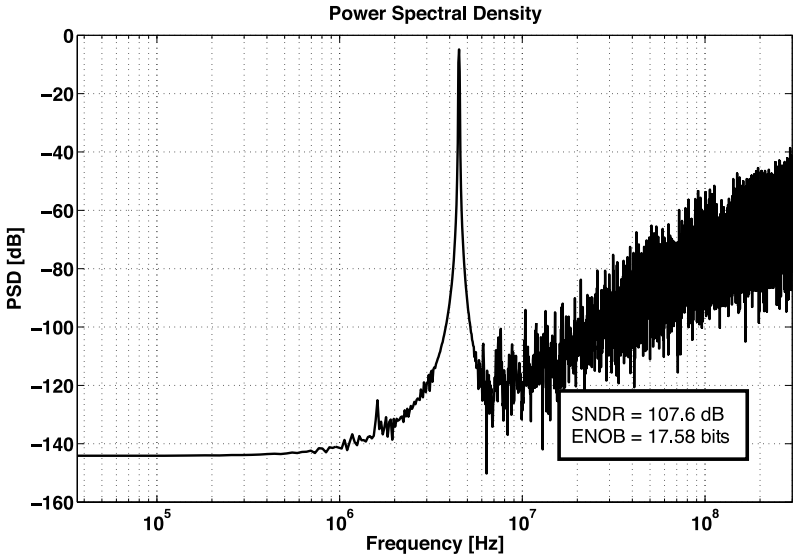

Fig. 2. Output spectrum of the proposed modulator.

the proposed structure.

Fig. 2 shows the output spectrum of the proposed modulator with −6 dBFS, 4.1 MHz sinusoidal input. The simulation comparison results of key parameters of the two modulators are listed in Table I. For both modulators, the internal clock frequency was set to 300 MHz. However, the effective clock frequency of the proposed modulator is $2f_s$, doubling the effective OSR of the modulator. Thus, the signal bandwidth of the proposed modulator improves 100% under the same OSR when compared to the conventional modulator. Also, the proposed modulator with VCO-based quantizer has a third-order noise shaping characteristics to further improve the SNDR of the modulator. As expected, the SNDR improvement of the proposed modulator was approximately 21 dB, almost 3.5 bits.

Table I. Performance summary of the conventional and proposed modulator.

Parameter	This work	Conventional
Supply Voltage (V)	1.2	1.2
Signal bandwidth (MHz)	4.7	2.4
Clock frequency (MHz)	300	300
Effective sampling rate (MHz)	600	300
Effective OSR	64	64
Input range (V)	0.8	0.8
Peak SNR (dB)	112.1	91.6
Peak SNDR (dB)	107.6	87.3
DR (dB)	116.3	95.2
Power consumption (mW)	15	13
Technology	65 nm	65 nm

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4 Conclusion

A time-interleaved sigma-delta modulator with VCO-based quantizer is presented. This proposed modulator introduces the VCO-based multibit quantizer into the time-interleaved sigma-delta modulator to achieve the improvement of the signal bandwidth and signal-to-noise ratio simultaneously. Finally, all these design metrics have no adverse effects on power consumption.

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