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An efficient radix-4 Quasi-cyclic shift network for QC-LDPC decoders

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Abstract: A Radix-4 Quasi-cyclic shift network (QSN) for reconfigurable QC-LDPC decoders is presented in this paper. A complexity reduction technique is described to reduce the total gate count at each stage in addition to the fact that Radix-4 logarithmic barrel shifter naturally offers less number of stages compared to Radix-2. The proposed Radix-4 QSN architecture supports various code rates and all sizes of sub matrices. Moreover, a novel Radix-4 signal generator is proposed which is particularly an essential element for reconfigurable LDPC decoders. The synthesis, placement and routing (P & R) of the proposed network is performed using TSMC 90-nm standard cell CMOS technology. The implementation results shows that the proposed network outperforms its predecessors by about 11% and 38% in terms of area and clock frequency respectively.

Keywords: shift network, LDPC, multi-size barrel shifter, Radix-4

Classification: Electron devices, circuits, and systems

References

[1] S. Hwang and H. Lee: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **21** (2013) 1337.

[2] S. Kim, G. E. Sobelman and H. Lee: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **19** (2011) 1099.

[3] D. Oh and K. Parhi: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **18** (2010) 85.

[4] X. Peng, X. Zhao, Z. Chen, F. Maehara and S. Goto: IEICE Trans. Fundamentals **E93-A** (2010) 2551.

[5] X. Chen, S. Lin and V. Akella: IEEE Trans. Circuits Syst. II **57** (2010) 782.

[6] J. R. Hauser: in *Handbook of Semiconductor Manufacturing Technology*, ed. R. Doering and Y. Nishi (CRC Press, Bosa Roca, 2007) 2nd ed. 1-21.

1 Introduction

Low-density parity-check (LDPC) codes, are widely used in modern communication systems. The hardware implementation of LDPC decoder is gener-

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ally very complex. The switch network is one of the sources of complexity and critical path within LDPC decoders [1, 2]. QC-LDPC codes simplify the switch network. QC-LDPC code eliminates the random shifting (or permutation) and only cyclic shifting is required [1]. The conventional barrel shifter architectures are not sufficient for modern reconfigurable LDPC decoders because conventional barrel shifters don't support cyclic shifting when the number of inputs is less than the network size or they don't support LDPC decoders with multi-size sub matrices [3, 4, 5].

Recently, many switch network designs are presented for reconfigurable QC-LDPC decoders. Some of the efficient designs based on Benes network, Banyan network and Barrel shifters are given in [3, 4] and [5], respectively. To the best of our knowledge, the Radix-2 Quasi-cyclic shift network (QSN) design [5] has performed better than all other designs. The QSN architecture has utilized two conventional logarithmic barrel shifters and a merge network to perform the required cyclic shifts for arbitrary number of inputs. This works present a novel idea of designing QSN based on high radix number system.

2 Radix-4 QSN architecture

Generally, the Radix-2 logarithmic barrel shifters consist of a base unit of two to one multiplexers. So, Radix-4 approach consists of four to one multiplexers. Radix-2 network can offer maximum two numbers of shifts at each stage (here, s = stage), i.e. 0×2^s and 1×2^s. So, intuitively the Radix-4 network offers maximum four numbers of shifts at each stage, 0×4^s, 1×4^s, 2×4^s and 3×4^s. Hence it offers shift amount of 0/1/2/3, 0/16/32/48 for first and third stage, respectively. Total numbers of stages required for shift value of *'N'* are $\lceil \log_4 N \rceil$. It is clear that total numbers of stages are reduced compared to Radix-2 [5], which are the core constituent of complexity and critical path. A 16×16 Radix-4 logarithmic barrel shifter using four to one multiplexers is shown in Fig. 1 (a).

Radix-4 QSN requires a base-4 representation of the shift amount. So, each stage requires a 2-bit control value. The most complex part of the barrel shifter architecture shown in Fig. 1 (a) is a fixed wired interconnecting network between the multiplexer stages. Each multiplexer needs four wired inputs. So, 16 multiplexers require total of 64 (=16 × 4) interconnecting wires and total of 128 interconnecting wires are required for two stage 16×16 barrel shifter shown in Fig. 1 (a). All the interconnections are implemented using Eq. (1).

$$iNum = (N - (miNum \times 4^{stage}) + mNum) \quad mod \quad N. \qquad (1)$$

where, *'N'* is a network size, *'iNum'* is a stage input, *'miNum'* is an input number of a 4×1 multiplexer and *'mNum'* is a multiplexer number. *I[0] to I[15]* inputs shown in Fig. 1 (a) are *iNum's* or stage inputs for first stage; while for all other stages, outputs of multiplexers from stage *'s-1'* are considered as stage inputs for stage *'s'*. *'miNum'* can take only four values (0, 1, 2

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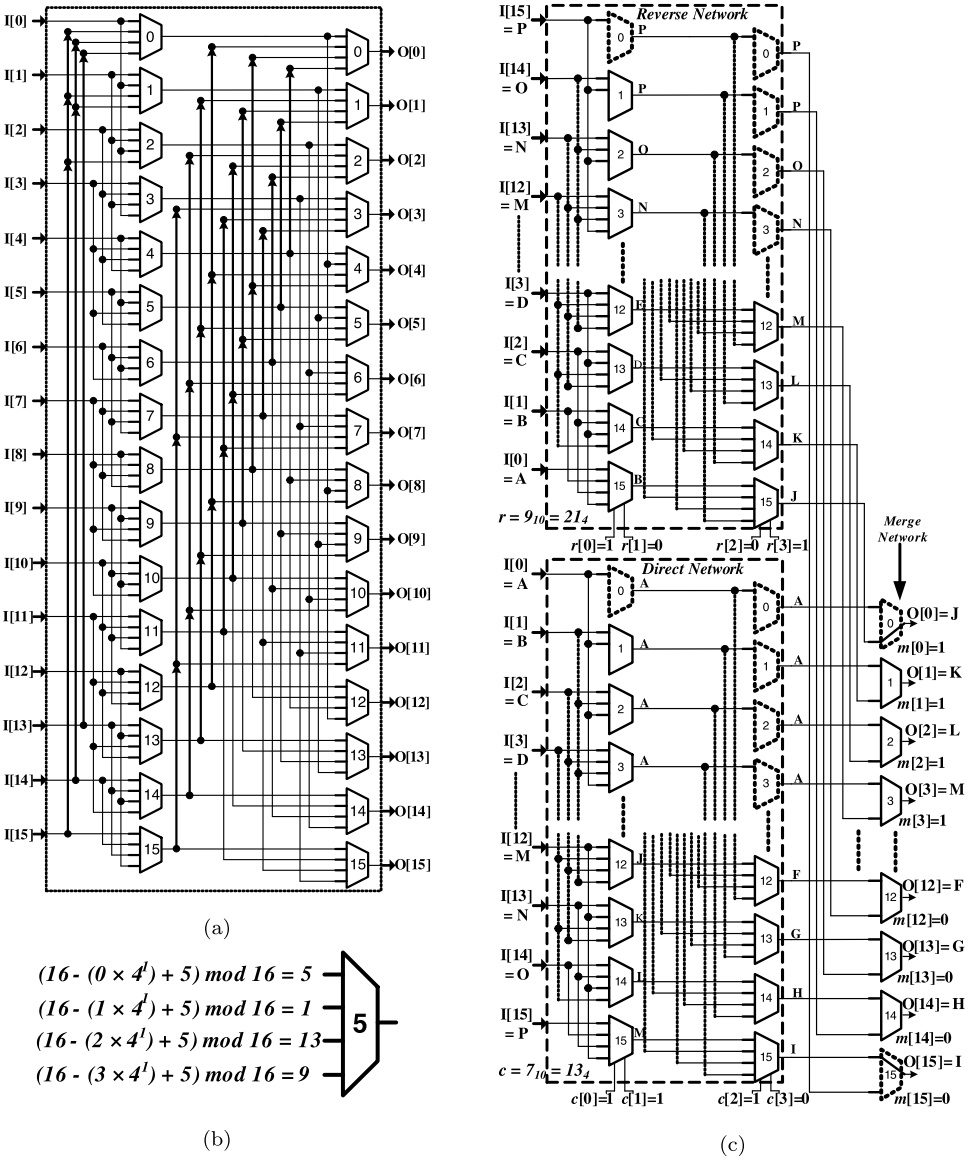

Fig. 1. (a) Radix-4 barrel shifter. (b) Interconnections for multiplexer #5 in 2^{nd} stage. (c) Proposed Radix-4 QSN architecture

and 3) for Radix-4 as all multiplexers require total of 4 inputs. *'mNum'* or multiplexer number is shown inside each multiplexer in Fig. 1 (a). Fig. 1 (b) shows that how multiplexer # 5 is connected in stage # 1 (2^{nd} stage) using Eq. (1).

Fig. 1 (a) shows two types of interconnecting wires, one with arrow head and others without arrow head. All the wires with the arrow head in upward direction are actually shifting the signals 'up' from their original input positions. For instance, first stage shifts the input signals by a maximum value of three. Thus, the last three signals are shifted in upward direction. The rest of the input signals can be shifted downward with respect to their original input positions. But when the number of inputs *(I[0] to I[n-1])* to the network are less than network size NS ($n < NS$), these upward signals become insignificant as last *'NS-n'* inputs are no longer present. The author

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Table I. Total multiplexers required for Radix-4 QSN

Stage	Mux	$N > 3(4^{s-1})$	$3(4^{s-1}) \geq N > 2(4^{s-1})$	$2(4^{s-1}) \geq N > 0$
s-1	$4-to-1$	$N - 3 \times 4^{s-1}$	-	-
	$3-to-1$	4^{s-1}	$N - 2 \times 4^{s-1}$	-
	$2-to-1$	4^{s-1}	4^{s-1}	$N - 4^{s-1}$
	$1-to-1$	4^{s-1}	4^{s-1}	4^{s-1}
zero to s-2	$4-to-1$	$\sum_{i=0}^{s-2}(N - 3 \times 4^i)$		
	$3-to-1$	$\sum_{i=0}^{s-2}(4^i)$		
	$2-to-1$			
	$1-to-1$			

$1-to-1$ *Mux = eliminated multiplexer,* N *= network size and* s *= stage.*

of QSN [5] solved the problem by using two barrel shifters instead of one and a merge stage to combine the outputs of two networks. The proposed architecture for Radix-4 QSN is shown in Fig. 1 (c). Direct network takes inputs from *I[0] to I[15]*; while reverse network takes inputs in reverse order, i.e. from *I[15] to I[0]*. Merge control signals are shown as m[i]. All the upward signals are eliminated in Fig. 1 (c) because now it is the responsibility of the second barrel shifter (or reverse network) to provide all the upward shifting signals to the merge network. The control value of direct network is *'c' (cyclic shift)*; while the control value for reverse network is *'r' (difference of number of inputs and cyclic shift amount)*. A merge network is used to merge the signals from both the networks, as shown in Fig. 1 (c). After the elimination of upward directed signals, first 4^s multiplexers in each stage are completely eliminated. Furthermore, second 4^s multiplexers turn into two to one multiplexers, while next 4^s multiplexers turn into three to one multiplexes. The rest are four to one multiplexers. These results provide a significant area reduction specifically, when the numbers of stages are large. The total number of multiplexers required for Radix-4 QSN are calculated using the Table I. The proposed complexity reduction method not only reduces number of multiplexers but also reduces the interconnecting wire required between stages. The interconnecting wires between stages are calculated using Eq. (2).

$$Total\,Wires = (4 \times N) - (1 \times 4^{stage} + 2 \times 4^{stage} + 3 \times 4^{stage}). \quad (2)$$

For 16×16 Radix-4 QSN network shown in Fig. 1 (c), first stage requires 58 (= 64 − 6) wires, while second stage requires 40 (= 64 − 24) wires. Hence, total of 196 (= 98×2) interconnecting wires are required for both 'direct' and 'reverse' network. While 16×16 Radix-2 QSN requires 226 (= 113×2) wires. Thus, 16×16 Radix-4 QSN network shows 13% saving in terms of interconnection complexity. The improvement in terms of interconnection complexity increases with the increase in network size.

3 Radix-4 signal generator

Signal generator consists of two parts; a merge stage signal generator and a reverse cyclic shift generator. Reverse cyclic shift is the difference of network size *'N'* and cyclic shift *'c'* value $(N - c)$. A subtractor generates a reverse cyclic shift. Merge stage selects a signal from direct or reverse network and routes a proper signal to the output, as shown in Fig. 1 (c). Merge network selects the output of reverse network for all upward directed signals and direct

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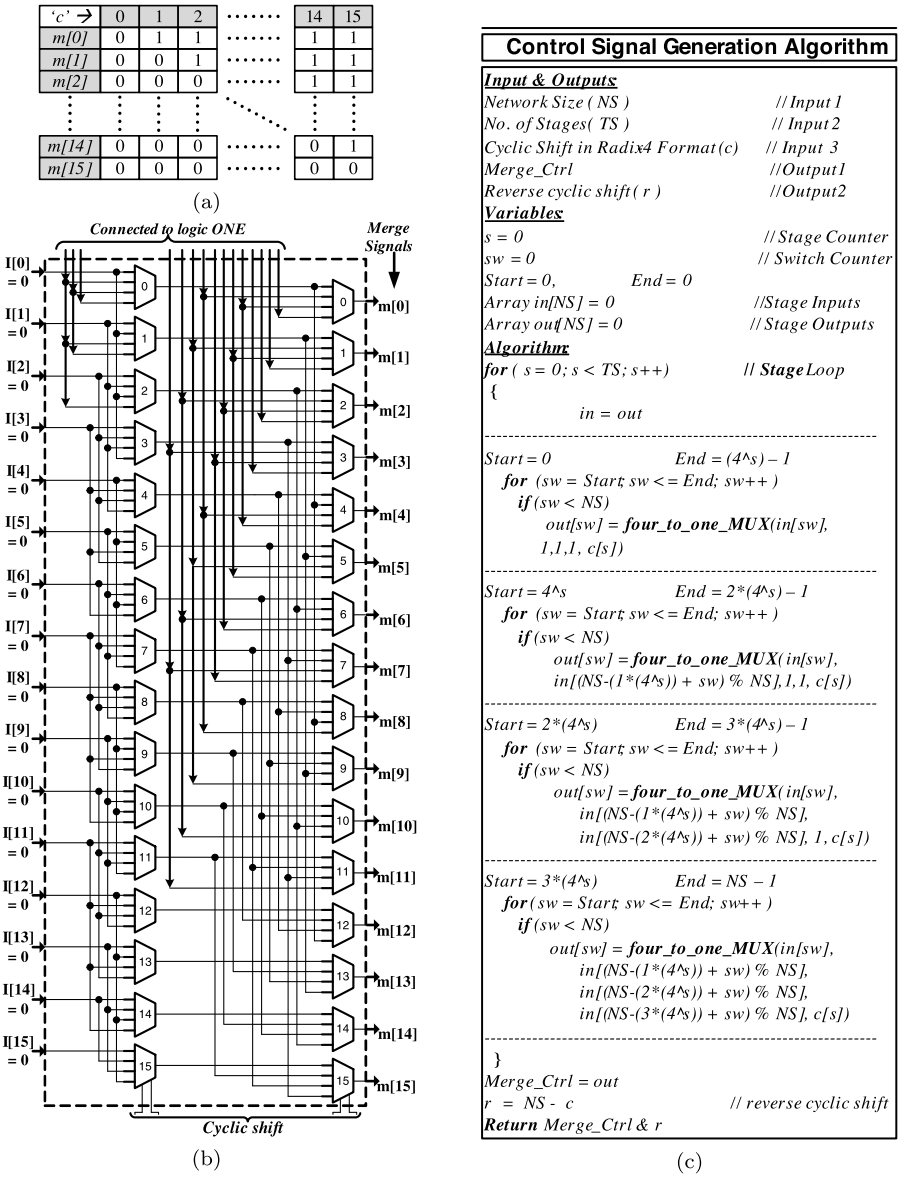

Fig. 2. (a) Merge control signals for 16×16 Radix-4 QSN. (b) Radix-4 barrel shifter setup for signal generator. (c) Proposed control signal generation algorithm for Radix-4 QSN

network for all downward directed signals. Hence, for a cyclic shift of seven on a 16 × 16 Radix-4 QSN network, the merge network selects first seven signals from the reverse network (m[0] to m[6]); while rest of the signals (m[7] to m[15]) are selected from direct network. So, it selects top 'c' (cyclic shift value) signals from reverse network and the rest from direct network. Even if the numbers of inputs are less than the total network size, it still selects top 'c' signals from reverse network. This fact actually simplifies the merge signal generator design compared to [5], because merge signal generator is independent of the sub network size. Thus, the merge control signals are directly the function of cyclic shift value.

A 16 × 16 Radix-4 QSN merge stage control signals (m[0] to m[15]) for a cyclic shift values from zero to 15 are shown in Fig. 2 (a). It is clear that the zeros are shifting in a cyclic shifting manner and each shifted zero is

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Table II. Implementation results (8-bit word length)

	Proposed (90-nm)			QSN [5] (180-nm)			OPN [3] (180-nm)		
	Total mm^2	*Control* mm^2	*Freq* MHz	*Total* mm^2	*Control* mm^2	*Freq* MHz	*Total* mm^2	*Control* mm^2	*Freq* MHz
32×32	0.0365	0.0014	800	0.160	0.0063	286	0.165	0.014	-
48×48	0.0588	0.0019	780	0.259	0.0086	250	0.289	0.049	-
64×64	0.0837	0.0023	765	0.368	0.0103	250	0.447	0.058	-
96×96	0.1317	0.0031	650	0.592	0.0144	200	0.722	0.114	94

replaced by one. So, the controller for the merge stage can be implemented as a Radix-4 barrel shifter with all inputs equal to zero. Furthermore, all the downward directed interconnecting wires are fed with the value of one, as shown in Fig. 2 (b). The control signal generation algorithm for Radix-4 QSN is shown in Fig. 2 (c), where *'four_to_one_Mux'* is a 4-to-1 multiplexer with control value *'c'*. Constant *'1'* input inside each 4-to-1 multiplexer depicts all downward directed signals connected to *'logic 1'*. Similar signals are shown in Fig. 2 (b) as *'connected to logic ONE'*. Moreover, Eq. (1) is used to make the connections between the multiplexer stages.

4 Implementation and comparison results

The proposed Radix-4 QSN design (with 8-bit word length) was modeled in Verilog HDL and synthesized with TSMC 90-nm CMOS technology (All the inputs and outputs were loaded with buffers). The layout was carried out using 9-layer metal technology.

Table II shows implementation and comparison results for proposed Radix-4 QSN architecture. It is clear that Radix-4 QSN performs much better compared to [3, 5]. A 96×96 network is the key requirement for IEEE 802.11n and IEEE 802.16e standard LDPC decoders. Generally, an area scaling factor of $(1.414^2)^2 \approx 4$ and a frequency scaling factor of $1.414^2 \approx 2$ is used to convert a 90-nm result to 180-nm result [6]. Thus, scaled area value for 96×96 network equals $0.1317 \times 4 = 0.527\,mm^2$, that translates to about 11% saving in terms of area compared to [5] and 27% compared to [3]. Scaled frequency value for 96×96 network equals $650 \div 2 = 325\,MHz$, which is about 38% and 70% higher than [5] and [3], respectively.

5 Conclusion

The proposed work describes an efficient Radix-4 QSN architecture for reconfigurable QC-LDPC decoders. This work paves a way for the development and implementation of high radix QSN network. A novel complexity reduction technique is described to reduce a gate count at each stage. Furthermore, a novel signal generator suitable for Radix-4 QSN is also proposed. The proposed design shows a definite performance improvement over its predecessor.

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