IEICE Electronics Express, Vol.7, No.4, 308–313

A 24 mW, 5 Gb/s fully balanced differential output trans-impedance amplifier with active inductor and capacitive degeneration techniques in 0.18 μm CMOS technology

B. Shammugasamy, T. Z. A. Zulkifli[a)], **and H. Ramiah**

RMIC Group, School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Malaysia

a) *eezainal@eng.usm.my*

Abstract: In this paper, a low power 24 mW 5 Gb/s differential output transimpedance amplifier (TIA) is realized in 0.18 μm CMOS technology for optical interconnect application. The TIA is a fully balanced and differential architecture design that can improve immunity with the common mode noise attributed to the power supply. The differential gain achieved is 66 dBΩ with a -3 dB bandwidth of 4.0 GHz for a 0.5 pF photodiode capacitance (C_{pd}) by implementing both the active inductor peaking and capacitive degeneration techniques. The TIA core consumes only 24 mW power from a single 1.8 V power supply while achieving the sensitivity of -19.0 dBm for a bit error rate (BER) of 10^{-12}.

Keywords: transimpedance amplifier, RGC, active inductor

Classification: Integrated circuits

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DOI: 10.1587/elex.7.308
Received January 06, 2010
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Published February 25, 2010

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1 Introduction

In the consumer electronics market for multimedia application, the high speed transmission standards such as High Definition Multimedia Interface (HDMI) plays a crucial role in transmitting uncompressed digital data. However, when it comes to digital transmission in HDMI technology, the fiber optic connection medium has always been preferred compared with the copper medium, as the signal transmitted through copper cable is prone to crosstalk and electromagnetic interference (EMI) issues, which significantly degrade the signal quality. As such, improving the existing optical system of HDMI is necessary to fulfill the ever increasing data bandwidth demand. TIA is one of the most critical blocks in the front-end optical receiver design. It converts the low amplitude input current signal to an amplified output voltage signal.

In the past, many papers featuring an optical receiver operating at 10 Gb/s in 0.18 μm CMOS technology were published. As the data rate for an HDMI interface is targeted at 5 Gb/s, the existing 10 Gb/s TIA design can still be employed to be integrated with the HDMI optical interface. However, it is not feasible due to its bulky design, as on chip spiral inductors are implemented for bandwidth extension. Yun et al. implemented an optical transceiver for HDMI application in 0.18 μm CMOS technology as in [1], but it was only up to a 4 Gb/s data rate. A low power 5 Gb/s TIA was published in [2], but it was fabricated using a higher cost 0.13 μm CMOS technology. Thus, this paper presents a low-power, high-gain, and fully balanced differential output TIA in 0.18 μm CMOS technology that operates up to 5 Gb/s of data rate. In this design, the existing Regulated Cascode (RGC) [3] architecture is modified for the gain and bandwidth extension together with the source degeneration differential amplifier to meet the 5 Gb/s design specification in HDMI interface. A dummy capacitor is placed externally to match the actual photodiode capacitance to improve the power supply rejection (PSR).

This paper is organized as follows. Section 2 describes the design of each blocks involved in the proposed 5 Gb/s TIA architecture. The simulated results of the proposed design are discussed in section 3. The conclusion is given in Section 4.

2 Differential Output TIA Circuit Implementation

In this design, RGC architecture is implemented at the input of the TIA design to prevent the photodiode capacitance (C_{pd}) from affecting the -3 dB bandwidth. The conventional RGC circuit is shown in Fig. 1 (a). To minimize the input referred noise for better optical input sensitivity, the TIA gain should be maximized [4]. Thus, to minimize the input referred noise by the

DOI: 10.1587/elex.7.308
Received January 06, 2010
Accepted January 22, 2010
Published February 25, 2010

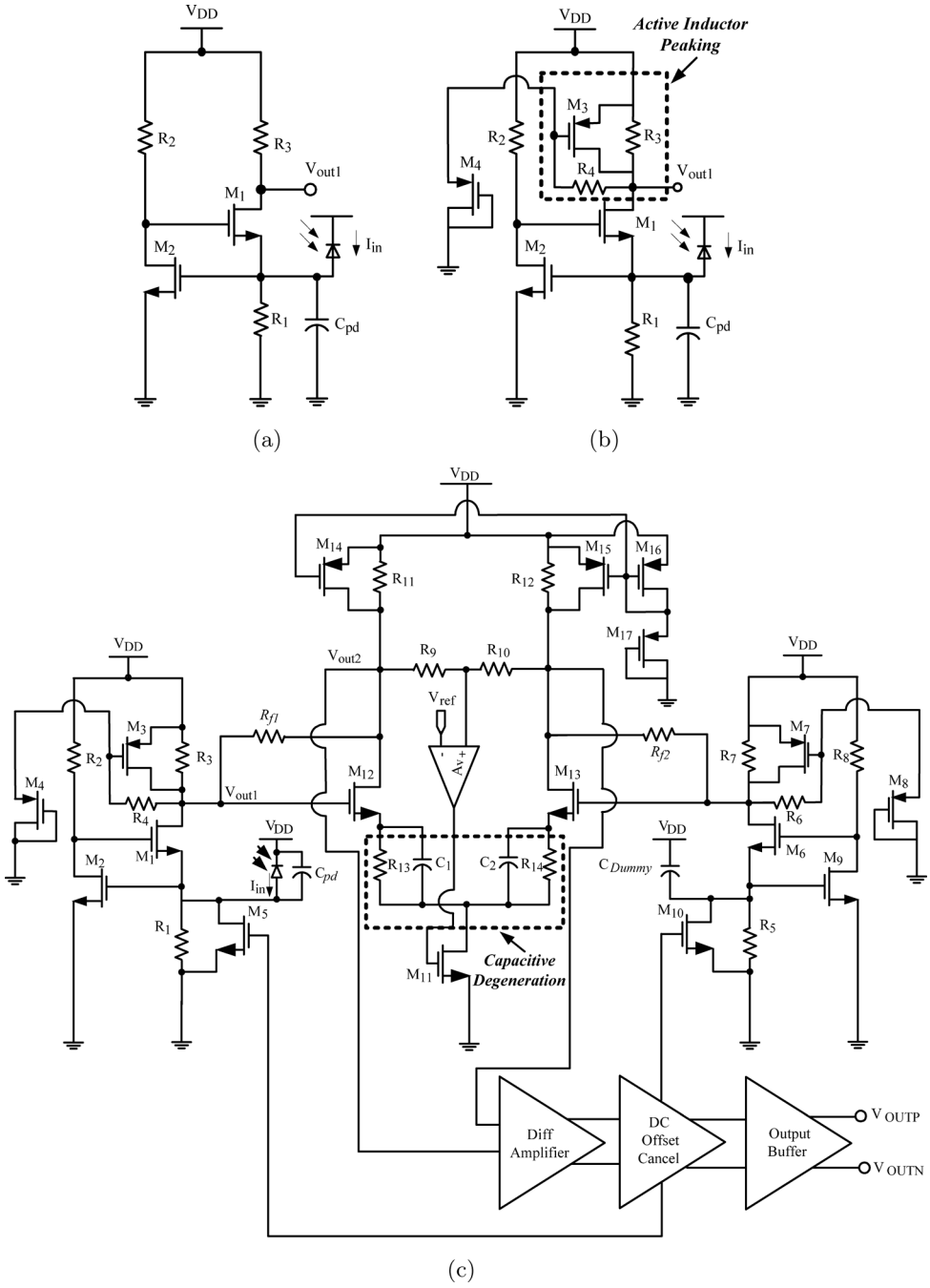

Fig. 1. (a) Conventional circuit of RGC, (b) Modified circuit of RGC, and (c) The proposed integrated differential output TIA circuit

RGC itself, the load resistor R_3 should be large. However, increasing the size of the load resistor cannot maintain the output dc voltage at 1.2 V for a larger signal swing, as the voltage headroom is limited for a larger biasing current especially for the bandwidth extension. Thus, the current bleeding technique [4] is adopted to improve the gain, which simultaneously lowers down the input referred noise as illustrated in Fig. 1 (b). Load resistor R_3 and PMOS transistor M_3 divide the biasing current at the output branch in order to set R_3 larger. To alleviate the output node bandwidth degradation of the RGC due to the increased R_3 size, the active inductor peaking technique

DOI: 10.1587/elex.7.308
Received January 06, 2010
Accepted January 22, 2010
Published February 25, 2010

is implemented together with the current bleeding technique, as discussed in [5]. In this design, the load from the PMOS M_3 gate to the ground terminal is carried out in a diode-connected PMOS M_4 configuration for minimum power consumption. Adding the active inductor peaking technique at the RGC output node increases the impedance at high frequency, which compensates for the drop in the load capacitance; thus, the bandwidth is extended. The output impedance of the RGC circuit is as follows:

$$\begin{aligned} Z_{out1}(s) \approx\ & R_3 \| r_{o3} \| \frac{sC_{gs3}R_4 + g_{m4}R_4 + 1}{sC_{gs3} + g_{m4} + g_{m3}} \| \\ & (r_{o1} + g_{m1}R_1 r_{o1}(1+A) + R_1). \end{aligned} \tag{1}$$

where R_1 is the input resistance of the TIA circuit; r_{o1} and r_{o3} are the output resistance of transistors M_1 and M_3, respectively; R_4 is the load resistance of the active inductor; A is the gain of the RGC local feedback; g_{m3} and g_{m4} are the transconductance of transistors M_3 and M_4, respectively; and C_{gs3} is the gate-to-source capacitance of transistor M_3. Assuming the right hand side of Eq. (1) in which the second and the fourth term are larger than the first and the third term, the following argument holds true. At DC, it reduces to $\lim_{s\to 0} Z_{out1}(s)R_{out1} \approx [R_3 \| (\frac{g_{m4}R_4+1}{g_{m4}+g_{m3}})]$, whereas as the frequency goes to infinity, it yields $\lim_{s\to\infty} Z_{out1}(s)R_{out1} \approx [R_3 \| R_4]$.

As a result, the bandwidth at the output node is extended. Shunt feedback topology is chosen as the following stage after RGC due to its low input impedance characteristics. To extend further the gain and bandwidth of this stage, the capacitive degeneration method is implemented, as shown in Fig. 1 (c). In this case, the zero that is created at the frequency of $(1/R_{13}C_1)$ cancels the pole at the shunt feedback output node. Although adding the source degeneration amplifier does decrease the gain linearly, the current bleeding technique employed in the load of this stage increases the overall gain that is limited by the voltage headroom. This technique was implemented by adding transistor M_{14} in parallel with load resistor R_{11}, while maintaining the same DC voltage drop at the output node. The RGC transimpedance gain is as follows:

$$R_{out1-in} = \frac{V_{out1}}{I_{in}} \approx \frac{(1/g_{m4})R_3 + R_3R_4}{(1/g_{m4}) + R_3 + R_4 + (g_{m3}/g_{m4})R_3}. \tag{2}$$

On the other hand, the shunt feedback DC gain is as follows:

$$\frac{V_{out2}}{V_{out1}} \approx \frac{(1 + g_{m12}R_{13} - g_{m12}R_{f1})(R_{11} \| r_{o14})}{(1 + g_{m12}R_{13})(R_{11} \| r_{o14} + R_{f1})}. \tag{3}$$

Also, the overall DC transimpedance gain from the RGC input to the shunt feedback output is given as follows:

$$\frac{V_{out2}}{I_{in}} \approx \frac{R_{load2}R_{out1-in}(1 + g_{m12}R_{13} - g_{m12}R_{f1})}{R_{load2} + R_{out1} + R_{f1} + g_{m12}R_{total}}, \tag{4}$$

in which $R_{total} = R_{out1}R_{13} + R_{f1}R_{13} + R_{load2}R_{13} + R_{load2}R_{out1}$, and $R_{load2} = (R_{11} \| r_{o14})$. Fig. 1 (c) illustrates the proposed fully balanced differential output circuit architecture. In this design, the RGC, shunt feedback, differential

DOI: 10.1587/elex.7.308
Received January 06, 2010
Accepted January 22, 2010
Published February 25, 2010

amplifier, DC feedback cancellation, common mode feedback (CMFB), and output buffer are integrated in a system level to form a differential architecture circuit. Another source degeneration differential amplifier stage is added to boost further the overall gain of TIA. Thus, the overall −3 dB bandwidth of the TIA is determined by the output pole of the differential amplifier, which is eventually compensated by the zero created by the stage itself. Adding a CMFB circuit in the TIA system maintains the common mode output DC voltage at 1.2 V at each block across process, voltage, and temperature (PVT) variations. As the proposed architecture is fully differential for better common mode noise rejection, the TIA needs to be integrated with a DC offset feedback cancellation circuit. To overcome the load of the preceding stages, frequency-doubler architecture [4] is adopted as the 50 Ω output buffer. The output buffer is designed with a gain in the range of 1 dB and an expected output load capacitance of 0.1 pF.

3 Simulation Results

Table I summarizes the simulated performance of the differential TIA. A total gain of 66 dBΩ and a 4.0 GHz bandwidth are achieved with an input photodiode capacitor of 0.5 pF and an expected wirebond inductance of 1 nH. The simulated TIA achieves an input current sensitivity of −19.0 dBm for a BER of 10^{-12} with the assumed extinction ratio and photodiode responsivity of 9 dB and 0.85 A/W, respectively. The TIA achieves an input current dynamic range of 36 dB. The TIA core and DC feedback circuit consumes only 24 mW of DC power, while the output buffer itself consumes 25 mW of power. The implementation of both the active inductor peaking and capacitive degeneration techniques extends the bandwidth of the proposed differential TIA with an almost flat gain frequency response for wideband range operation. The transient simulation was performed with a pseudorandom bit stream (PRBS) of 2^{23-1}. Figs. 2 (a), 2 (b), 2 (c) and 2 (d) illustrate the simulated eye diagram at 1.25 Gb/s, 2.5 Gb/s, 3.125 Gb/s, and 5 Gb/s data rate, respectively, with the noise option in the circuit simulator enabled at an input sensitivity of −19.0 dBm. The TIA gain frequency response and equivalent input noise of the TIA are shown in Figs. 2 (e) and 2 (f).

Table I. Performance summary of the differential TIA

Parameter	This work	[2]
Power consumption (Core Design)	24 mW	14 mW
Supply Voltage, V_{DD}	1.8 V	1.8 V
Bandwidth, −3 dB	4.0 GHz	4.2 GHz
Transimpedance Gain	66 dBΩ	52.8 dBΩ
Data Rate	5 Gbps	5 Gbps
CMOS Technology	0.18 μm	0.13 μm
Optical Sensitivity	−19.0 dBm	N/A
Input Dynamic Range	36 dB	N/A
Photodiode Capacitor, C_{pd}	0.5 pF	1.0 pF

DOI: 10.1587/elex.7.308
Received January 06, 2010
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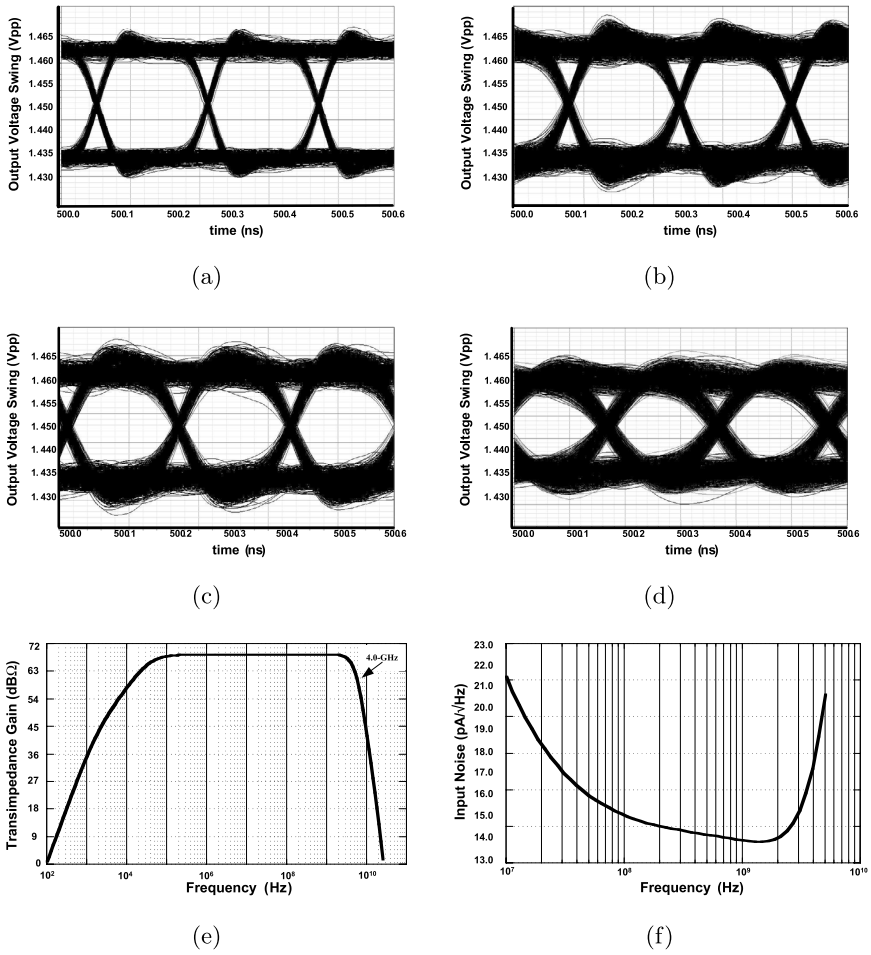

Fig. 2. Eye-diagram at (a) 1.25-Gb/s, (b) 2.5-Gb/s, and (c) 3.125-Gb/s, (d) 5-Gb/s, (e) TIA Gain vs Frequency Response, and (f) TIA Equivalent Input Noise Response

4 Conclusion

A fully balanced differential TIA was designed in 0.18 μm CMOS technology operating at 5 Gb/s. The TIA achieved a differential gain of 66 dBΩ with an input sensitivity of -19.0 dBm. The proposed TIA can be implemented in the HDMI interface for optical analog front-end due to its low power design and good optical sensitivity.

Acknowledgments

This project was partially supported by the MOSTI EScienceFund, with grant no. 03-01-05-SF0302. The authors would like to express their sincerest appreciation to all the RMIC group members and to Silterra Malaysia Sdn. Bhd.

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