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A novel adder cell for ultra low voltage, ultra low power networks in nanoscale VLSI circuits

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Abstract: A novel full adder cell is designed so that it can overcome the challenges of circuit design in deep submicron (DSM) technology. The proposed adder cell utilizes multiplexing control input techniques (MCIT) for the sum operation and uses a new arrangement of pass transistors for carry operation. The adder is then used in an 8×8 bit Braun-array multiplier to show its performance. The layout of multiplier is simulated in 32 nm CMOS technology by Microwind31 (MW31) VLSI CAD TOOL. Simulated results show that our circuit operates properly in nanoscale and has a very small area.

Keywords: 32 nm CMOS, 8×8 bit multiplier, BSIM4, full-adder, ultra-low-voltage

Classification: Integrated circuits

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1 Introduction

Increasing demand for faster, smaller, cheaper and less in need of battery recharge, portable electronic devices, has encouraged researchers to work on different optimization methods both in high level [1, 2] and low level [3, 4] design sequences.

Decreasing the minimum feature size in CMOS technology [5] is a common optimization method that can significantly decrease the power and area of the circuit. But as we move to DSM technology, more unwanted effects such as leakage, come into account [5, 6, 7]. As a result of these effects, a lot of former architectures can not be directly used in DSM technology and need to be modified or replaced with new ones. One of these structures is the MCIT based adder of [3] that has a small area but it can not be used in DSM technology because of a number of problems such as leakage, so in this work, at first the leakage mechanisms in DSM technology are introduced. The problems of the MCIT based adder of [3] in DSM technology are then discussed. According to these problems and based on the former architecture, a modified full adder for DSM technology is then proposed. This structure is then used to implement a multiplier in DSM technology to depict its performance in terms of functionality and area efficiency.

2 Leakage in deep submicron technology

For any MOS transistor, there is a threshold voltage (Vth). Below this voltage, the channel gradually disappears and the current decreases exponentially. In long channel CMOS circuits, operating voltages are considerably larger than Vth and leakage can be neglected in many cases but in DSM circuits the operating voltages are close to threshold voltages and the leakage current becomes significant. This current may even affect the functionality of the circuit.

The leakage current is made of three major components [6], the first one is subthreshold leakage that flows between drain and source in the subthreshold region. Eq. (1) can be used to obtain the value of this current.

$$I_{ds} = Ke^{(V_{gs}-V_{th})/(nV_T)}(1 - e^{-V_{ds}/V_T}) \tag{1}$$

Where I_{ds} is the subthreshold leakage current, K is a function of technology, V_T is the thermal voltage, V_{ds} is the drain-source voltage and V_{gs} is the gate-source voltage.

The second component is the gate leakage that is caused by the tunneling effect through the thin oxide layer of the gate. Eq. (2) can be used for calculation of the value of this current.

$$I_{ox} = K_1 W(V_{DD}/T_{ox})^2 e^{-aT_{ox}/V_{DD}} \tag{2}$$

Where Tox, Iox are the gate oxide thickness and leakage current respectively, K1 and a are experimentally derived parameters and W is the channel width.

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The third component of leakage in DSM circuits is the current that flows through the reverse biased p-n junctions of drain-substrate and source-substrate and is called junction band-to-band tunneling (BTBT) current. The mentioned leakage components for a NMOS transistor in off state with a gate voltage of zero and a drain voltage equal to the supply voltage are depicted in Fig. 1 (a).

3 Conventional adder cell of [3]

In [3] a Shannon-Based adder cell is designed so that it uses the MCIT for the sum operation and the Shannon theorem for the carry operation. This circuit is shown in Fig. 1 (b). The three inputs of the full adder are represented as A, B, C and its carry and sum outputs are represented as C0, S respectively.

The simulated input and output (I/O) curves of the generated layout of the proposed adder of [3] in 32 nm technology are presented in Fig. 1 (c). As seen from the curves, the sum output doesn't have a complete swing because of the voltage drop on the NMOS transistors. The carry circuit has also two problems, the first one is that it doesn't generate '0' logic value, because the three branches of the carry circuit are connected to V_{DD} and are only used to pass '1' logic level and the second problem that makes the carry circuit uselss in DSM technology is the leakage, that explains the shape of C0 signal in Fig. 1 (c).

Fig. 1 (d) shows a branch of the carry circuit with some of the leakage paths. When the supply voltage is applied to the circuit and the input signals are low, the transistors of this branch are in off state but the leakage mechanisms in DSM technology cause the leakage currents to flow in the paths shown in Fig. 1 (d). In fact the currents that flow in the V_{DD} to C0 direction are subthreshold currents and the currents that flow through the gates are gate oxide leakage currents. The BTBT leakage current also exists in this circut but it is not shown in the figure.

When these currents flow through the transistors, the drain-source paths, show a limited resistance and this causes the V_{ds} voltages to drop gradually with increasing of the currents. At last the voltage drop on the transistors becomes very small and the V_{DD} appears in the output. After this second, the output is in high state independent of the state of input signals that are applied to the transistors. It is clear that during the transition of C0 to get to its final value, any arrangement of input signals that makes the C0 high, can expedite the process of transition as seen in Fig. 1 (d).

4 Proposed adder cell

The proposed adder of this letter is shown in Fig. 1 (e). This adder utilizes the MCIT structure of former architecture for sum operation, but with two CMOS inverters in series with the output to compensate the voltage drop on NMOS transistors.

The carry circuit utilizes PMOS transistors to transfer logic '1' and NMOS transistors to transfer logic '0'. This work solves the problem of voltage drop

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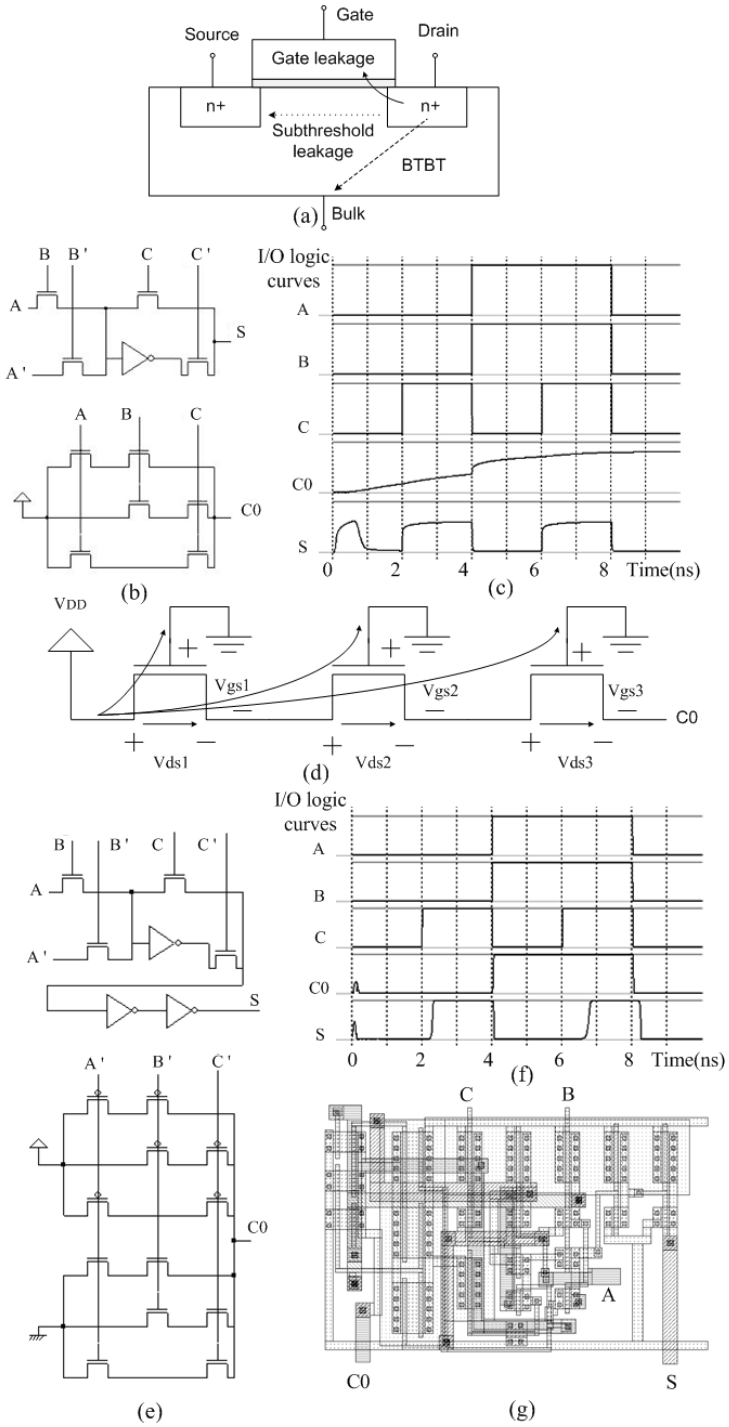

Fig. 1. (a) Leakage mechanisms (b) Shannon-based adder cell of [3] (c) Simulated I/O curves of [3] in 32 nm technology (d) Some leakage paths in carry circuit (e) proposed full adder (f) Simulated I/O curves of the proposed adder (g) layout of the proposed adder

at the output node. The problem of leakage is also solved because every NMOS branch is connected to ground and every PMOS branch is connected to V_{DD}; so the powerful electrical fields that caused leakage currents in the off state transistors, are eliminated in the proposed structure. Layout of the

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proposed adder cell in 32 nm technology is simulated using the BSIM4 Spice Model considering parasitic capacitances that are extracted from the layout. The simulated I/O curves and layout of the proposed adder are shown in Fig. 1 (f) and Fig. 1 (g) respectively. As it can be seen from the curves, the output nodes of the circuit have complete swing. So this architecture can operate properly in a 32 nm logic network.

5 Nanoscale, 8×8 bit multiplier

The proposed full adder, is used to implement an 8×8 bit Braun-Array multiplier. Fig. 2 shows an example of its simulated output curves.
As seen from the curves, this circuit operates properly as a multiplier in

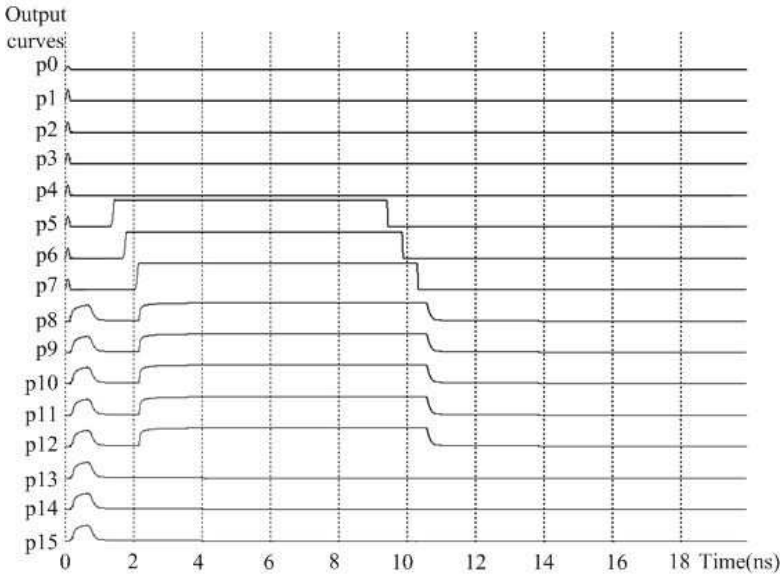

Fig. 2. Simulated output curves of the multiplier in 32 nm CMOS technology

32 nm technology and this means that our goal is achieved. Table I (a) and Table I (b) show the specifications of the proposed adder and multiplier respectively.

The increased number of transistors, in our proposed adder cell and also using PMOS transistors in it, may seem to be a problem because it can increase the area of the chip; but it should be noted that when technology scales down from 0.35 μm to 32 nm the problem of area is automatically solved and the functionality of the circuit is in more priority than its size and as discussed before, the conventional structure of [3] can not operate properly in DSM technology. Another fact is that with a denser layout, the extra area of the added transistors can be compensated. Our simulation results are compared with the estimated area of the multipliers of [3] in 32 nm technology. These estimated values are achieved by utilizing full scaling rules [5]. By utilizing these rules, if we respectively represent the channel length, width and area of a MOS device by "L", "W" and "A" and also define the scaled

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values by a prime notation then we will have:

$$A' = W'L' = \frac{WL}{\alpha^2} \Longrightarrow A' = \frac{A}{\alpha^2} \tag{3}$$

In these relations "α" represents the scaling constant. When the technology is decreased from 0.35 μm to 32 nm we have:

$$\frac{350\,nm}{32\,nm} \approx 10.94 \tag{4}$$

So the scaling can be done with α=10.94. Table I (c) shows the scaled values of area for the Braun-array multipliers of [3] in 32 nm technology and also their comparison with the area of our multiplier. As it can be seen from

Table I.

(a) proposed adder specifications

average power(μw)	delay (ns)	area (μm^2)	num of NMOS transistors	num of PMOS transistors
0.484	0.5	9.6	12	16

(b) implemented multiplier specifications

average power(μw)	max. delay(ns)	area (μm^2)	supply voltage(v)	technology
84	3.5	36×23	0.35	32 nm

(c) Scaled results of a 8×8 bit multiplier with different adders in 32 nm

adder type	MCIS	CPL 12T	Shannon-based	proposed
Area $(\mu m)^2$	3173.5	2710.4	1661.07	828
% area reductin	73.91	69.45	50.15	-

Table I (c), area of our multiplier is extremely less than the estimated area of multipliers with the same architecture and different adder cells in 32 nm technology. So we can claim that the dense layout of our proposed multiplier has compensated the extra area of the increased number of transistors.

6 Conclusion

Simulated results of the proposed adder cell, showed that it operates properly in 32 nm CMOS technology, and this architecture solves the problems of the MCIT based adder of [3]. An 8×8 bit multiplier was implemented using the proposed adder cell, and the simulation results showed that this multiplier operates properly in DSM technology. So the goal of achieving a full adder with good performance in small sized, DSM digital circuits is achieved.

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