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Two-stage digital I/Q demodulator employing a reconfigurable 16-phase down-mixing technique

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Abstract: This letter presents a new two-stage digital I/Q demodulator employing a reconfigurable 16-phase quadrature intermediate frequency (IF) sampling technique for multistandard wireless systems such as mobile TV applications. The proposed two-stage digital I/Q demodulator provides the flexibility for the multiphase scheme such as a quadrature phase shift keying (QPSK) and 16-quadrature amplitude modulation (QAM) at the level of down-mixing, which introduces an efficient architecture for the following decimation filter. In this letter, the prototype chip has been implemented in a 0.18 μm standard CMOS technology and occupied with the active chip area of 0.02 mm^2. The power consumption of the fabricated chip is 0.42 mW with a 1.8 V supply voltage at the sampling frequency of 26 MHz. The experimental results show that the proposed two-stage digital I/Q demodulator is suitable for multistandard wireless systems which require small silicon area and low power dissipation.

Keywords: demodulation, down-mixing, quadrature, sigma-delta
Classification: Integrated circuits

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1 Introduction

Recently, the continuous and rapidly increasing growth in the consumer electronics field and advances in semiconductor technology have accelerated the digital convergence between various wireless applications such as cellular phone, mobile internet device (MID), and mobile TV. For example, a digital multimedia broadcasting function has been integrated into a handheld device such as a smart phone. As a result, it is necessary that multifunctional and multistandard features have to be included into just one device [1, 2]. In order to accomplish these requirements, the proper choice of system architecture and efficient implementation of the adopted architecture has been required.

For years, owing to the flexibility and efficiency of digital signal processing (DSP), versatile realization schemes have been presented mainly in the digital domain [3]. In general, since there are limitations of resources such as silicon area and power dissipation, a reconfigurable architecture has been preferred for implementation in the digital regime. In wireless systems, a digital modulation scheme uses a finite number of distinct signals to represent the digital data. Among the various digital modulation techniques, a quadrature phase shift keying (QPSK) and 16-quadrature amplitude modulation (QAM) are widely adopted [4]. This letter proposes a new two-stage digital I/Q demodulator using a reconfigurable 16-phase quadrature intermediate frequency (IF) sampling technique for multistandard wireless systems.

2 System architecture

Fig. 1 (a) shows a block diagram of the wireless receiver architecture using a digital IF topology, which is one of the strong candidates for reconfigurable wireless systems. The dotted boxes illustrate the output spectrum at each

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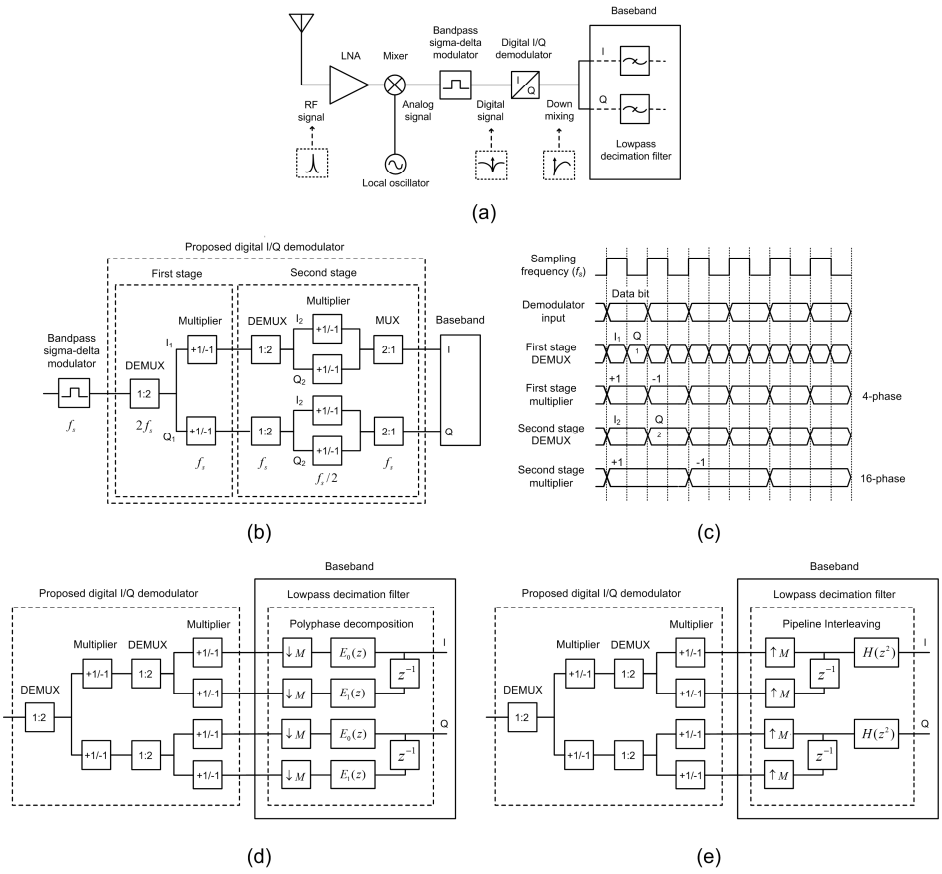

Fig. 1. The proposed two-stage digital I/Q demodulator: (a) Wireless receiver architecture using a digital IF. (b) Block diagram. (c) Timing scheme. (d) Application for polyphase decomposition of decimation filter. (e) Application for pipeline interleaving of decimation filter.

section, which identify the change of signal in the received path. As shown in Fig. 1 (a), the transmitted RF signal is received through the antenna, which is mixed with the local oscillator (LO). The resulting signal is called an IF signal, which is also converted to the bandpass digital IF signal which has noise shaping components. After this stage, the signal is processed in the digital domain. The digital I/Q demodulator takes a quadrature IF sampling process which obtains the I/Q channel signal. The sine and cosine signals are adopted to demodulate the received IF signal, which provide the bit sequences for I/Q channels, respectively. As a consequence, the bandpass IF signal can be expressed as

$$X(t) = A(t)\cos\left[\omega_o t + B(t)\right] = I(t)\cos\omega_o t - Q(t)\sin\omega_o t \qquad (1)$$

where $X(t)$ is the bandpass IF signal, $A(t)$ is the amplitude of $X(t)$, and $B(t)$ is the phase of the $X(t)$ [5].

Since the mismatch between the I/Q signal branches introduce an overall I/Q imbalance and significantly affects the system performance [6], the adoption of single path is desirable for elimination of the I/Q mismatch.

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Furthermore, through this digital I/Q demodulation, the bandpass digital IF signal is converted to the lowpass digital IF signal, as illustrated in Fig. 1 (a). The lowpass decimation filter in the next section reduces the data rate. In general, since the overall complexity of the digital system is mainly due to the digital decimation filters [7], it is necessary to reduce the system requirements for the following digital filter section. Since the DSP sections are more flexible than the analog circuit sections, the digital blocks such as the digital I/Q demodulator and decimation filter can provide a reconfigurable architecture.

3 Proposed two-stage digital I/Q demodulator

Fig. 1 (b) shows the block diagram of the proposed two-stage digital I/Q demodulator. The proposed two-stage digital I/Q demodulator is realized using a demultiplexer, multiplier, and multiplexer (MUX). Fig. 1 (c) illustrates the timing scheme of the proposed two-stage digital I/Q demodulator at each stage. As depicted in Fig. 1 (c), after the first stage, the resulting output bits have 4-phase data such as I_1, 0, $-I_1$, and 0 at the I channel. The following second stage processes the output bits of the first stage of the I channel. Thus, 8-phase quadrature demodulations such as I_1I_2, 0, $-I_1Q_2$, 0, $-I_1I_2$, 0, I_1Q_2, and 0 are obtained, sequentially. On the other hand, the resulting output bits also have 4-phase data such as 0, Q_1, 0, and $-Q_1$ at the Q channel. The following second stage processes the output bits of the first stage at the Q channel. Therefore, 8-phase quadrature demodulations such as 0, Q_1I_2, 0, $-Q_1Q_2$, 0, $-Q_1I_2$, 0, and Q_1Q_2 are also obtained, sequentially. In this work, since the proposed two-stage digital I/Q demodulator adopts a quadrature IF sampling technique which reflects data bits at 90° intervals, there is no linearity problem in the multiphase scheme. As a result, the proposed digital I/Q demodulator provides 16-phases using a two-stage I/Q demodulation technique, which can be reconfigurable for various modulation schemes such as a QPSK and 16-QAM. The lowpass decimation filters in the next stage attenuate the quantization noise and adjacent channels in the I/Q paths, respectively.

Fig. 1 (d) depicts the system architecture which adopts the polyphase decomposition for the following decimation filter. In general, the polyphase decomposition architecture is more efficient than the conventional structure for the decimation filter section [8]. A proper choice of the first stage at the decimation filter section can improve considerably the power consumption, silicon area, and maximum sampling frequency. Fig. 1 (e) shows the system architecture which adopts the proposed two-stage digital I/Q demodulator and the decimation filter using pipeline interleaving (PI) technique. The pipeline interleaving technique introduces the efficient architecture [9]. Furthermore, since it is not necessary to use a MUX at the output of the second stage, the proposed two-stage digital I/Q demodulator is suitable for the decimation section which adopts the pipeline interleaving structure.

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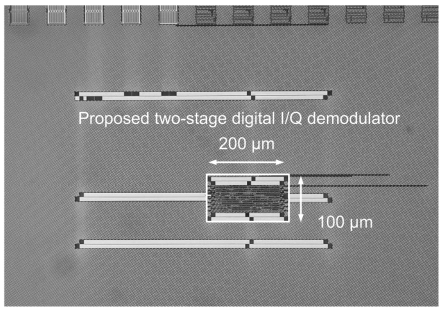
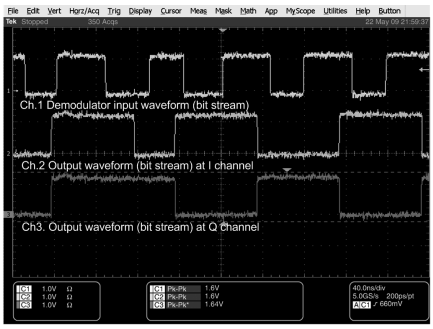
4 Measurement results

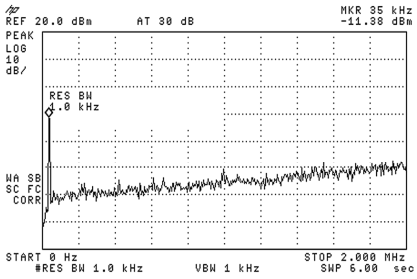
Fig. 2 (a) shows the micrograph of the prototype chip. The proposed two-stage digital I/Q demodulator has been fabricated in a 0.18 μm standard CMOS technology. In this work, the proposed digital I/Q demodulator occupies a silicon area of 200 μm $\times$ 100 μm (0.02 mm^2).



(a)



(b)



(c)

Fig. 2. (a) Micrograph of the prototype chip. (b) Measured output waveform in time domain. (c) Measured output spectrum of I channel in frequency domain.

The prototype chip adopts a sampling frequency of 26 MHz which has been widely used in recent wireless systems [1]. The sampling frequency of 26 MHz is generated by a signal generator, which provides a reference clock frequency. Moreover, since the input signal is located at a quarter of the sampling frequency, the input signal of 6.5 MHz is adopted. In this work, a fully differential input signal of 6.5 MHz is generated by an arbitrary waveform generator (AWG). The initial input signal which is generated by the AWG is processed by the bandpass sigma-delta modulator with the sampling frequency of 26 MHz. As a result, the bandpass sigma-delta modulated signals are fed to the input of the proposed digital I/Q demodulator.

A bit error rate (BER) is usually adopted for the overall system performance. The BER data is measured in terms of the number of errors that occur within a given sequence of bits. An error vector magnitude (EVM) also shows the deviation of a received constellation from an ideal reference constellation. The eye diagram is generally used to define the signal integrity. However, since this work is not focused on overall receiver system, the mea-

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Table I. Performance summary

Parameter	This work		[1]	[2]
Technology [μm]	0.18		FPGA	0.25
Supply voltage [V]	1.8		1.8	1.0
Clock frequency [MHz]	26		26	30.72
Input frequency [MHz]	6.5		6.5	8.192
Power consumption [mW]	0.42		-	5.6 (filter)
Chip area [mm²]	0.02		0.08	0.03
Phase scheme	16		4	4
Circuitry	Digital		Digital	Digital
Flexibility	Reconfigurable		Fixed	Fixed
Bandwidth [MHz]	1.536	8	1.536	1.536
Application	T-DMB	DVB-H	T-DMB	DAB

surements of BER, EVM, and eye diagram are not adequate. Since the digital I/Q demodulations are processed before the decimation filtering, the output bits of the digital I/Q demodulator include the noise shaping components. Therefore, there is no meaning to measure the BER, EVM, and eye diagram without decimation filtering. In order to measure an accurate BER, EVM, and eye diagram of complete receiver, it is necessary to integrate other digital blocks in future work.

Fig. 2 (b) shows the output waveform in time domain, which is measured by oscilloscope. The waveform at channel 1 depicts an input signal for the proposed digital I/Q demodulator, which is bandpass sigma-delta modulated. The waveform at channel 2 shows an output signal at I channel, which is lowpass sigma-delta modulated at down-mixing. The waveform at channel 3 is the output signal at Q channel, which is also lowpass sigma-delta modulated at down-mixing. In this case, since both I/Q channels are measured in time domain, they are depicted as bit streams. Fig. 2 (c) shows the measured output spectrum of I channel in frequency domain, which is measured by spectrum analyzer. In this case, the output spectrum of the proposed two-stage digital I/Q demodulator is lowpass sigma-delta modulated with noise shaping components. In other words, the bandpass sigma-delta modulated signal of 6.5 MHz is down-converted to the lowpass sigma-delta modulated signal of baseband such as 35 KHz. As a result, the measured output spectrum shape is closed to the theoretical expectation which is confirmed the operation of the proposed digital I/Q modulator, as illustrated in Fig. 1 (a).

Table I shows the performance summary of the proposed two-stage digital I/Q demodulator together with previous works [1, 2]. Since the previous digital I/Q demodulators have been realized using a field programmable gate array (FPGA) or different CMOS technology, there is a limitation to compare the performance in same condition. Here, DAB stands for digital audio broadcasting. As shown in Table I, the proposed digital I/Q demodulator supports various mobile TV applications such as the provision of a 1.536 MHz bandwidth for the terrestrial digital multimedia broadcasting (T-DMB) system and an 8 MHz bandwidth for the digital video broadcasting handheld (DVB-H) system.

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5 Conclusion

This letter discusses a new two-stage digital I/Q demodulator employing a reconfigurable 16-phase quadrature IF sampling technique for multistandard wireless systems such as mobile TV applications, which provides the flexibility required for the multiphase digital modulation schemes such as QPSK and 16-QAM at the level of down-mixing. The proposed digital I/Q demodulator relieves the overload to the following DSP section, which can be applied to efficient decimation filter schemes such as polyphase decomposition and pipeline interleaving. The proposed digital I/Q demodulator has sufficient efficiency in chip area and power dissipation, which can further accelerate the digital convergence between different wireless systems.

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